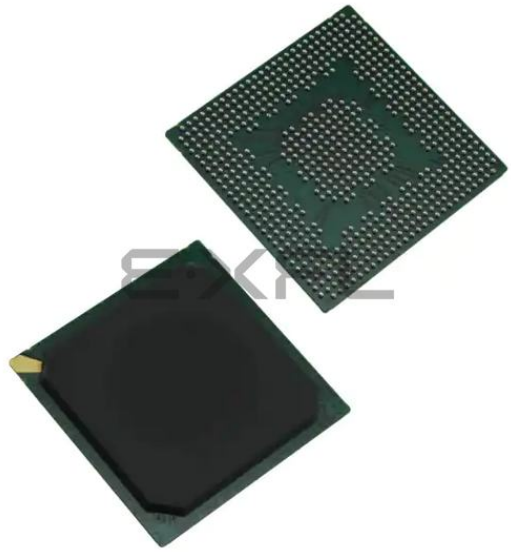

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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Security; SEC 3.3
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8315evragda

CAUTION

When the device is in D3 warm (standby) mode, all external voltage supplies applied to any I/O pins, with the exception of wake-up pins, must be turned off. Applying supplied external voltage to any I/O pins, except the wake up pins, while the device is in D3 warm standby mode may cause permanent damage to the device.

An example of the power-up sequence is shown in Figure 4 when implemented along with low power D3 warm mode.

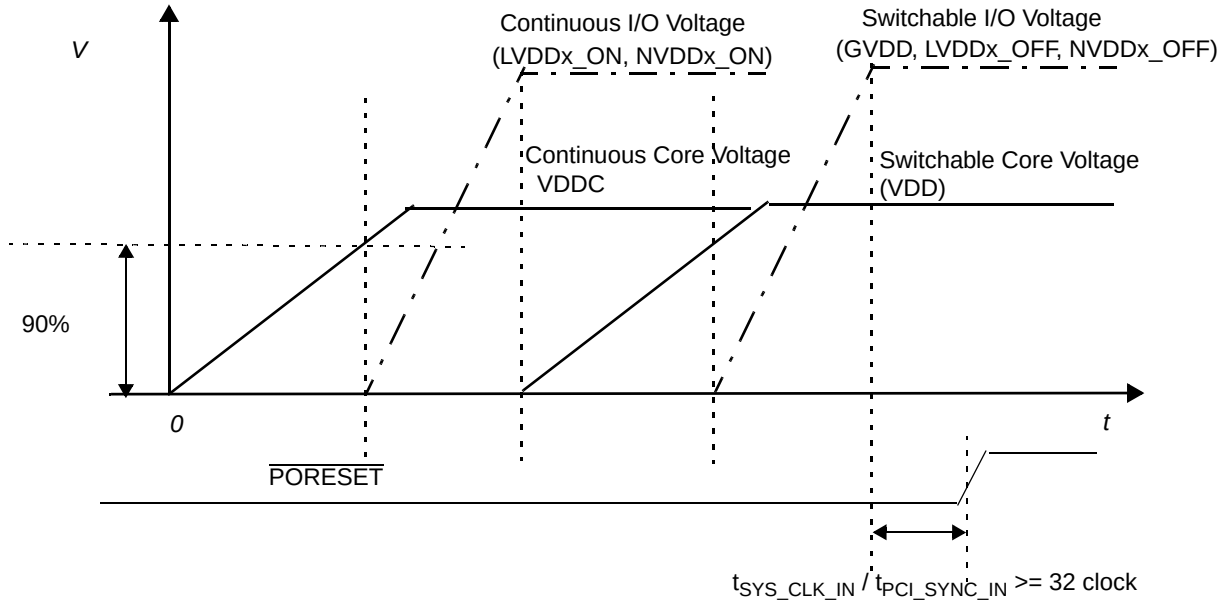

Figure 4. Power Up Sequencing Example with Low power D3 Warm Mode

The switchable and continuous supplies can be combined when the D3 warm mode is not used.

The SATA power supplies VDD33PLL and VDD33ANA should go high after NVDD3_OFF supply and go low before NVDD3_OFF supply. The NVDD3_OFF voltage levels should not drop below the VDD33PLL, VDD33ANA voltages at any time.

Table 28. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load.

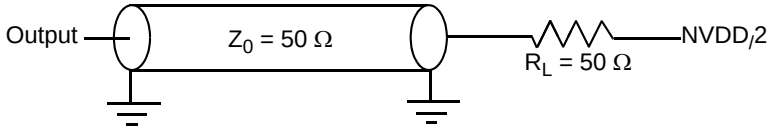

Figure 14. AC Test Load

This figure shows the RMII receive AC timing diagram.

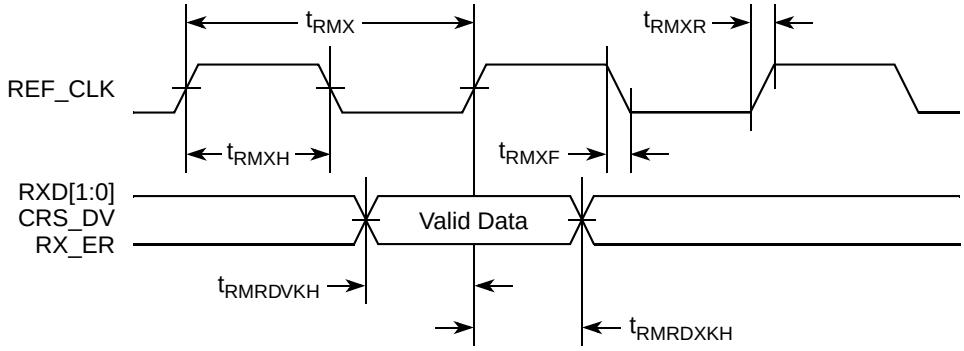

Figure 15. RMII Receive AC Timing Diagram

9.2.3 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 29. RGMII and RTBI AC Timing Specifications

At recommended operating conditions (see Table 2)

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	–0.6	—	0.6	ns
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.6	ns

Table 33. 1588 Timer AC Specifications (continued)

Parameter	Symbol	Min	Max	Unit	Note

Note:
1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected.
2. Asynchronous signals.
3. Inputs need to be stable at least one TMR clock.

9.5 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-Coupled serial link from the dedicated SerDes interface of MPC8315E as shown in Figure 18, where C_{TX} is the external (on board) AC-Coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XCOREVSS. The reference circuit of the SerDes transmitter and receiver is shown in Figure 49.

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines described in Section 26.4, "Connection Recommendations," as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the TSEC_GTX_CLK125 clock is not required for this port. Instead, SerDes reference clock is required on SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ pins.

9.5.1 DC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 15, "High-Speed Serial Interfaces (HSSI)."

9.5.2 AC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

This table lists the SGMII SerDes reference clock AC requirements. Please note that SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

Table 34. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Unit	Note
t_{REF}	REFCLK cycle time	—	8	—	ns	—
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

9.5.3 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 35 and Table 36 describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX[n] and $\overline{\text{SD\_TX[n]}}$) as depicted in Figure 17.

Table 35. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	XCOREVDD	0.95	1.0	1.05	V	—
Output high voltage	VOH	—	—	$XCOREVDD_{-Typ}/2 + \lvert V_{OD}\rvert_{-max}/2$	mV	1
Output low voltage	VOL	$XCOREVDD_{-Typ}/2 - \lvert V_{OD}\rvert_{-max}/2$	—	—	mV	1
Output ringing	V_{RING}	—	—	10	%	—
Output differential voltage[2, 3, 5]	$\lvert V_{OD}\rvert$	323	500	725	mV	Equalization setting: 1.0x
		296	459	665		Equalization setting: 1.09x
		269	417	604		Equalization setting: 1.2x
		243	376	545		Equalization setting: 1.33x
		215	333	483		Equalization setting: 1.5x
		189	292	424		Equalization setting: 1.71x
		162	250	362		Equalization setting: 2.0x
Output offset voltage	V_{OS}	425	500	575	mV	1, 4
Output impedance (single-ended)	R_O	40	—	60	Ω	—
Mismatch in a pair	ΔR_O	—	—	10	%	—
Change in V_{OD} between “0” and “1”	$\Delta \lvert V_{OD}\rvert$	—	—	25	mV	—
Change in V_{OS} between “0” and “1”	ΔV_{OS}	—	—	25	mV	—
Output current on short to GND	I_{SA}, I_{SB}	—	—	40	mA	—

Note:

1. This will not align to DC-coupled SGMII. $XCOREVDD_{-Typ}$=1.0V.
2. $\lvert V_{OD}\rvert = \lvert V_{TXn} - V_{\overline{TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX-DIFFp-p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the table assumes the following transmit equalization setting in the TXEQA (for SerDes lane A) or TXEQE (for SerDes lane E) bit field of MPC8315E’s SerDes Control Register 0:
   - The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. V_{OS} is also referred to as output common mode voltage.
5. The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $XCOREVDD_{-Typ}$=1.0V, no common mode offset variation (V_{OS} = 500 mV), SerDes transmitter is terminated with 100-Ω differential load between TX[n] and $\overline{TX}$[n].

Table 38. SGMII Receive AC Timing Specifications

At recommended operating conditions with XCOREVDD = 1.0V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal Jitter Tolerance	JSIN	0.1	—	—	UI p-p	1
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1
Bit Error Ratio	BER	—	—	10^{-12}		—
Unit Interval	UI	799.92	800	800.08	ps	2
AC Coupling Capacitor	C_{TX}	5	—	200	nF	3

Note:

1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It's recommended to be placed near the device transmitter outputs.
4. Refer to RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications.

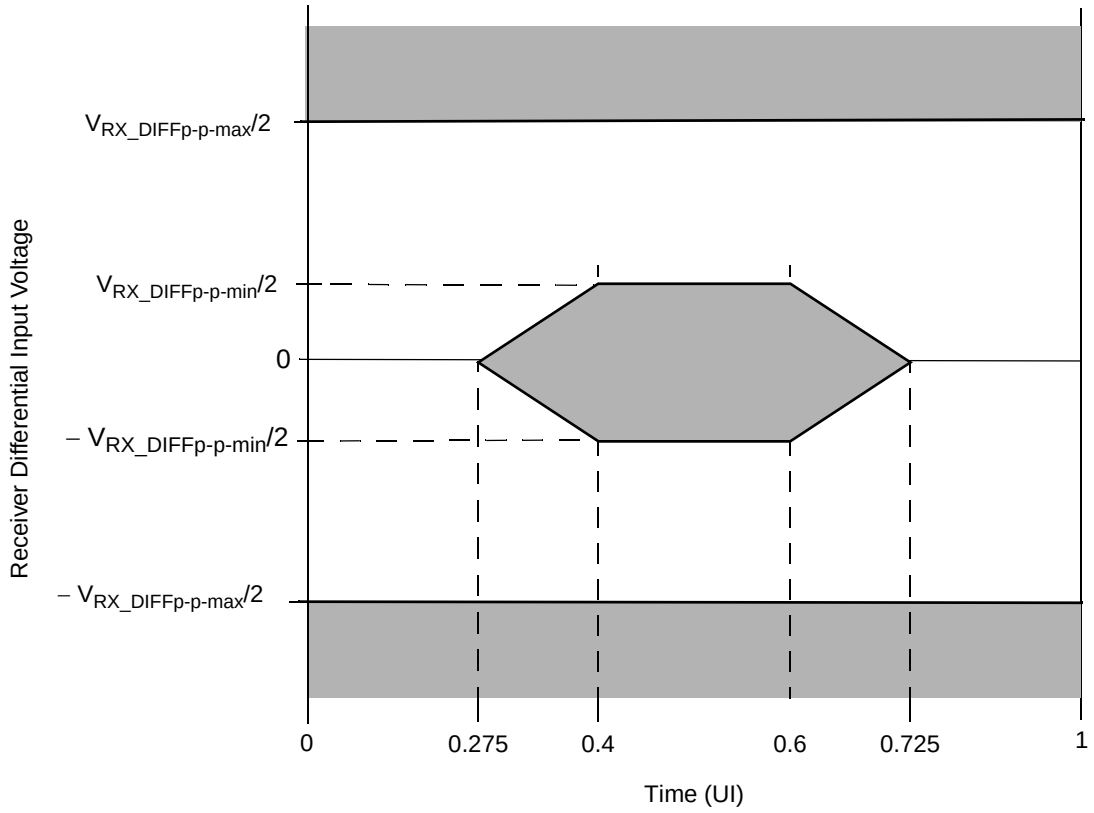

Figure 20. SGMII Receiver Input Compliance Mask

Table 44. Local Bus General Timing Parameters (continued)

Parameter	Symbol [1]	Min	Max	Unit	Note
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD	t_{LBKHOZ}	—	4	ns	8
LALE output rise to LCLK negative edge	$t_{LALEHOV}$	—	3.0	ns	

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from NVDD/2 of the rising/falling edge of LCLK0 to 0.4 × NVDD of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.
8. For active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This figure provides the AC test load for the local bus.

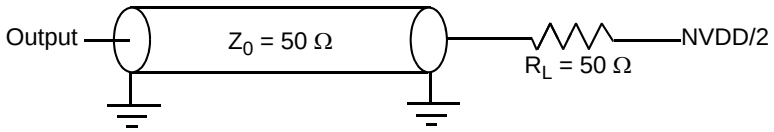

Figure 24. Local Bus AC Test Load

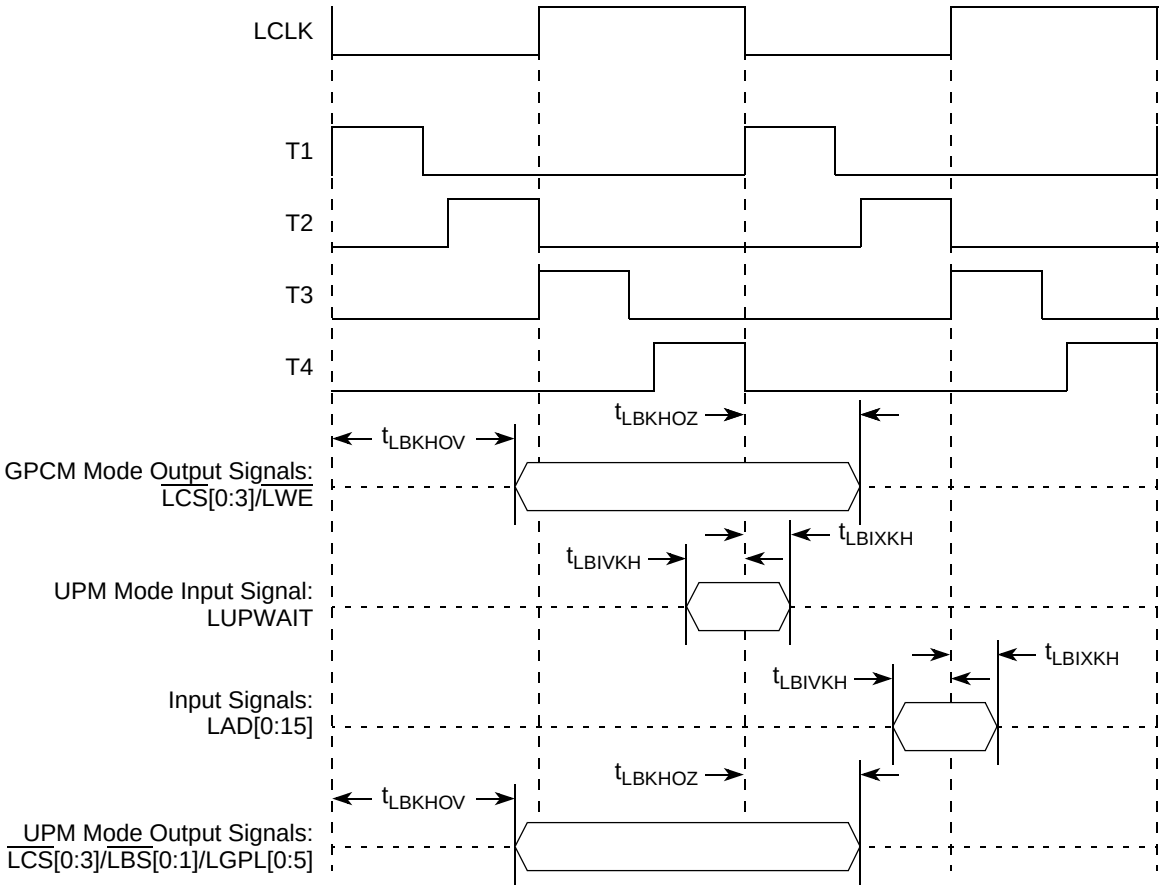

Figure 27. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

12 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface.

12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface.

Table 45. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

This figure shows the PCI input AC timing conditions.

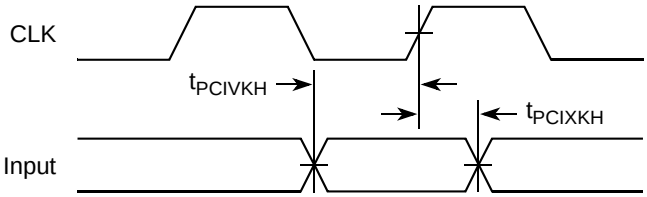

Figure 36. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

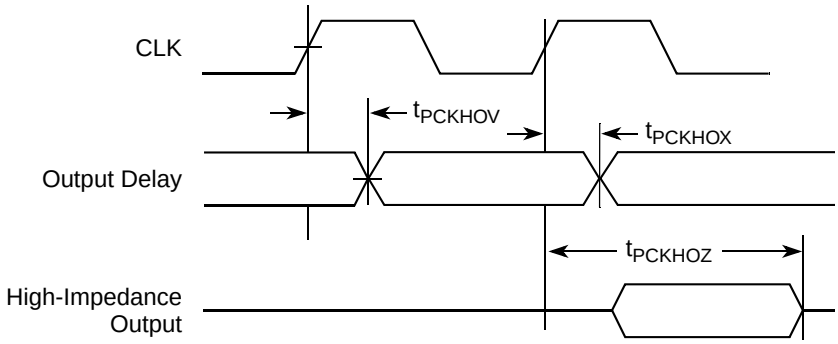

Figure 37. PCI Output AC Timing Measurement Condition

15 High-Speed Serial Interfaces (HSSI)

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

15.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 38 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (TXn and $\overline{\text{TXn}}$) or a receiver input (RXn and $\overline{\text{RXn}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals TXn, $\overline{\text{TXn}}$, RXn and $\overline{\text{RXn}}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's Single-Ended Swing.
2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

between 100 mV and 400 mV. Figure 40 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

— For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to XCOREVSS. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (XCOREVSS). Figure 41 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- **Single-ended Mode**
  — The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400mV and 800mV peak-peak (from Vmin to Vmax) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  — The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.
  — To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

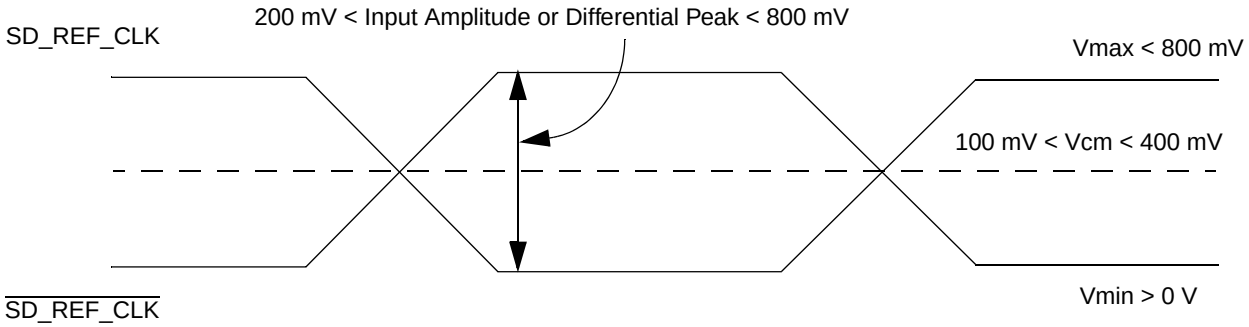

Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

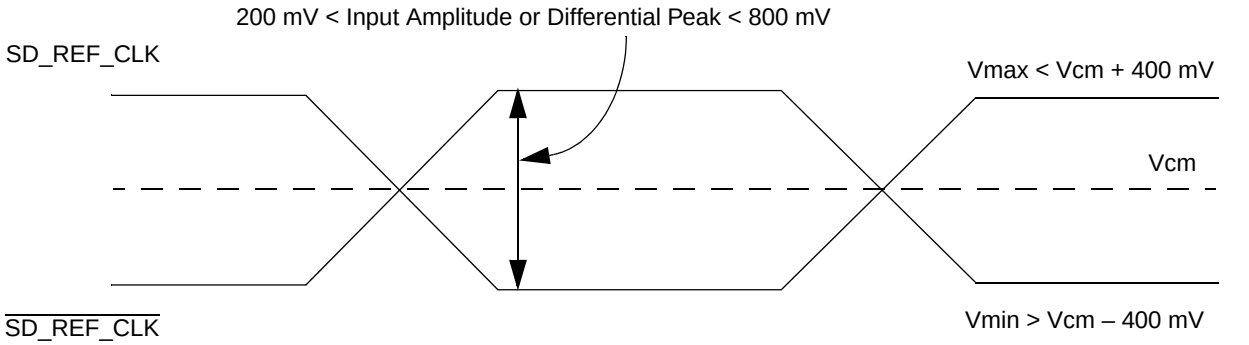

Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)

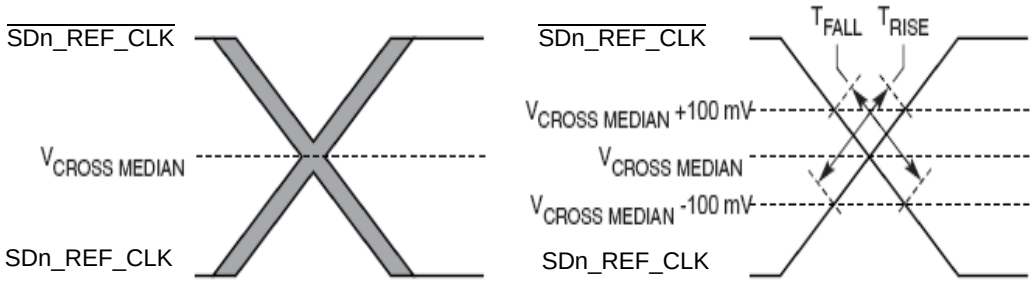

Figure 48. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- Section 9.5.2, “AC Requirements for SGMII SD_REF_CLK and SD_REF_CLK”
- Section 16.2, “AC Requirements for PCI Express SerDes Clocks”

15.2.4.1 Spread Spectrum Clock

SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

15.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane’s transmitter and receiver.

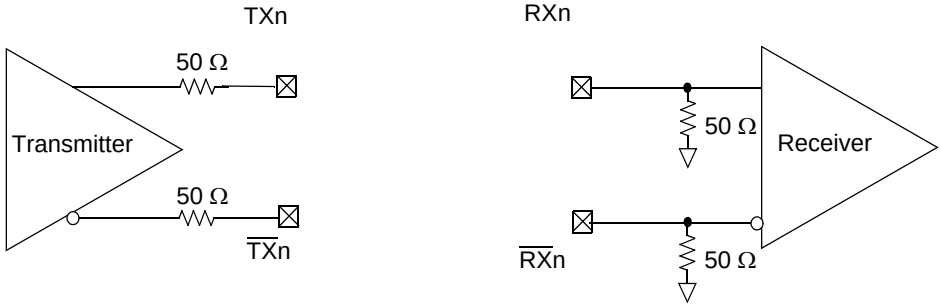

Figure 49. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express or SGMII) in this document based on the application usage:

- Section 9.5, “SGMII Interface Electrical Characteristics”
- Section 16, “PCI Express”

Note that external AC Coupling capacitor is required for the above two serial transmission protocols with the capacitor value defined in specification of each protocol section.

16.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 51 is specified using the passive compliance/test measurement load (see Figure 52) in place of any real PCI Express RX component. In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 52) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 51) expected at the input receiver based on an adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 Ω probes—see Figure 52). Note that the series capacitors, $C_{PEACCTX}$, are optional for the return loss measurement.

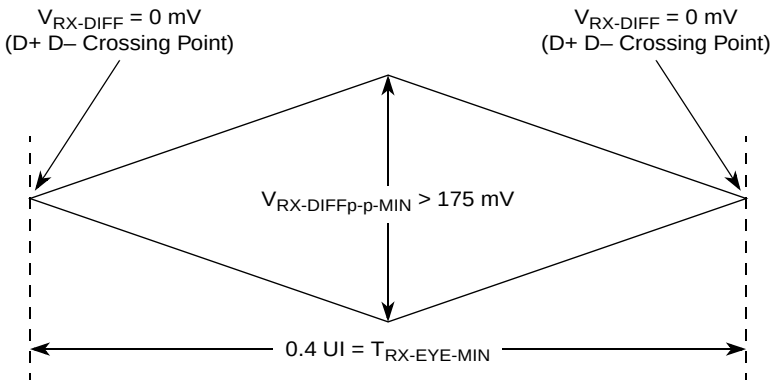

Figure 51. Minimum Receiver Eye Timing and Voltage Compliance Specification

16.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 52.

Table 61. Timers Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit

Note:
1. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers input are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure provides the AC test load for the Timers.

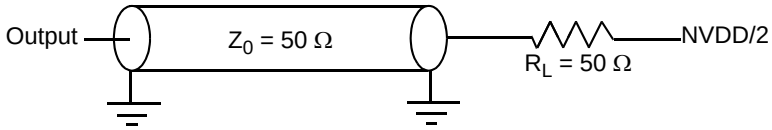

Figure 54. Timers AC Test Load

19 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8315E.

19.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO.

Table 62. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le$ NVDD	—	± 5	μA

19.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 63. GPIO Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Note:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
Local Bus Controller Interface				
LAD0	AB28	I/O	$NVDD3_{OFF}$	11
LAD1	AB27	I/O	$NVDD3_{OFF}$	11
LAD2	AC28	I/O	$NVDD3_{OFF}$	11
LAD3	AA24	I/O	$NVDD3_{OFF}$	11
LAD4	AC27	I/O	$NVDD3_{OFF}$	11
LAD5	AD28	I/O	$NVDD3_{OFF}$	11
LAD6	AB25	I/O	$NVDD3_{OFF}$	11
LAD7	AC26	I/O	$NVDD3_{OFF}$	11
LAD8	AD27	I/O	$NVDD3_{OFF}$	11
LAD9	AB24	I/O	$NVDD3_{OFF}$	11
LAD10	AE28	I/O	$NVDD3_{OFF}$	11
LAD11	AE27	I/O	$NVDD3_{OFF}$	11
LAD12	AE26	I/O	$NVDD3_{OFF}$	11
LAD13	AF28	I/O	$NVDD3_{OFF}$	11
LAD14	AC24	I/O	$NVDD3_{OFF}$	11
LAD15	AD25	I/O	$NVDD3_{OFF}$	11
LA16	V24	O	$NVDD3_{OFF}$	11
LA17	V25	O	$NVDD3_{OFF}$	11
LA18	W26	O	$NVDD3_{OFF}$	11
LA19	W28	O	$NVDD3_{OFF}$	11
LA20	U24	O	$NVDD3_{OFF}$	11
LA21	W24	O	$NVDD3_{OFF}$	11
LA22	Y28	O	$NVDD3_{OFF}$	11
LA23	AH23	O	$NVDD3_{OFF}$	11
LA24	AH24	O	$NVDD3_{OFF}$	11
LA25	AG23	O	$NVDD3_{OFF}$	11
$\overline{\text{LCS}}$[0]	AD22	O	$NVDD3_{OFF}$	12
$\overline{\text{LCS}}$[1]	AF25	O	$NVDD3_{OFF}$	12
$\overline{\text{LCS}}$[2]	AG24	O	$NVDD3_{OFF}$	12
$\overline{\text{LCS}}$[3]	AF24	O	$NVDD3_{OFF}$	12
$\overline{\text{LWE}}$[0] /$\overline{\text{LFWE}}$/$\overline{\text{LBS}}$	AE23	O	$NVDD3_{OFF}$	12
$\overline{\text{LWE}}$[1]	AG26	O	$NVDD3_{OFF}$	12
LBCTL	AH26	O	$NVDD3_{OFF}$	12
LALE	AF26	O	$NVDD3_{OFF}$	11
LGPL0/LFCLE	Y27	O	$NVDD3_{OFF}$	—

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_REQ0	E18	I/O	$NVDD2_{OFF}$	—
PCI_REQ1/CPCI_HS_ES	C18	I	$NVDD2_{OFF}$	—
PCI_REQ2	E17	I	$NVDD2_{OFF}$	—
PCI_GNT0	B20	I/O	$NVDD2_{OFF}$	—
PCI_GNT1/CPCI_HS_LED	D17	O	$NVDD2_{OFF}$	—
PCI_GNT2/CPCI_HS_ENUM	E15	O	$NVDD2_{OFF}$	—
M66EN	L24	I	$NVDD2_{OFF}$	—
PCI_CLK0	E23	O	$NVDD2_{OFF}$	—
PCI_CLK1	F24	O	$NVDD2_{OFF}$	—
PCI_CLK2	E25	O	$NVDD2_{OFF}$	—
PCI_PME	B23	I/O	$NVDD2_{OFF}$	2
ETSEC1/_USBULPI				
GPIO_24/TSEC1_COL/USBDR_TXDRXD0	J1	I/O	$LVDD1_{OFF}$	—
GPIO_25/TSEC1_CRS/USBDR_TXDRXD1	H1	I/O	$LVDD1_{OFF}$	—
TSEC1_GTX_CLK/USBDR_TXDRXD2	K5	I/O	$LVDD1_{OFF}$	3
TSEC1_RX_CLK/USBDR_TXDRXD3	J4	I/O	$LVDD1_{OFF}$	—
TSCE1_RX_DV/USBDR_TXDRXD4	J2	I/O	$LVDD1_{OFF}$	—
TSEC1_RXD[3]/USBDR_TXDRXD5	G1	I/O	$LVDD1_{OFF}$	—
TSEC1_RXD[2]/USBDR_TXDRXD6	H3	I/O	$LVDD1_{OFF}$	—
TSEC1_RXD[1]/USBDR_TXDRXD7/TSEC_TMR_CLK	J5	I/O	$LVDD1_{OFF}$	—
TSEC1_RXD[0]/USBDR_NXT/TSEC_TMR_TRIG1	H2	I	$LVDD1_{OFF}$	—
TSEC1_RX_ER/USBDR_DIR/TSEC_TMR_TRIG2	H5	I	$LVDD1_{OFF}$	—
TSEC1_TX_CLK/USBDR_CLK	G2	I	$LVDD1_{OFF}$	—
GPIO_28/TSEC1_TXD[3]/TSEC_TMR_GCLK	F3	I/O	$LVDD1_{OFF}$	—
GPIO_29/TSEC1_TXD[2]/TSEC_TMR_PP1	F2	I/O	$LVDD1_{OFF}$	—
GPIO_30/TSEC1_TXD[1]/TSEC_TMR_PP2	F1	I/O	$LVDD1_{OFF}$	—
TSEC1_TXD[0]/USBDR_STP/ TSEC_TMR_PP3	G4	O	$LVDD1_{OFF}$	12
GPIO_31/TSEC1_TX_EN/TSEC_TMR_ALARM1	F4	I/O	$LVDD1_{OFF}$	—
TSEC1_TX_ER/TSEC_TMR_ALARM2	G5	O	$LVDD1_{OFF}$	—
TSEC_GTX_CLK125	D1	I	$NVDD1_{ON}$	—
TSEC_MDC/LB_POR_CFG_BOOT_ECC	E3	I/O	$NVDD1_{ON}$	9
TSEC_MDIO	E2	I/O	$NVDD1_{ON}$	

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
USB_DP	A11	I/O	USB_VDDA	—
USB_DM	A12	I/O	USB_VDDA	—
USB_VBUS	C12	I	—	—
USB_TPA	A14	O	—	—
USB_RBIAS	D14	I	—	8
USB_PLL_PWR3	A13	I	—	—
USB_PLL_GND0 & USB_PLL_GND1	D13	I	—	—
USB_PLL_PWR1	B13	I	—	—
USB_VSSA_BIAS	E14	I	—	—
USB_VDDA_BIAS	C14	I	—	—
USB_VSSA	E13	I	—	—
USB_VDDA	E12	I	—	—
GPIO				
GPIO_0/$\overline{\text{DMA\_DREQ1}}$/$\overline{\text{GTM1\_TOUT1}}$	C5	I/O	$NVDD1_{ON}$	—
GPIO_1/$\overline{\text{DMA\_DACK1}}$/GTM1_TIN2/GTM2_TIN1	A4	I/O	$NVDD1_{ON}$	—
GPIO_2/$\overline{\text{DMA\_DONE1}}$/$\overline{\text{GTM1\_TGATE2}}$/$\overline{\text{GTM2\_TGATE1}}$	K3	I/O	$NVDD4_{OFF}$	—
GPIO_3/GTM1_TIN3/GTM2_TIN4	K1	I/O	$NVDD4_{OFF}$	—
GPIO_4/$\overline{\text{GTM1\_TGATE3}}$/$\overline{\text{GTM2\_TGATE4}}$	K2	I/O	$NVDD4_{OFF}$	—
GPIO_5/$\overline{\text{GTM1\_TOUT3}}$/$\overline{\text{GTM2\_TOUT1}}$	L5	I/O	$NVDD4_{OFF}$	—
GPIO_6/GTM1_TIN4/GTM2_TIN3	L3	I/O	$NVDD4_{OFF}$	—
GPIO_7/$\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$	L1	I/O	$NVDD4_{OFF}$	—
GPIO_8/USBDR_DRIVE_VBUS/GTM1_TIN1/GTM2_TIN2	M1	I/O	$NVDD4_{OFF}$	—
GPIO_9/USBDR_PWRFAULT/$\overline{\text{GTM1\_TGATE1}}$/$\overline{\text{GTM2\_TGATE2}}$	M2	I/O	$NVDD4_{OFF}$	—
GPIO_10/USBDR_PCTL0/$\overline{\text{GTM1\_TOUT2}}$/$\overline{\text{GTM2\_TOUT1}}$	M5	I/O	$NVDD4_{OFF}$	—
GPIO_11/USBDR_PCTL1/$\overline{\text{GTM1\_TOUT4}}$/$\overline{\text{GTM2\_TOUT3}}$	M4	I/O	$NVDD4_{OFF}$	—
SPI				
SPIMOSI/GPIO_15	W3	I/O	$NVDD1_{OFF}$	—
SPIMISO/GPIO_16	W4	I/O	$NVDD1_{OFF}$	—
SPICLK	Y1	I/O	$NVDD1_{OFF}$	—
SPISEL/GPIO_17	W2	I/O	$NVDD1_{OFF}$	—

Table 77. Suggested PLL Configurations

Conf. No.	SPMF	Core\PLL	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)
6	0010	0000101	66.67	133.33	333.33
7	0101	0000110	25	125	375
8	0100	0000110	33.33	133.33	400
9	0010	0000110	66.67	133.33	400

25 Thermal

This section describes the thermal specifications of the MPC8315E.

25.1 Thermal Characteristics

This table provides the package thermal characteristics for the 620 29 × 29 mm TEPBGA II.

Table 78. Package Thermal Characteristics for TEPBGA II

Characteristic	Board type	Symbol	Value	Unit	Note
Junction to ambient natural convection	Single layer board (1s)	$R_{\theta JA}$	23	°C/W	1, 2
Junction to ambient natural convection	Four layer board (2s2p)	$R_{\theta JA}$	16	°C/W	1, 2, 3
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	18	°C/W	1, 3
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	13	°C/W	1, 3
Junction to board	—	$R_{\theta JB}$	8	°C/W	4
Junction to case	—	$R_{\theta JC}$	6	°C/W	5
Junction to package top	Natural convection	Ψ_{JT}	6	°C/W	6

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

25.2 Thermal Management Information

For the following sections, $P_D = (VDD \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers.

25.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity T_J - T_A) are possible.

25.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction to ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JB}$ = junction to board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

Table 79. Heat Sinks and Junction-to-Case Thermal Resistance of MPC8315E TEPBGA II

Heat Sink Assuming Thermal Grease	Air Flow	29 × 29 mm TEBGA II
		Junction-to-Ambient Thermal Resistance
AAVID 30 x 30 x 9.4 mm Pin Fin	Natural Convection	14.4
AAVID 30 x 30 x 9.4 mm Pin Fin	0.5 m/s	11.4
AAVID 30 x 30 x 9.4 mm Pin Fin	1 m/s	10.1
AAVID 30 x 30 x 9.4 mm Pin Fin	2 m/s	8.9
AAVID 35 x 31 x 23 mm Pin Fin	Natural Convection	12.3
AAVID 35 x 31 x 23 mm Pin Fin	0.5 m/s	9.3
AAVID 35 x 31 x 23 mm Pin Fin	1 m/s	8.5
AAVID 35 x 31 x 23 mm Pin Fin	2 m/s	7.9
AAVID 43 x 41 x 16.5 mm Pin Fin	Natural Convection	12.5
AAVID 43 x 41 x 16.5 mm Pin Fin	0.5 m/s	9.7
AAVID 43 x 41 x 16.5 mm Pin Fin	1 m/s	8.5
AAVID 43 x 41 x 16.5 mm Pin Fin	2 m/s	7.7
Wakefield, 53 x 53 x 25 mm Pin Fin	Natural Convection	10.9
Wakefield, 53 x 53 x 25 mm Pin Fin	0.5 m/s	8.5
Wakefield, 53 x 53 x 25 mm Pin Fin	1 m/s	7.5
Wakefield, 53 x 53 x 25 mm Pin Fin	2 m/s	7.1

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #12
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias. Note that the RC filter results in lower voltage level on AVDD. This does not imply that the DC specification can be relaxed.

This figure shows the PLL power supply filter circuit.

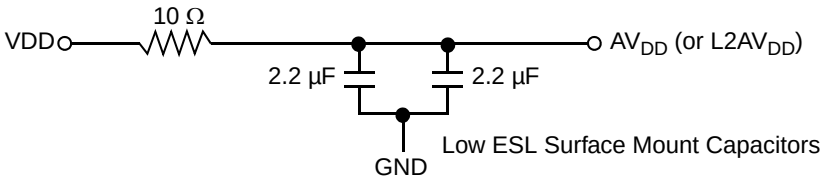

Figure 63. PLL Power Supply Filter Circuit

26.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8315E system, and the MPC8315E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each VDD, NVDD, GVDD, and LVDD pins of the device. These decoupling capacitors should receive their power from separate VDD, NVDD, GVDD, LVDD, and GND power planes in the PCB, utilizing thick and short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the VDD, NVDD, GVDD, and LVDD planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

26.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to NVDD, GVDD, or LVDD as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

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