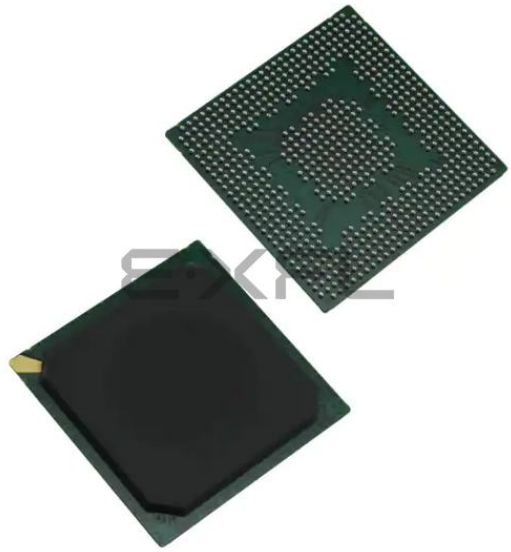

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8315vragda

1 Overview

The MPC8315E incorporates the e300c3 (MPC603e-based) core, which includes 16 Kbytes of L1 instruction and data caches, on-chip memory management units (MMUs), and floating-point support. In addition to the e300 core, the SoC platform includes features such as dual enhanced three-speed 10, 100, 1000 Mbps Ethernet controllers (eTSECs) with SGMII support, a 32- or 16-bit DDR1/DDR2 SDRAM memory controller, dual SATA 3 Gbps controllers (MPC8315E-specific), a security engine to accelerate control and data plane security protocols, and a high degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration. The MPC8315E also offers peripheral interfaces such as a 32-bit PCI interface with up to 66 MHz operation, 16-bit enhanced local bus interface with up to 66 MHz operation, TDM interface, and USB 2.0 with an on-chip USB 2.0 PHY.

The MPC8315E offers additional high-speed interconnect support with dual integrated SATA 3 Gbps interfaces and dual single-lane PCI Express interfaces. When not used for PCI Express, the SerDes interface may be configured to support SGMII. The MPC8315E security engine (SEC 3.3) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. This figure shows a block diagram of the MPC8315E.

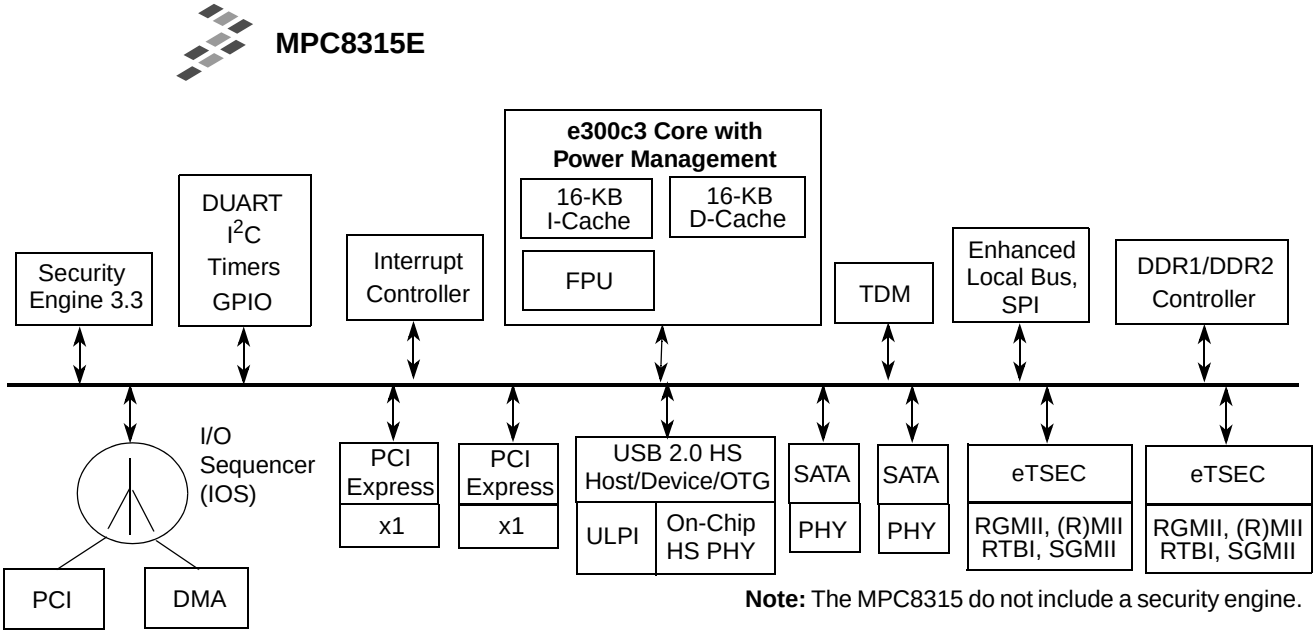


Figure 1. MPC8315E Block Diagram

2 MPC8315E Features

The following features are supported in the MPC8315E.

2.1 e300 Core

The e300 core has the following features:

- Operates at up to 400 MHz

using a simple handshake protocol. The three user programmable machines (UPMs) can be programmed to interface to synchronous devices or custom ASIC interfaces. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM or UPM controller. Both may exist in the same system. The local bus can operate at up to 66 MHz.

The system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

3 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8315E, which is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but they are included for complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

3.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings [1]

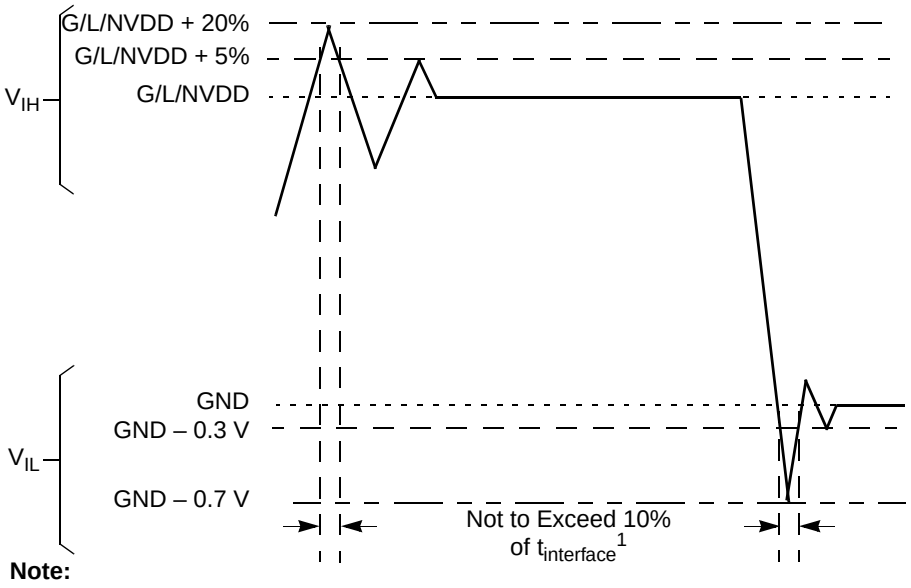
Characteristic		Symbol	Max Value	Unit	Note
Core supply voltage		VDD	–0.3 to 1.26	V	—
PLL supply voltage		AVDD	–0.3 to 1.26	V	—
DDR1 DRAM I/O supply voltage		GVDD	–0.3 to 2.7	V	—
DDR2 DRAM I/O supply voltage		GVDD	–0.3 to 1.9	V	—
PCI, local bus, DUART, system control and power management, I^2C, Ethernet management, 1588 timer and JTAG I/O voltage		NVDD	–0.3 to 3.6	V	7
USB, and eTSEC I/O voltage		LVDD	–0.3 to 2.75 or –0.3 to 3.6	V	6, 8
PHY voltage	USB PHY	USB_PLL_PWR1	–0.3 to 1.26	V	—
		USB_PLL_PWR3, USB_VDDA_BIAS, VDDA	–0.3 to 3.6	V	—
	SERDES PHY	XCOREVDD, XPADVDD, SDAVDD	–0.3 to 1.26	V	—
	SATA PHY	SATA_VDD, VDD1IO, VDD1ANA	–0.3 to 1.26	V	—
		VDD33PLL, VDD33ANA	–0.3 to 3.6	V	—

Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value[1]	Unit	Status in D3 Warm mode	Note

Note:
1. The NVDDx_ON are static power supplies and can be connected together.
2. The NVDDx_OFF are switchable power supplies and can be connected together.
3. Minimum Temperature is specified with T_A;maximum temperature is specified with T_J.
4. All Power rails must be connected and power applied to the MPC8315 even if the IP interfaces are not used.
5. All I/O pins should be interfaced with peripherals operating at same voltage level.
6. This voltage is the input to the filter discussed in Section 26.2, "PLL Power Supply Filtering" and not necessarily the voltage at the AVDD pin.
7. All 1V power supplies should be derived from the same source.

This figure shows the undershoot and overshoot voltages at the interfaces of the MPC8315E.



Note:
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for GVDD/NVDD/LVDD

3.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	NVDD = 3.3 V
PCI signals	25	
DDR signal[1]	18	GVDD = 2.5 V
DDR2 signal 1	18	GVDD = 1.8 V

Table 5. MPC8315E Power Dissipation (continued)

Interface	Frequency	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	NV_{DD} (3.3 V)	LVDD1_OFF/ LVDD2_ON (3.3V)	LVDD2 _ON (3.3V)	VDD33PLL, VDD33ANA (3.3V)	SATA_VDD, VDD1IO, VDD1ANA (1.0V)	XCOREVDD, XPADVDD, SDAVDD (1.0V)	Unit
DDR 2 Rs = 22Ω Rt = 75Ω	266MHz, 32 bits	0.246	—	—	—	—	—	—	—	W
	200MHz, 32bits	0.225	—	—	—	—	—	—	—	W
PCI I/O load = 50pF	33 MHz	—	—	0.120	—	—	—	—	—	W
	66 MHz	—	—	0.249	—	—	—	—	—	W
Local bus I/O load = 20pF	66 MHz	—	—	—	—	0.056	—	—	—	W
	50 MHz	—	—	—	—	0.040	—	—	—	W
eTSEC I/O load = 20pF Multiple by number of interface used	MII, 25MHz	—	—	—	0.008	—	—	—	—	W
	RGMII, 125MHz (3.3V)	—	—	—	0.078	—	—	—	—	W
	RGMII, 125MHz (2.5V)	—	—	—	0.044	—	—	—	—	W
USBDR Controller (ULPI mode) load =20pF	60 MHz	—	—	—	0.078	—	—	—	—	W
USBDR+ Internal PHY (UTMI mode)	480 MHz	—	—	—	0.274	—	—	—	—	W
PCI Express two x1lane	2.5 GHz	—	—	—	—	—	—	—	0.190	W
SATA two ports	3.0 GHz	—	—	—	—	—	0.021	0.206	—	W
Other I/O	—	—	—	0.015	—	—	—	—	—	W

5 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8315E.

Table 11. DDR2 SDRAM DC Electrical Characteristics for GVDD(typ) = 1.8 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Note

Note:
1. GVDD is expected to be within 50 mV of the DRAM GVDD at all times.
2. MVREF is expected to be equal to 0.5 × GVDD, and to track GVDD DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GVDD.

This table provides the DDR2 capacitance when GVDD(typ) = 1.8 V.

Table 12. DDR2 SDRAM Capacitance for GVDD(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GVDD = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8315E when GVDD(typ) = 2.5 V.

Table 13. DDR SDRAM DC Electrical Characteristics for GVDD(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GVDD	2.3	2.7	V	1
I/O reference voltage	MVREF	0.49 × GVDD	0.51 × GVDD	V	2
I/O termination voltage	V_{TT}	MVREF – 0.04	MVREF + 0.04	V	3
Input high voltage	V_{IH}	MVREF + 0.15	GVDD + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF – 0.15	V	—
Output leakage current	I_{OZ}	–9.9	–9.9	μA	4
Output high current (V_{OUT} = 1.95 V, GVDD = 2.3V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Note:
1. GVDD is expected to be within 50 mV of the DRAM GVDD at all times.
2. MVREF is expected to be equal to 0.5 × GVDD, and to track GVDD DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GVDD.

This table provides the DDR capacitance when GVDD(typ) = 2.5 V.

Table 14. DDR SDRAM Capacitance for GVDD(typ) = 2.5 V Interface

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ,DQS	C_{IO}	6	8	pF	1

7.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions

Parameter	Symbol [1]	Min	Max	Unit	Note
MCK[n] cycle time at MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	7.5	10	ns	2
ADDR/CMD output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHAS}	 2.9 3.5	 — —	ns	3
ADDR/CMD output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHAX}	 3.15 4.20	 — —	ns	3
$\overline{\text{MCS}}$[n] output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHCS}	 3.15 4.20	 — —	ns	3
$\overline{\text{MCS}}$[n] output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHCX}	 3.15 4.20	 — —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ//MDM output setup with respect to MDQS 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 900 1000	 — —	ps	5
MDQ//MDM output hold with respect to MDQS 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 1100 1200	 — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Table 29. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions (see Table 2)

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Clock cycle duration [3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12} [6]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Note:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the RTBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is LVDD/2.
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention. GTX_CLK supply voltage is fixed at 3.3V inside the chip. If PHY supplies a 2.5 V Clock signal on this input, set TSCOMOBI bit of System I/O configuration register (SICRH) as 1. See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
7. The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm

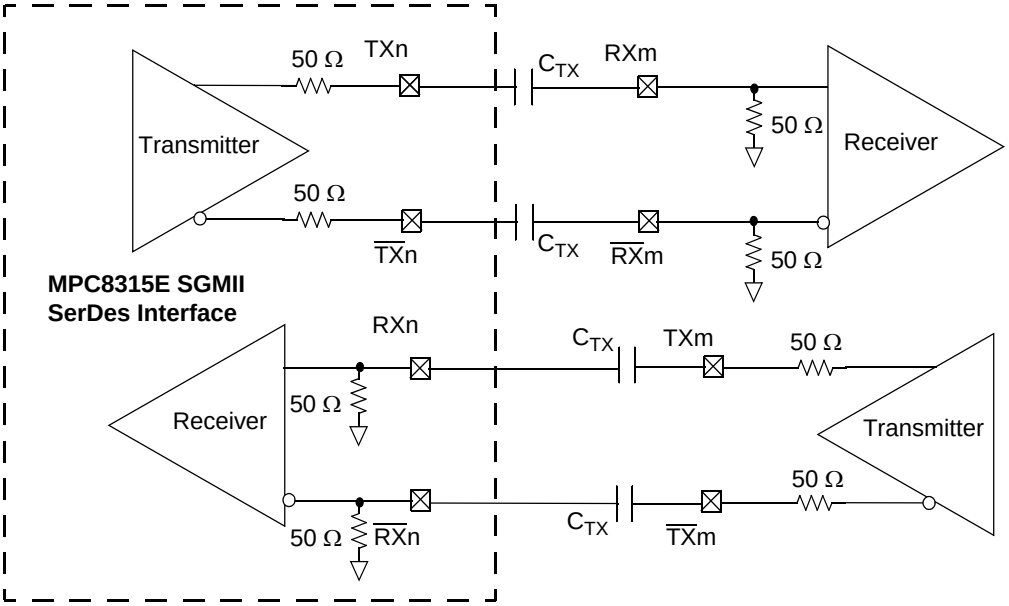


Figure 18. 4-Wire AC-Coupled SGMII Serial Link Connection Example

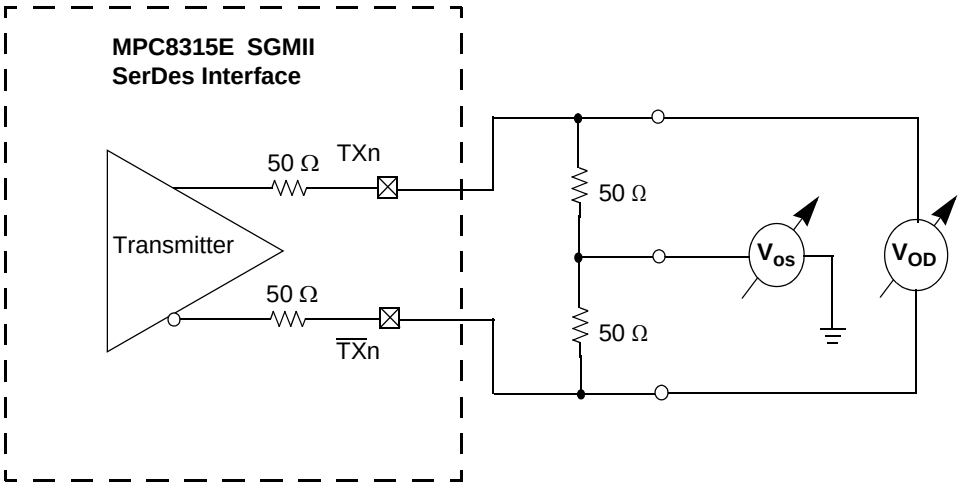


Figure 19. SGMII Transmitter DC Measurement Circuit

Table 36. SGMII DC Receiver Electrical Characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		XCOREVDD	0.95	1.0	1.05	V	—
DC Input voltage range		—	N/A			—	1
Input differential voltage	EQ = 0	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2, 4
	EQ = 1		175	—			
Loss of signal threshold	EQ = 0	VLOS	30	—	100	mV	3, 4
	EQ = 1		65	—	175		

Table 38. SGMII Receive AC Timing Specifications

At recommended operating conditions with XCOREVDD = 1.0V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal Jitter Tolerance	JSIN	0.1	—	—	UI p-p	1
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1
Bit Error Ratio	BER	—	—	10^{-12}		—
Unit Interval	UI	799.92	800	800.08	ps	2
AC Coupling Capacitor	C_{TX}	5	—	200	nF	3

Note:

1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It's recommended to be placed near the device transmitter outputs.
4. Refer to RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications.

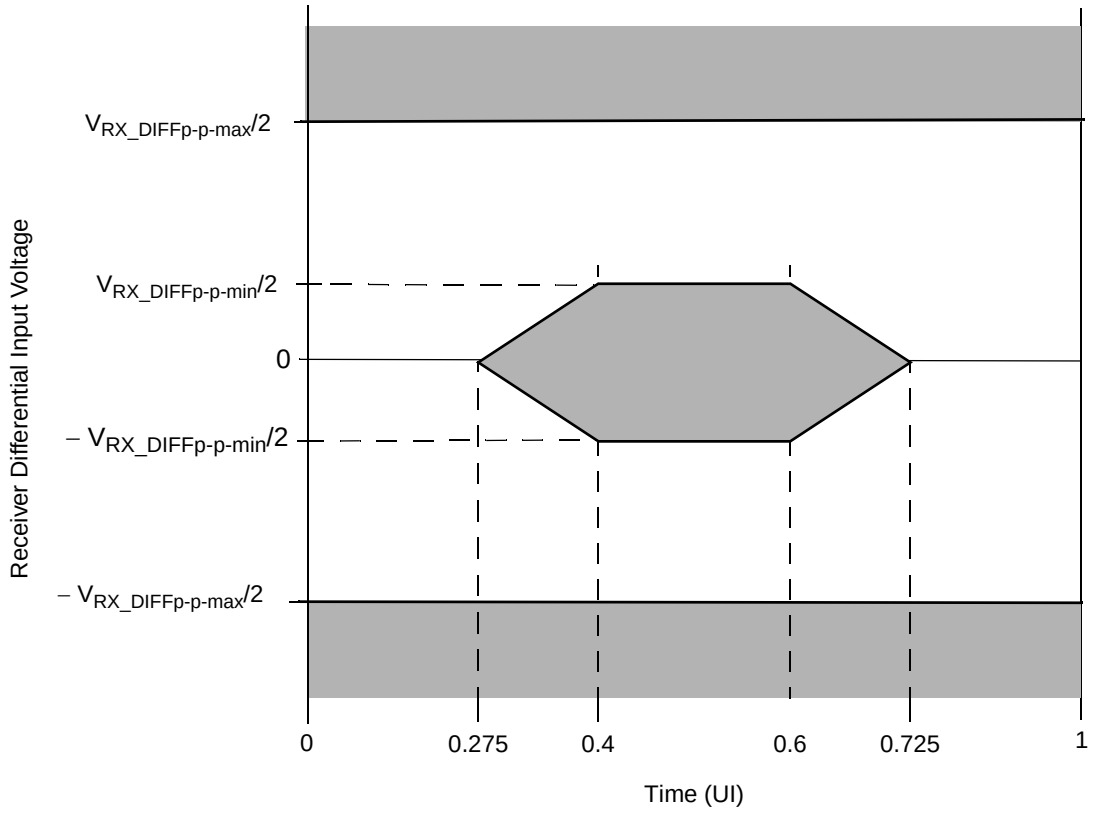


Figure 20. SGMII Receiver Input Compliance Mask

Table 40. USB General Timing Parameters (continued)

Parameter	Symbol [1]	Min	Max	Unit	Note
USB clock to output valid—all outputs	t_{USKHOV}	—	9	ns	1
Output hold from USB clock—all outputs	t_{USKHOX}	1	—	ns	1

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the us clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from NVDD/2 of the rising edge of USB clock to 0.4 × NVDD of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 22 and Figure 23 provide the AC test load and signals for the USB, respectively.

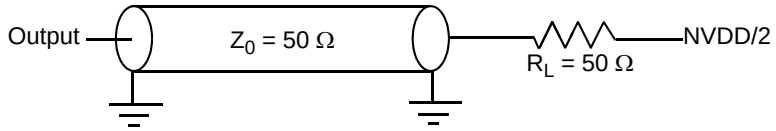


Figure 22. USB AC Test Load

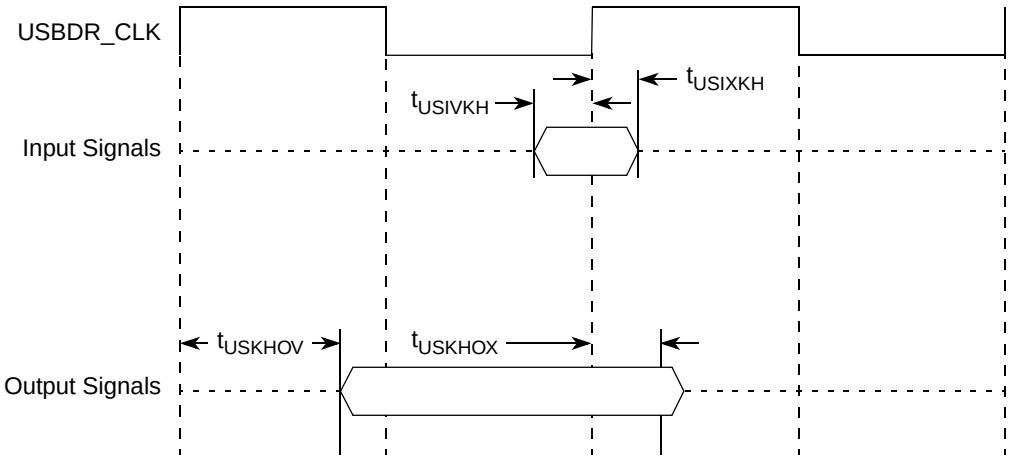


Figure 23. USB Signals

10.2 On-Chip USB PHY

This section provides the AC and DC electrical specifications for the USB PHY interface of the MPC8315E.

For details refer to Tables 7-7 through 7-10, and Table 7-14 in the *USB 2.0 Specifications document*, and the pull-up/down resistors ECN updates, all available at www.usb.org.

This table provides the USB clock input (USB_CLK_IN) DC timing specifications.

This figure shows the PCI input AC timing conditions.

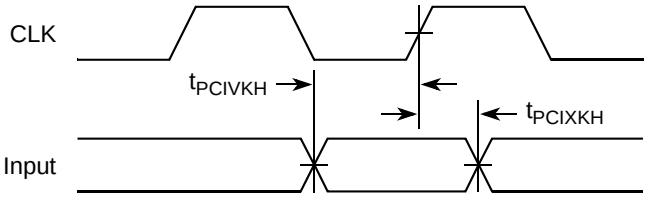


Figure 36. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

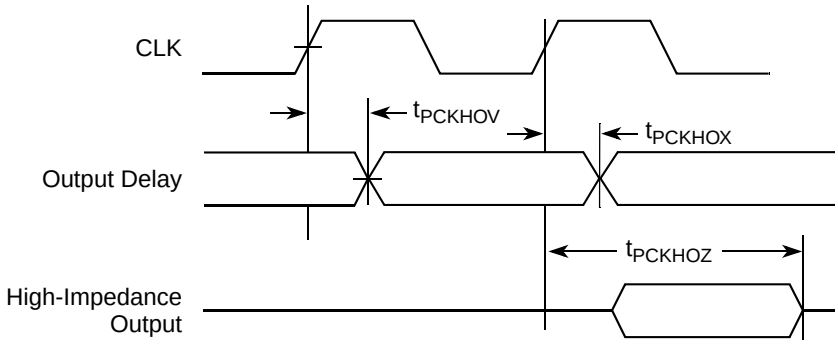


Figure 37. PCI Output AC Timing Measurement Condition

15 High-Speed Serial Interfaces (HSSI)

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

15.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 38 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (TXn and $\overline{\text{TXn}}$) or a receiver input (RXn and $\overline{\text{RXn}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals TXn, $\overline{\text{TXn}}$, RXn and $\overline{\text{RXn}}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's Single-Ended Swing.
2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

between 100 mV and 400 mV. Figure 40 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

— For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to XCOREVSS. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (XCOREVSS). Figure 41 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- **Single-ended Mode**
  — The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400mV and 800mV peak-peak (from Vmin to Vmax) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  — The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.
  — To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

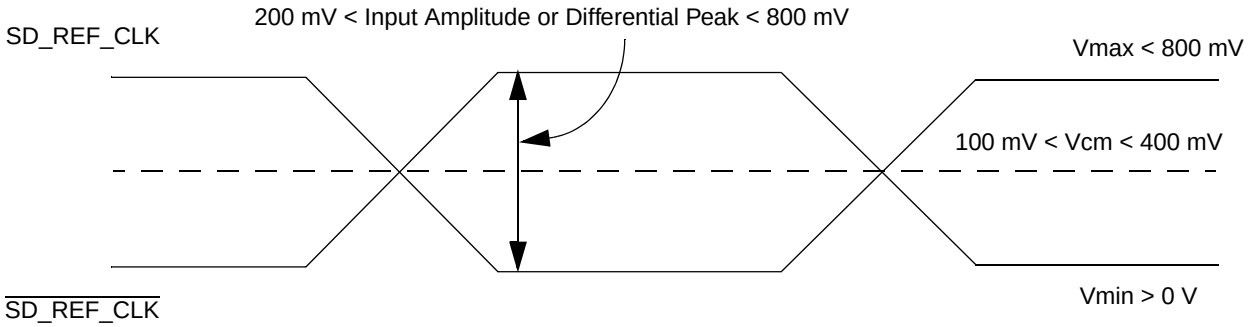


Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

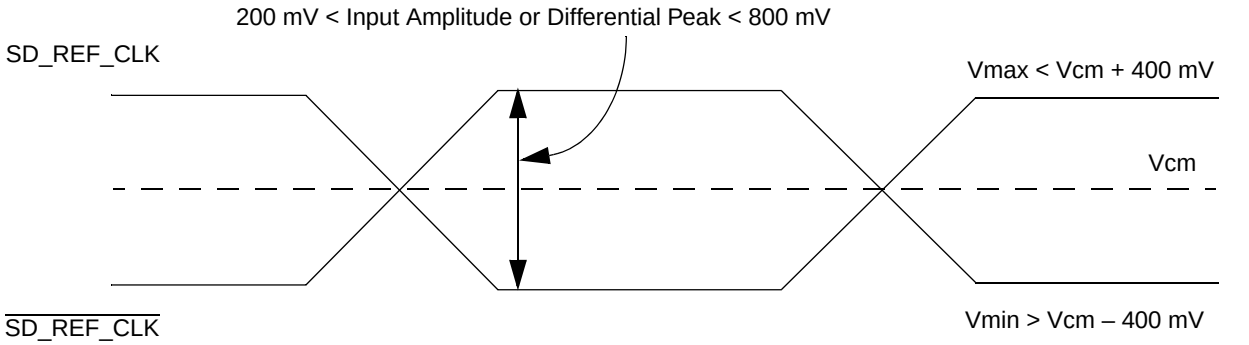


Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)

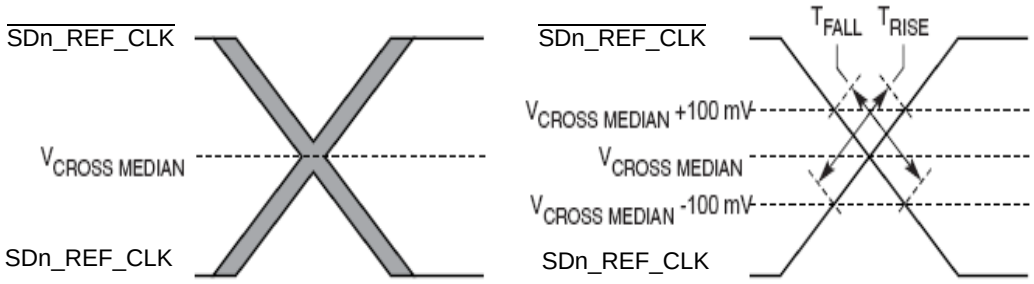


Figure 48. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- Section 9.5.2, “AC Requirements for SGMII SD_REF_CLK and SD_REF_CLK”
- Section 16.2, “AC Requirements for PCI Express SerDes Clocks”

15.2.4.1 Spread Spectrum Clock

SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

15.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane’s transmitter and receiver.

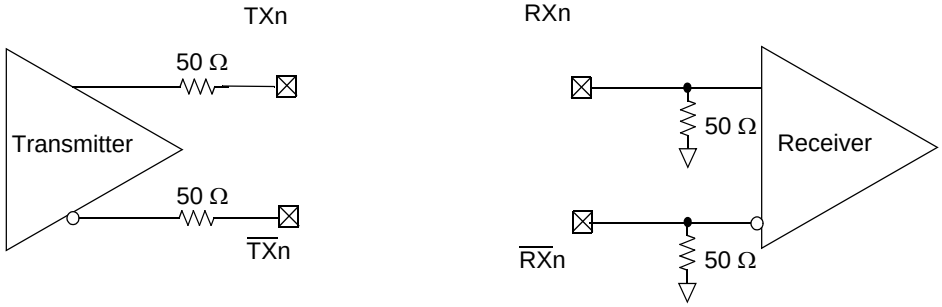


Figure 49. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express or SGMII) in this document based on the application usage:

- Section 9.5, “SGMII Interface Electrical Characteristics”
- Section 16, “PCI Express”

Note that external AC Coupling capacitor is required for the above two serial transmission protocols with the capacitor value defined in specification of each protocol section.

Table 54. Differential Transmitter (TX) Output Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Unit	Note
Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	$T_{TX-IDLE-SET-TO-IDLE}$	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.	—	—	20	UI	—
Maximum time to transition to valid TX specifications after leaving an electrical idle condition	$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle	—	—	20	UI	—
Differential return loss	$RL_{TX-DIFF}$	Measured over 50 MHz to 1.25 GHz.	12	—	—	dB	4
Common mode return loss	RL_{TX-CM}	Measured over 50 MHz to 1.25 GHz.	6	—	—	dB	4
DC differential TX impedance	$Z_{TX-DIFF-DC}$	TX DC Differential mode Low Impedance	80	100	120	Ω	—
Transmitter DC impedance	Z_{TX-DC}	Required TX D+ as well as D- DC Impedance during all states	40	—	—	Ω	—
Lane-to-Lane output skew	$L_{TX-SKEW}$	Static skew between any two Transmitter Lanes within a single Link	—	—	500 + 2 UI	ps	—
AC coupling capacitor	C_{TX}	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.	75	—	200	nF	8
Crosslink random timeout	$T_{crosslink}$	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port.	0	—	1	ms	7

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 52 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 50.)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 52). Note that the series capacitors, C_{TX}, is optional for the return loss measurement.
5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 52 for both V_{TX-D+} and V_{TX-D-}.
6. See Section 4.3.1.8 of the *PCI Express Base Specifications*, Rev 1.0a.
7. See Section 4.2.6.3 of the *PCI Express Base Specifications*, Rev 1.0a.
8. MPC8315E SerDes transmitter does not have C_{TX} built-in. An external AC Coupling capacitor is required

Table 56. Reference Clock Input Requirements (continued)

Parameter	Symbol	Conditions	Min	Typical	Max	Unit	Note
Total reference clock jitter, phase noise integration from 100 Hz to 3 MHz	t_{CLK_PJ}	peak to peak jitter at refClk input	—	—	100	ps	—

Note:
1. Only 50/75/100/125/150 MHz have been tested, other in between values will not work correctly with the rest of the system.

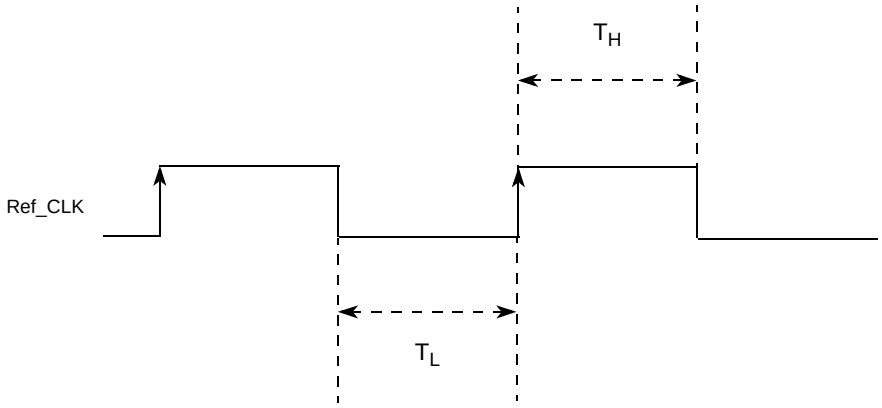


Figure 53. Reference Clock Timing Waveform

17.2 SATA AC Electrical Characteristics

This table provides the general AC parameters for the SATA interface.

Table 57. SATA AC Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Note
Channel Speed 1.5G 3.0G	t_{CH_SPEED}	—	 1.5 3.0	—	Gbps	—
Unit Interval 1.5G 3.0G	T_{UI}	—	 666.4333 333.3333	—	ps	—

21.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the SPI.

Table 66. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

21.2 SPI AC Timing Specifications

This table and provide the SPI input and output AC timing specifications.

Table 67. SPI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
SPI outputs valid—master mode (internal clock) delay	t_{NIKHOV}	—	6	ns
SPI outputs hold—master mode (internal clock) delay	t_{NIKHOX}	0.5		ns
SPI outputs valid—slave mode (external clock) delay	t_{NEKHOV}	—	8.5	ns
SPI outputs hold—slave mode (external clock) delay	t_{NEKHOX}	2	—	ns
SPI inputs—master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—master mode (internal clock)input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Note:

1. Output specifications are measured from the 50% level of the rising edge of SPICLK to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

This figure provides the AC test load for the SPI.

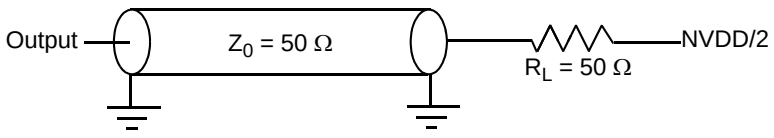


Figure 56. SPI AC Test Load

Figure 57 and Figure 58 represent the AC timing from Table 67. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
USB_DP	A11	I/O	USB_VDDA	—
USB_DM	A12	I/O	USB_VDDA	—
USB_VBUS	C12	I	—	—
USB_TPA	A14	O	—	—
USB_RBIAS	D14	I	—	8
USB_PLL_PWR3	A13	I	—	—
USB_PLL_GND0 & USB_PLL_GND1	D13	I	—	—
USB_PLL_PWR1	B13	I	—	—
USB_VSSA_BIAS	E14	I	—	—
USB_VDDA_BIAS	C14	I	—	—
USB_VSSA	E13	I	—	—
USB_VDDA	E12	I	—	—
GPIO				
GPIO_0/$\overline{\text{DMA\_DREQ1}}$/$\overline{\text{GTM1\_TOUT1}}$	C5	I/O	$NVDD1_{ON}$	—
GPIO_1/$\overline{\text{DMA\_DACK1}}$/GTM1_TIN2/GTM2_TIN1	A4	I/O	$NVDD1_{ON}$	—
GPIO_2/$\overline{\text{DMA\_DONE1}}$/$\overline{\text{GTM1\_TGATE2}}$/$\overline{\text{GTM2\_TGATE1}}$	K3	I/O	$NVDD4_{OFF}$	—
GPIO_3/GTM1_TIN3/GTM2_TIN4	K1	I/O	$NVDD4_{OFF}$	—
GPIO_4/$\overline{\text{GTM1\_TGATE3}}$/$\overline{\text{GTM2\_TGATE4}}$	K2	I/O	$NVDD4_{OFF}$	—
GPIO_5/$\overline{\text{GTM1\_TOUT3}}$/$\overline{\text{GTM2\_TOUT1}}$	L5	I/O	$NVDD4_{OFF}$	—
GPIO_6/GTM1_TIN4/GTM2_TIN3	L3	I/O	$NVDD4_{OFF}$	—
GPIO_7/$\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$	L1	I/O	$NVDD4_{OFF}$	—
GPIO_8/USBDR_DRIVE_VBUS/GTM1_TIN1/GTM2_TIN2	M1	I/O	$NVDD4_{OFF}$	—
GPIO_9/USBDR_PWRFAULT/$\overline{\text{GTM1\_TGATE1}}$/$\overline{\text{GTM2\_TGATE2}}$	M2	I/O	$NVDD4_{OFF}$	—
GPIO_10/USBDR_PCTL0/$\overline{\text{GTM1\_TOUT2}}$/$\overline{\text{GTM2\_TOUT1}}$	M5	I/O	$NVDD4_{OFF}$	—
GPIO_11/USBDR_PCTL1/$\overline{\text{GTM1\_TOUT4}}$/$\overline{\text{GTM2\_TOUT3}}$	M4	I/O	$NVDD4_{OFF}$	—
SPI				
SPIMOSI/GPIO_15	W3	I/O	$NVDD1_{OFF}$	—
SPIMISO/GPIO_16	W4	I/O	$NVDD1_{OFF}$	—
SPICLK	Y1	I/O	$NVDD1_{OFF}$	—
SPISEL/GPIO_17	W2	I/O	$NVDD1_{OFF}$	—

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
VSS1IO	M24, N24, P19, P20, P25, P27, R25, R27, T24	I	—	—
XCOREVDD	P2, P10, R2, T1	I	—	—
XCOREVSS	R3, R10, U2, V2	I	—	—
XPADVDD	P3, R9, U3	I	—	—
XPADVSS	P5, P9, V3	I	—	—

Note:

1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to NVDD.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to NVDD.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. This pin must always be tied to VSS.
7. Thermal sensitive resistor.
8. This pin should be connected to USB_VSSA_BIAS through 10K precision resistor.
9. The LB_POR_CFG_BOOT_ECC functionality for this pin is only available in MPC8315E revision 1.1 and later. The LB_POR_CFG_BOOT_ECC is sampled only during the $\overline{\text{PORESET}}$ negation. This pin with an internal pull down resistor enables the ECC by default. To disable the ECC an external strong pull up resistor or a tristate buffer is needed.
10. This pin should be connected to an external 2.7 K ±1% resistor connected to VSS. The resistor should be placed as close as possible to the input.
11. This pin has a weak internal pull-down.
12. This pin has a weak internal pull-up.

25.2 Thermal Management Information

For the following sections, $P_D = (VDD \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers.

25.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity T_J - T_A) are possible.

25.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction to ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JB}$ = junction to board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias. Note that the RC filter results in lower voltage level on AVDD. This does not imply that the DC specification can be relaxed.

This figure shows the PLL power supply filter circuit.

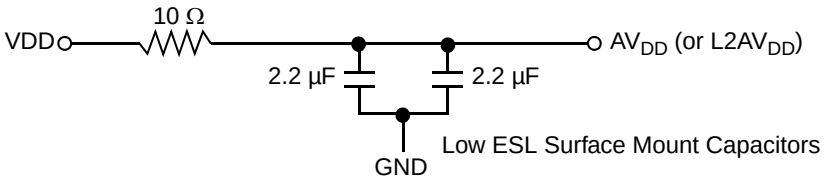


Figure 63. PLL Power Supply Filter Circuit

26.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8315E system, and the MPC8315E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each VDD, NVDD, GVDD, and LVDD pins of the device. These decoupling capacitors should receive their power from separate VDD, NVDD, GVDD, LVDD, and GND power planes in the PCB, utilizing thick and short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the VDD, NVDD, GVDD, and LVDD planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

26.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to NVDD, GVDD, or LVDD as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.