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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8315cvradda

2.9 Dual Serial ATA (SATA) Controllers

The SATA controllers have the following features:

- Designed to comply with *Serial ATA Rev 2.5 Specification*
- ATAPI 6+
- Spread spectrum clocking on receive
- Asynchronous notification
- Hot plug including asynchronous signal recovery
- Link power management
- Native command queuing
- Staggered spin-up and port multiplier support
- SATA 1.5 and 3.0 Gbps operation
- Interrupt driven
- Power management support
- Error handling and diagnostic features
  - Far end/near end loopback
  - Failed CRC error reporting
  - Increased ALIGN insertion rates
  - Scrambling and CONT override

2.10 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The eTSECs include the following features:

- Two SGMII/RGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Std 802.3™, IEEE 802.3u™, IEEE 802.3x™, IEEE 802.3z™, IEEE 802.3au™, IEEE 802.3ab™, and IEEE Std 1588™
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status.

2.11 Integrated Programmable Interrupt Controller (IPIC)

The integrated programmable interrupt controller (IPIC) provides a flexible solution for general-purpose interrupt control. The IPIC programming model is compatible with the MPC8260 interrupt controller and supports external and internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

2.12 Power Management Controller (PMC)

The MPC8315E supports a range of power management states that significantly lower power consumption under the control of the power management controller. The PMC includes the following features:

- Provides power management when the device is used in both PCI host and agent modes
- PCI Power Management 1.2 D0, D1, D2, D3hot, and D3cold states
- PME generation in PCI agent mode, PME detection in PCI host mode
- Wake-up from Ethernet (magic packet), USB, GPIO, and PCI (PME input as host) while in the D1, D2 and D3hot states
- A new low-power standby power management state called D3warm
  - The PMC, one Ethernet port, and the GTM block remain powered via a split power supply controlled through an external power switch
  - Wake-up events include Ethernet (magic packet), GTM, GPIO, or IRQ inputs and cause the device to transition back to normal operation
  - PCI agent mode is not be supported in D3warm state
- PCI Express-based PME events are not supported

2.13 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the MPC8315E to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

2.14 DMA Controller, I^2C, DUART, Enhanced Local Bus Controller (eLBC), and Timers

The integrated four-channel DMA controller includes the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters)
- Misaligned transfer capability for source/destination address
- Supports external DREQ, DACK and DONE signals

There is one I^2C controller. This synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The eLBC port allows connections with a wide variety of external DSPs and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GVDD + 0.3)	V	2, 4
	DDR DRAM reference	MVREF	–0.3 to (GVDD + 0.3)	V	2, 4
	eTSEC signals	LV_{IN}	–0.3 to (LVDD + 0.3)	V	3, 4
	Local bus, DUART, SYS_CLK_IN, system control and power management, I^2C, and JTAG signals	NV_{IN}	–0.3 to (NVDD + 0.3)	V	3, 4
	PCI	NV_{IN}	–0.3 to (NVDD + 0.3)	V	5
	SATA_CLKIN	NV_{IN}	–0.3 to (NVDD + 0.3)	V	3, 4
Storage temperature range		T_{STG}	–55 to150	°C	—

Note:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** (N,L)V_{IN} must not exceed (N,L)VDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. (M,N,L)V_{IN} and MVREF may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
5. NV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 2.
6. The max value of supply voltage should be selected based on the RGMII mode.
7. NVDD means NVDD1_OFF, NVDD1_ON, NVDD2_OFF, NVDD2_ON, NVDD3_OFF, NVDD4_OFF
8. LVDD means LVDD1_OFF and LVDD2_ON

3.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for theMPC8315E. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value[1]	Unit	Status in D3 Warm mode	Note
SerDes internal digital power	XCOREVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes internal digital power	XCOREVSS	0.0	V	—	—
SerDes I/O digital power	XPADVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes I/O digital power	XPADVSS	0.0	V	—	—
SerDes analog power for PLL	SDAVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes analog power for PLL	SDAVSS	0.0	V	—	—
Dedicated 3.3 V analog power for USB PLL	USB_PLL_PWR3	3.3 ± 165mv	V	Switched Off	—
Dedicated 1.0 Vanalog power for USB PLL	USB_PLL_PWR1	1.0 ± 50 mv	V	Switched Off	—
Dedicated analog ground for USB PLL	USB_PLL_GND	0.0	V	—	—
Dedicated USB power for USB bias circuit	USB_VDDA_BIAS	3.3 ± 300 mv	V	Switched Off	—

Table 28. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load.

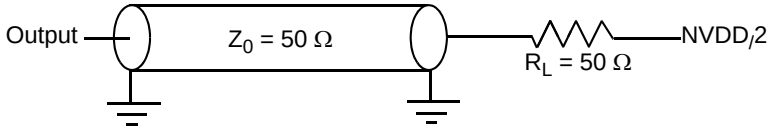


Figure 14. AC Test Load

This figure shows the RMII receive AC timing diagram.

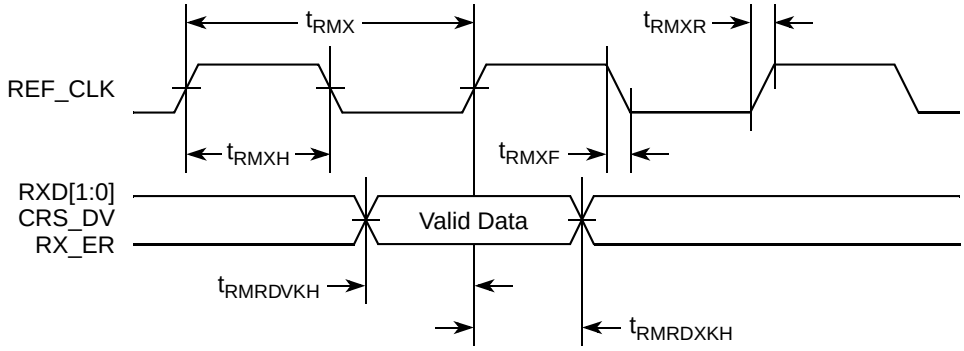


Figure 15. RMII Receive AC Timing Diagram

9.2.3 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 29. RGMII and RTBI AC Timing Specifications

At recommended operating conditions (see Table 2)

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	–0.6	—	0.6	ns
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.6	ns

Table 44. Local Bus General Timing Parameters (continued)

Parameter	Symbol [1]	Min	Max	Unit	Note
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD	t_{LBKHOZ}	—	4	ns	8
LALE output rise to LCLK negative edge	$t_{LALEHOV}$	—	3.0	ns	

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from NVDD/2 of the rising/falling edge of LCLK0 to 0.4 × NVDD of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.
8. For active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This figure provides the AC test load for the local bus.

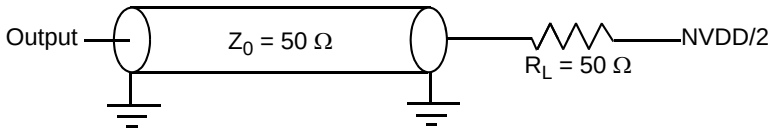


Figure 24. Local Bus AC Test Load

This figure shows the AC timing diagram for the I^2C bus.

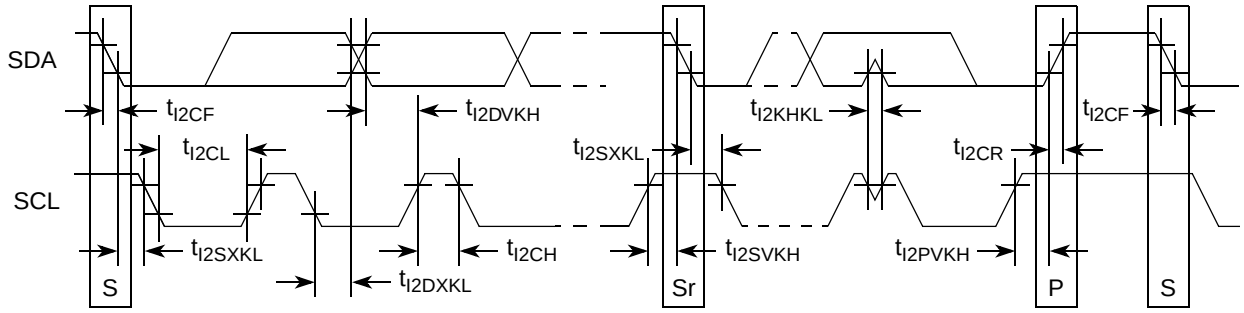


Figure 34. I^2C Bus AC Timing Diagram

14 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8315E.

14.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface.

Table 49. PCI DC Electrical Characteristics [1]

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	0.5 x NVDD	NVDD + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.5	0.3 × NVDD	V
High-level output voltage	V_{OH}	NVDD = min, I_{OH} = –500 µA	0.9 x NVDD	—	V
Low-level output voltage	V_{OL}	NVDD = min, I_{OL} = 1500 µA	—	0.1 x NVDD	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NVDD	—	± 10	µA

Note:
1. The symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

14.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8315E is configured as a host or agent device. This table shows the PCI AC timing specifications at 66 MHz.

Table 50. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol [1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.3	—	ns	2, 4

assumes that the LVPECL clock driver's output impedance is 50Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140Ω to 240Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8315E SerDes reference clock's differential input amplitude requirement (between 200mV and 800mV differential peak). For example, if the LVPECL output's differential peak is 900mV and the desired SerDes reference clock input amplitude is selected as 600mV, the attenuation factor is 0.67, which requires R2 = 25Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

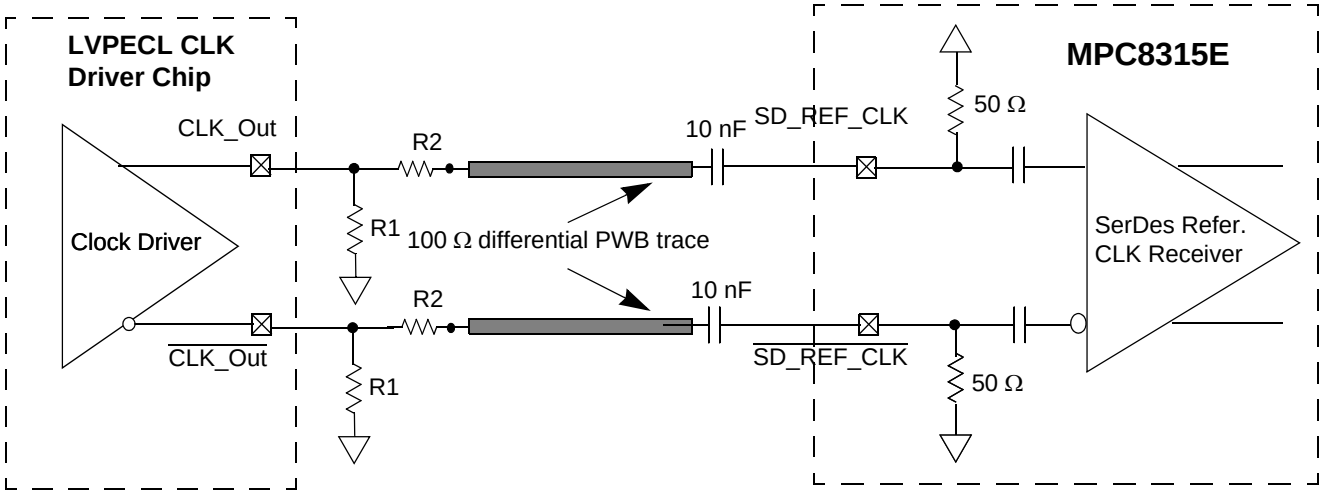


Figure 45. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8315E SerDes reference clock input's DC requirement.

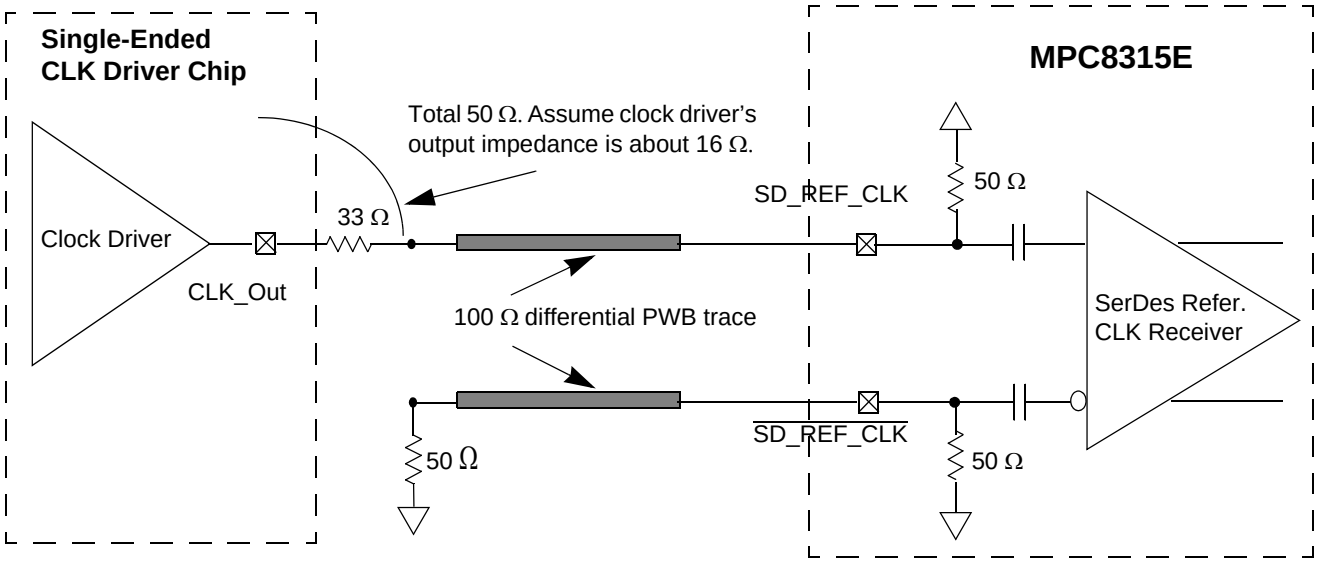


Figure 46. Single-Ended Connection (Reference Only)

16 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8315E.

16.1 DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK

For more information, see Section 15.2, "SerDes Reference Clocks."

16.2 AC Requirements for PCI Express SerDes Clocks

This table lists the PCI Express SerDes clock AC requirements.

Table 53. SD_REF_CLK and SD_REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Unit	Note
t_{REF}	REFCLK cycle time	—	10	—	ns	—
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	–50	—	50	ps	—

16.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

16.4 Physical Layer Specifications

Following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer please use the *PCI Express Base Specification*, Rev. 1.0a.

16.4.1 Differential Transmitter (TX) Output

This table defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 54. Differential Transmitter (TX) Output Specifications

Parameter	Symbol	Comments	Min	Typical	Max	Unit	Note
Unit interval	UI	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations.	399.88	400	400.12	ps	1
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	$V_{TX-DIFFp-p} = 2*\|V_{TX-D+} - V_{TX-D-}\|$	0.8	—	1.2	V	2

16.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 51 is specified using the passive compliance/test measurement load (see Figure 52) in place of any real PCI Express RX component. In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 52) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 51) expected at the input receiver based on an adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 Ω probes—see Figure 52). Note that the series capacitors, $C_{PEACCTX}$, are optional for the return loss measurement.

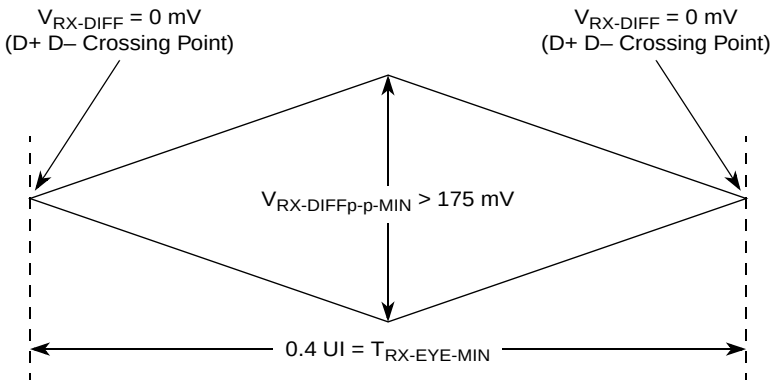


Figure 51. Minimum Receiver Eye Timing and Voltage Compliance Specification

16.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 52.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

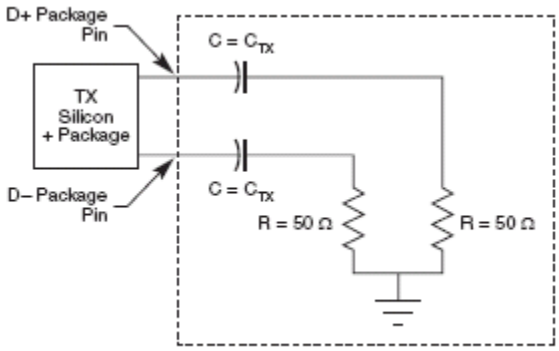


Figure 52. Compliance Test/Measurement Load

17 Serial ATA (SATA)

The serial ATA (SATA) of the MPC8315E is designed to comply with Serial ATA 2.5 Specification. Note that the external cabled applications or long backplane applications (Gen1x & Gen2x) are not supported.

17.1 Requirements for SATA REF_CLK

The reference clock for MPC8315E is a single ended input clock required for the SATA Interface operation. The AC requirements for the SATA reference clock are listed in the this table.

Table 56. Reference Clock Input Requirements

Parameter	Symbol	Conditions	Min	Typical	Max	Unit	Note
Frequency range	t_{CLK_REF}	—	50	75	150	MHz	1
Clock frequency tolerance	t_{CLK_TOL}	—	-350	0	+350	ppm	—
Input High Voltage	V_{CLK_INHI}	—	2.0	—	—	V	—
Input Low Voltage	V_{CLK_INLo}	—	—	—	0.7	V	—
Reference clock rise and fall time	t_{CLK_RISE}/ t_{CLK_FALL}	20% to 80% of nominal amplitude	—	—	2	ns	—
Reference clock duty cycle	t_{CLK_DUTY}	Measured at 1.6V	40	50	60	%	—

Table 61. Timers Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit

Note:
1. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers input are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure provides the AC test load for the Timers.

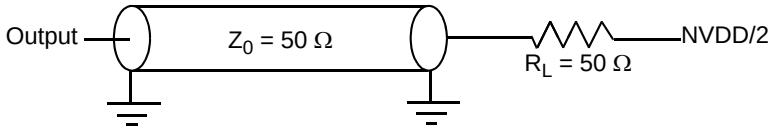


Figure 54. Timers AC Test Load

19 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8315E.

19.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO.

Table 62. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le$ NVDD	—	± 5	μA

19.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 63. GPIO Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Note:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Table 70. MPC8315E TEPBGA II Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Note
DDR Memory Controller Interface				
MEMC_MDQ[0]	AF16	I/O	GVDD	—
MEMC_MDQ[1]	AE17	I/O	GVDD	—
MEMC_MDQ[2]	AH17	I/O	GVDD	—
MEMC_MDQ[3]	AG17	I/O	GVDD	—
MEMC_MDQ[4]	AG18	I/O	GVDD	—
MEMC_MDQ[5]	AH18	I/O	GVDD	—
MEMC_MDQ[6]	AD18	I/O	GVDD	—
MEMC_MDQ[7]	AF19	I/O	GVDD	—
MEMC_MDQ[8]	AH19	I/O	GVDD	—
MEMC_MDQ[9]	AD19	I/O	GVDD	—
MEMC_MDQ[10]	AG20	I/O	GVDD	—
MEMC_MDQ[11]	AH20	I/O	GVDD	—
MEMC_MDQ[12]	AH21	I/O	GVDD	—
MEMC_MDQ[13]	AE21	I/O	GVDD	—
MEMC_MDQ[14]	AH22	I/O	GVDD	—
MEMC_MDQ[15]	AD21	I/O	GVDD	—
MEMC_MDQ[16]	AG10	I/O	GVDD	—
MEMC_MDQ[17]	AH9	I/O	GVDD	—
MEMC_MDQ[18]	AH8	I/O	GVDD	—
MEMC_MDQ[19]	AD11	I/O	GVDD	—
MEMC_MDQ[20]	AH7	I/O	GVDD	—
MEMC_MDQ[21]	AG7	I/O	GVDD	—
MEMC_MDQ[22]	AF8	I/O	GVDD	—
MEMC_MDQ[23]	AD10	I/O	GVDD	—
MEMC_MDQ[24]	AE9	I/O	GVDD	—
MEMC_MDQ[25]	AH6	I/O	GVDD	—
MEMC_MDQ[26]	AH5	I/O	GVDD	—
MEMC_MDQ[27]	AG6	I/O	GVDD	—
MEMC_MDQ[28]	AH4	I/O	GVDD	—
MEMC_MDQ[29]	AE6	I/O	GVDD	—
MEMC_MDQ[30]	AD8	I/O	GVDD	—
MEMC_MDQ[31]	AF5	I/O	GVDD	—
MEMC_MDM0	AE18	O	GVDD	—
MEMC_MDM1	AE20	O	GVDD	—
MEMC_MDM2	AE10	O	GVDD	—

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
LGPL1/LFALE	AA28	O	$NVDD3_{OFF}$	—
LGPL2/$\overline{\text{LFRE}}$/$\overline{\text{LOE}}$	Y25	O	$NVDD3_{OFF}$	12
LGPL3/$\overline{\text{LFWP}}$	Y24	O	$NVDD3_{OFF}$	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/$\overline{\text{LFRB}}$	AA26	I/O	$NVDD3_{OFF}$	2
LGPL5	AF22	O	$NVDD3_{OFF}$	12
LCLK0	AH25	O	$NVDD3_{OFF}$	11
LCLK1	AD24	O	$NVDD3_{OFF}$	11
DUART				
UART_SOUT1/MSRCID0 (DDR ID)/LSRCID0	C15	O	$NVDD2_{OFF}$	—
UART_SIN1/MSRCID1 (DDR ID)/LSRCID1	B16	I/O	$NVDD2_{OFF}$	—
$\overline{\text{UART\_CTS}}$[1]/MSRCID2 (DDR ID)/LSRCID2	D16	I/O	$NVDD2_{OFF}$	—
$\overline{\text{UART\_RTS}}$[1]/MSRCID3 (DDR ID)/LSRCID3	B17	O	$NVDD2_{OFF}$	—
UART_SOUT2/MSRCID4 (DDR ID)/LSRCID4	A16	O	$NVDD2_{OFF}$	—
UART_SIN2/MDVAL (DDR ID)/LDVAL	C16	I/O	$NVDD2_{OFF}$	—
$\overline{\text{UART\_CTS}}$[2]	A17	I	$NVDD2_{OFF}$	—
$\overline{\text{UART\_RTS}}$[2]	A18	O	$NVDD2_{OFF}$	—
I^2C interface				
IIC_SDA/$\overline{\text{CKSTOP\_OUT}}$	N1	I/O	$NVDD4_{OFF}$	2
IIC_SCL/$\overline{\text{CKSTOP\_IN}}$	N2	I/O	$NVDD4_{OFF}$	2
Interrupts				
$\overline{\text{MCP\_OUT}}$	W1	O	$NVDD1_{OFF}$	2
$\overline{\text{IRQ}}$[0]/$\overline{\text{MCP\_IN}}$	Y3	I	$NVDD1_{OFF}$	—
$\overline{\text{IRQ}}$[1]	E1	I	$NVDD1_{ON}$	—
$\overline{\text{IRQ}}$[2]	A7	I	$NVDD1_{ON}$	—
$\overline{\text{IRQ}}$[3]	AA1	I	$NVDD1_{OFF}$	—
$\overline{\text{IRQ}}$[4]	Y5	I	$NVDD1_{OFF}$	—
$\overline{\text{IRQ}}$[5]/$\overline{\text{CORE\_SRESET\_IN}}$	AA2	I	$NVDD1_{OFF}$	—
$\overline{\text{IRQ}}$[6] /$\overline{\text{CKSTOP\_OUT}}$	AA4	I/O	$NVDD1_{OFF}$	—
$\overline{\text{IRQ}}$[7]/$\overline{\text{CKSTOP\_IN}}$	AA5	I	$NVDD1_{OFF}$	—
Configuration				
$\overline{\text{CFG\_CLKIN\_DIV}}$	A5	I	$NVDD1_{ON}$	12
EXT_PWR_CTRL	D3	O	$NVDD1_{ON}$	12
PMC_PWR_OK	D4	I	—	12

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{QUIESCE}}$	B5	O	$NVDD1_{ON}$	—
System Control				
$\overline{\text{HRESET}}$	B6	I/O	$NVDD1_{ON}$	1
$\overline{\text{PORESET}}$	A6	I	$NVDD1_{ON}$	—
Clocks				
SYS_XTAL_IN	L27	I	$NVDD2_{ON}$	—
SYS_XTAL_OUT	J28	O	$NVDD2_{ON}$	—
SYS_CLK_IN	K28	I	$NVDD2_{ON}$	—
USB_XTAL_IN	A15	I	$NVDD2_{OFF}$	—
USB_XTAL_OUT	B14	O	$NVDD2_{OFF}$	—
USB_CLK_IN	B15	I	$NVDD2_{OFF}$	—
PCI_SYNC_OUT	J27	O	$NVDD2_{ON}$	3
RTC_CLK	K26	I	$NVDD2_{ON}$	—
PCI_SYNC_IN	K27	I	$NVDD2_{ON}$	—
MISC				
AVDD1	AC15	I	—	—
AVDD2	M23	I	—	—
THERM0	L25	I	$NVDD2_{ON}$	7
$\overline{\text{DMA\_DACK0}}$/GPIO_13	AC4	I/O	$NVDD1_{OFF}$	—
$\overline{\text{DMA\_DREQ0}}$/GPIO_12	AD1	I/O	$NVDD1_{OFF}$	—
DMA_DONE0/GPIO_14	AD2	I/O	$NVDD1_{OFF}$	—
NC, No Connect	A2	—	—	—
NC, No Connect	U25	—	—	—
PCI				
$\overline{\text{PCI\_INTA}}$	B18	O	$NVDD2_{OFF}$	—
$\overline{\text{PCI\_RESET\_OUT}}$	A20	O	$NVDD2_{OFF}$	—
PCI_AD[0]	J25	I/O	$NVDD2_{OFF}$	—
PCI_AD[1]	J24	I/O	$NVDD2_{OFF}$	—
PCI_AD[2]	K24	I/O	$NVDD2_{OFF}$	—
PCI_AD[3]	H27	I/O	$NVDD2_{OFF}$	—
PCI_AD[4]	H28	I/O	$NVDD2_{OFF}$	—
PCI_AD[5]	H26	I/O	$NVDD2_{OFF}$	—
PCI_AD[6]	G27	I/O	$NVDD2_{OFF}$	—
PCI_AD[7]	G28	I/O	$NVDD2_{OFF}$	—
PCI_AD[8]	F26	I/O	$NVDD2_{OFF}$	—

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
Power and Ground Supplies				
GVDD	Y11, Y12, Y14, Y15, Y17, AC8, AC11, AC14, AC17, AD6, AD9, AD17, AE8, AE13, AE19, AF10, AF15, AF21, AG2, AG3, AG8, AG13, AG19, AH2	I	—	—
LVDD1_OFF	H6, J3, L6, L9, M9	I	—	—
LVDD2_ON	C11, D9, E10, F11, J12	I	—	—
NVDD1_OFF	U9, V9, W10, Y4, Y6, AA3, AB4	I	—	—
NVDD1_ON	B1, B2, C1, D5, E7, F5, F9, J11, K10	I	—	—
NVDD2_OFF	B22, B27, C19, E16, F15, F18, F21, F25, H25, J17, J18, J23, L20, M20	I	—	—
NVDD2_ON	L26, N19	I	—	—
NVDD3_OFF	U20, V20, V23, V26, W19, Y18, Y26, AA23, AA25, AC20, AC25, AD23, AE25, AG25, AG27	I	—	—
NVDD4_OFF	K4, L2, M6, N10	I	—	—
VDD	J15, K15, K16, K17, K18, K19, L10, L19, M10, T10, U10, U19, V10, V19, W11, W12, W13, W14, W15, W16, W17, W18	I	—	—
VDD1ANA	P23, R23, T19	I	—	—
VDD1IO	M26, N26, P28, R28	I	—	—
VDDC	J14, K11, K12, K13, K14, M19	I	—	—
VSS	A3, A27, B3, B12, B24, B28, C6, C8, C13, C17, C21, C23, C26, D2, D7, D15, D18, D20, D22, E4, E6, E11, E24, E26, F8, F12, F14, F17, F20, G3, G26, H4, H23, J6, J26, K25, L4, L11, L12, L13, L14, L15, L16, L17, L18, L23, L28, M3, M11, M12, M13, M14, M15, M16, M17, M18, N5, N11, N12, N13, N14, N15, N16, N17, N18, P6, P11, P12, P13, P14, P15, P16, P17, P18, R6, R11, R12, R13, R14, R15, R16, R17, R18, T11, T12, T13, T14, T15, T16, T17, T18, U5, U6, U11, U12, U13, U14, U15, U16, U17, U18, V6, V11, V12, V13, V14, V15, V16, V17, V18, W5, W25, W27, Y2, Y23, AA6, AA27, AB2, AB26, AC5, AC9, AC12, AC18, AC21, AD3, AD14, AD16, AD20, AD26, AE2, AE7, AE11, AE16, AE22, AE24, AF2, AF9, AF12, AF18, AF20, AF23, AF27, AG1, AG5, AG11, AG16, AG22, AG28, AH27	I	—	—
VSS1ANA	P24, R19, R20, R24	I	—	—

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

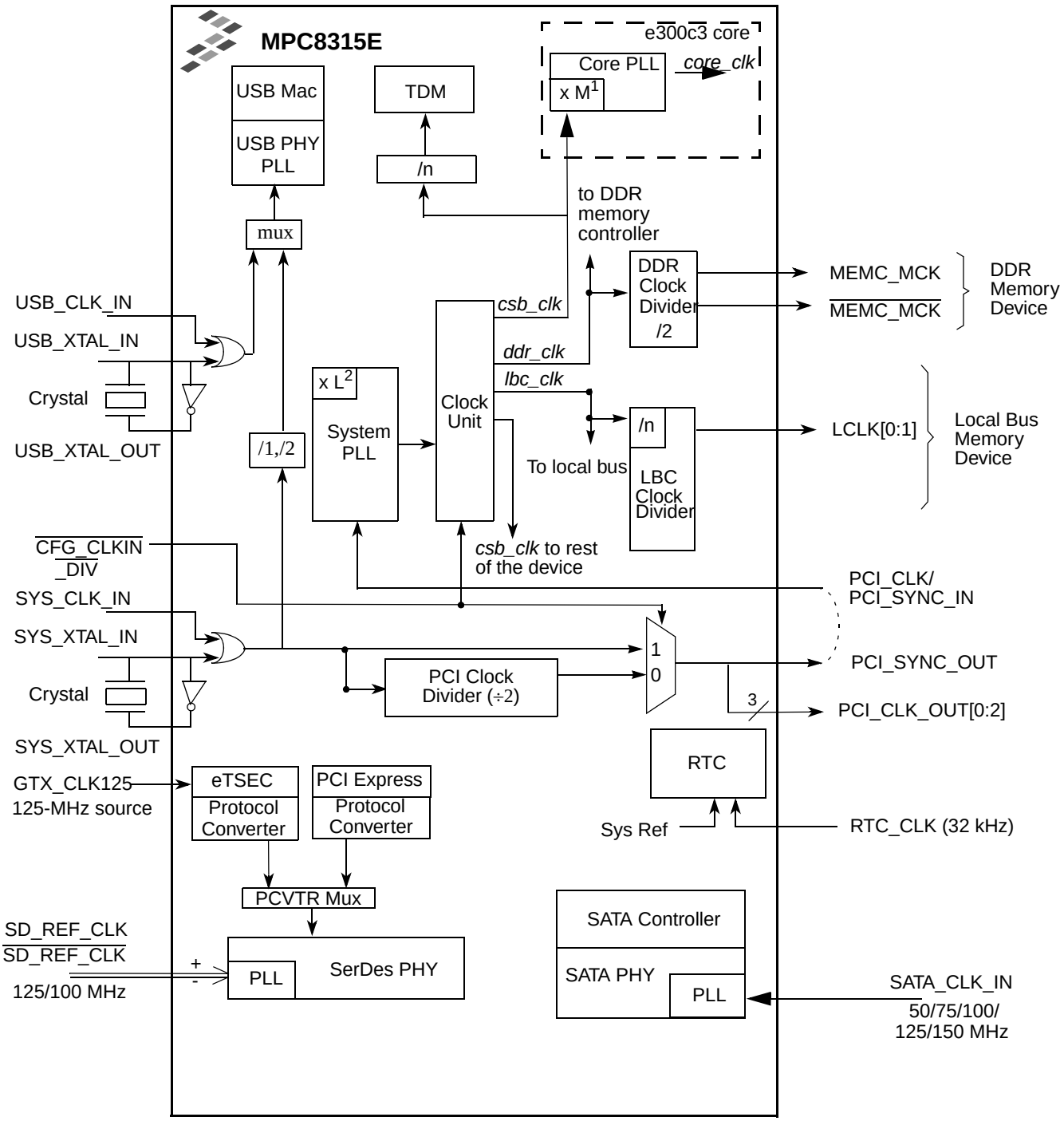
Signal	Package Pin Number	Pin Type	Power Supply	Note
VSS1IO	M24, N24, P19, P20, P25, P27, R25, R27, T24	I	—	—
XCOREVDD	P2, P10, R2, T1	I	—	—
XCOREVSS	R3, R10, U2, V2	I	—	—
XPADVDD	P3, R9, U3	I	—	—
XPADVSS	P5, P9, V3	I	—	—

Note:

1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to NVDD.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to NVDD.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. This pin must always be tied to VSS.
7. Thermal sensitive resistor.
8. This pin should be connected to USB_VSSA_BIAS through 10K precision resistor.
9. The LB_POR_CFG_BOOT_ECC functionality for this pin is only available in MPC8315E revision 1.1 and later. The LB_POR_CFG_BOOT_ECC is sampled only during the $\overline{\text{PORESET}}$ negation. This pin with an internal pull down resistor enables the ECC by default. To disable the ECC an external strong pull up resistor or a tristate buffer is needed.
10. This pin should be connected to an external 2.7 K ±1% resistor connected to VSS. The resistor should be placed as close as possible to the input.
11. This pin has a weak internal pull-down.
12. This pin has a weak internal pull-up.

24 Clocking

This figure shows the internal distribution of clocks within the MPC8315E.



1 Multiplication factor M = 1, 1.5, 2, 2.5, and 3. Value is decided by RCWLR[COREPLL].

2 Multiplication factor L = 2, 3, 4 and 5. Value is decided by RCWLR[SPMF].

Figure 62. MPC8315E Clock Subsystem

Table 73. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110–1111	Reserved

As described in Section 24, "Clocking," The LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ configuration input signal select the ratio between the primary clock input (SYS_CLK_IN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 74 and Table 75 shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN/PCI_SYNC_IN ratios.

Table 74. CSB Frequency Options for Host Mode

$\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ at Reset[1]	SPMF	csb_clk : Input Clock Ratio [2]	Input Clock Frequency (MHz)[2]		
			24	33.33	66.67
High/Low [3]	0010	2:1			133
High/Low	0011	3:1		100	—
High/Low	0100	4:1	96	133	—
High/Low	0101	5:1	120	—	—

1 $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ select the ratio between SYS_CLK_IN and PCI_SYNC_OUT.
2 SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.
3 In the Host mode it does not matter if the value is High or Low.

Table 75. CSB Frequency Options for Agent Mode

$\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio [2]	Input Clock frequency (MHz)[2]		
			25	33.33	66.67
High	0010	2: 1			133
High	0011	3: 1		100	—
High	0100	4: 1		133	—
High	0101	5: 1	120	—	—

1 $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ doubles csb_clk if set low.
2 SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias. Note that the RC filter results in lower voltage level on AVDD. This does not imply that the DC specification can be relaxed.

This figure shows the PLL power supply filter circuit.

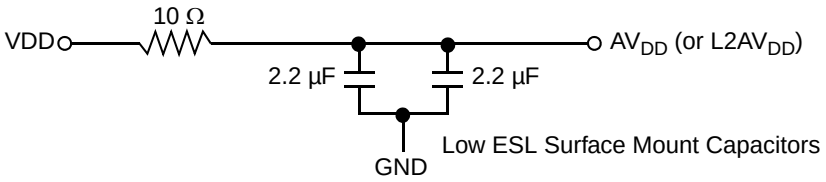


Figure 63. PLL Power Supply Filter Circuit

26.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8315E system, and the MPC8315E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each VDD, NVDD, GVDD, and LVDD pins of the device. These decoupling capacitors should receive their power from separate VDD, NVDD, GVDD, LVDD, and GND power planes in the PCB, utilizing thick and short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the VDD, NVDD, GVDD, and LVDD planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

26.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to NVDD, GVDD, or LVDD as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 81. Part Numbering Nomenclature

MPC	8315	E	C	VR	AG	D	A
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range [3]**	**Package [1]**	**e300 Core Frequency [2]**	**DDR Frequency**	**Revision Level**
MPC	8315	Blank = Not included E = included	Blank = 0 to 105°C C = –40 to 105°C	VR= Pb Free TEPBGA II	AD = 266 MHz AF = 333 MHz AG = 400 MHz	D = 266 MHz	Contact local Freescale sales office

Note:
1. See Section 23, “Package and Pin Listings,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by electric may support other maximum core frequencies.
3. Contact your local Freescale field applications engineer (FAE).

This table shows the SVR settings by device and package type.

Table 82. SVR Settings

Device	Package	SVR (Rev 1.0)	SVR (Rev 1.1)	SVR (Rev 1.2)
MPC8315E	TEPBGA II	0x80B4_0010	0x80B4_0011	0x80B4_0012
MPC8315	TEPBGA II	0x80B5_0010	0x80B5_0011	0x80B5_0012

Note:
1. PVR = 8085_0020 for all devices and revisions in this table.