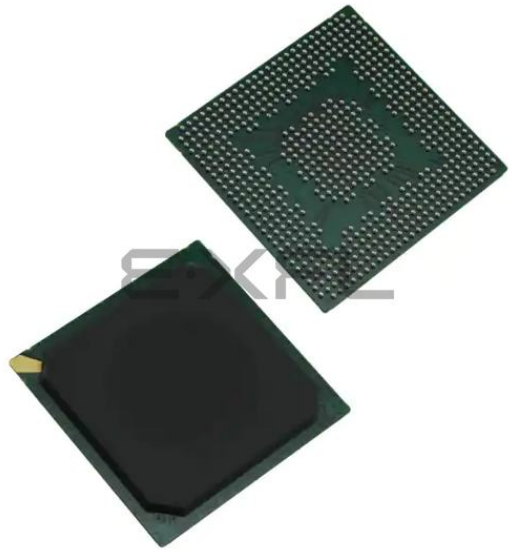

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8315cvrafda

1 Overview

The MPC8315E incorporates the e300c3 (MPC603e-based) core, which includes 16 Kbytes of L1 instruction and data caches, on-chip memory management units (MMUs), and floating-point support. In addition to the e300 core, the SoC platform includes features such as dual enhanced three-speed 10, 100, 1000 Mbps Ethernet controllers (eTSECs) with SGMII support, a 32- or 16-bit DDR1/DDR2 SDRAM memory controller, dual SATA 3 Gbps controllers (MPC8315E-specific), a security engine to accelerate control and data plane security protocols, and a high degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration. The MPC8315E also offers peripheral interfaces such as a 32-bit PCI interface with up to 66 MHz operation, 16-bit enhanced local bus interface with up to 66 MHz operation, TDM interface, and USB 2.0 with an on-chip USB 2.0 PHY.

The MPC8315E offers additional high-speed interconnect support with dual integrated SATA 3 Gbps interfaces and dual single-lane PCI Express interfaces. When not used for PCI Express, the SerDes interface may be configured to support SGMII. The MPC8315E security engine (SEC 3.3) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. This figure shows a block diagram of the MPC8315E.

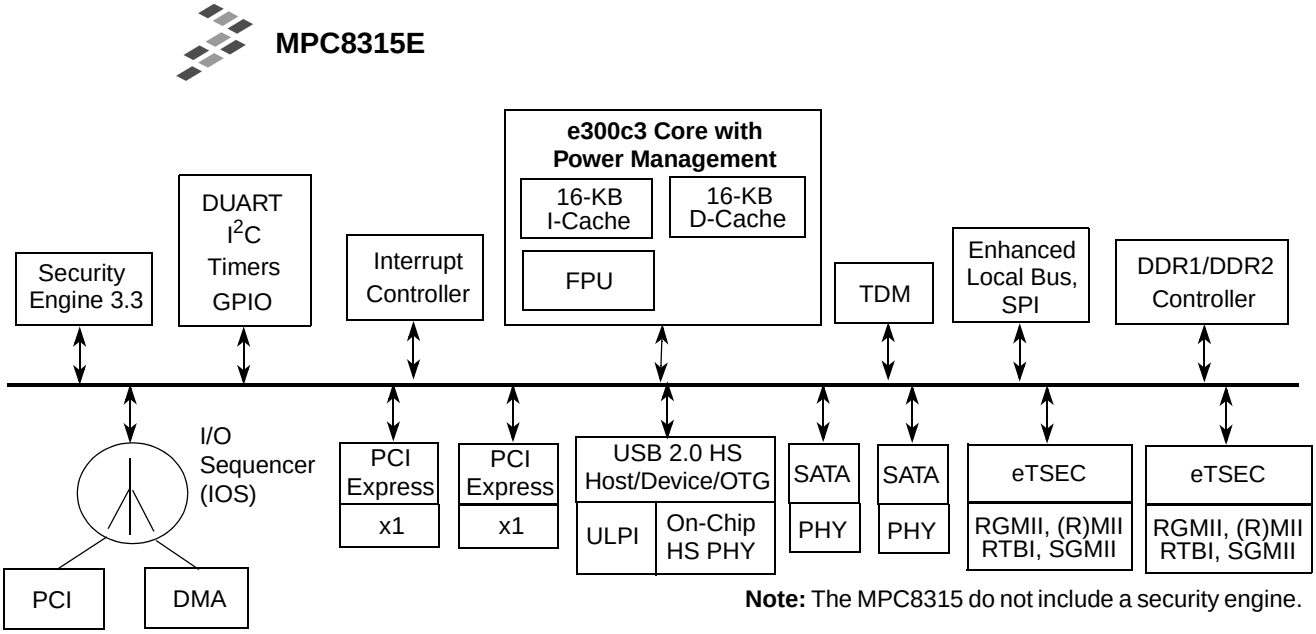

Figure 1. MPC8315E Block Diagram

2 MPC8315E Features

The following features are supported in the MPC8315E.

2.1 e300 Core

The e300 core has the following features:

- Operates at up to 400 MHz

- 16-Kbyte instruction cache, 16-Kbyte data cache
- One floating point unit and two integer units
- Software-compatible with the Freescale processor families implementing the PowerPC Architecture
- Performance monitor

2.2 Serial Interfaces

The following interfaces are supported in the MPC8315E.

- Two enhanced TSECs (eTSECs)
- Two Ethernet interfaces using one RGMII/MII/RMII/RTBI or SGMII (no GMII)
- Dual UART, one I^2C, and one SPI interface

2.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, 802.11i, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are:

- Public key execution unit (PKEU)
  - RSA and Diffie-Hellman (to 4096 bits)
  - Programmable field size up to 2048 bits
  - Elliptic curve cryptography (1023 bits)
  - F2m and F(p) modes
  - Programmable field size up to 511 bits
- Data encryption standard execution unit (DEU)
  - DES, 3DES
  - Two key (K1, K2) or three key (K1, K2, K3)
  - ECB, CBC, CFB-64 and OFB-64 modes for both DES and 3DES
- Advanced encryption standard unit (AESU)
  - Implements the Rinjdael symmetric key cipher
  - Key lengths of 128, 192, and 256 bits
  - ECB, CBC, CCM, CTR, GCM, CMAC, OFB, CFB, XCBC-MAC and LRW modes
  - XOR acceleration
- Message digest execution unit (MDEU)
  - SHA with 160-bit, 256-bit, 384-bit and 512-bit message digest
  - SHA-384/512
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- Random number generator (RNG)

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GVDD + 0.3)	V	2, 4
	DDR DRAM reference	MVREF	–0.3 to (GVDD + 0.3)	V	2, 4
	eTSEC signals	LV_{IN}	–0.3 to (LVDD + 0.3)	V	3, 4
	Local bus, DUART, SYS_CLK_IN, system control and power management, I^2C, and JTAG signals	NV_{IN}	–0.3 to (NVDD + 0.3)	V	3, 4
	PCI	NV_{IN}	–0.3 to (NVDD + 0.3)	V	5
	SATA_CLKIN	NV_{IN}	–0.3 to (NVDD + 0.3)	V	3, 4
Storage temperature range		T_{STG}	–55 to150	°C	—

Note:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** (N,L)V_{IN} must not exceed (N,L)VDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. (M,N,L)V_{IN} and MVREF may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
5. NV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 2.
6. The max value of supply voltage should be selected based on the RGMII mode.
7. NVDD means NVDD1_OFF, NVDD1_ON, NVDD2_OFF, NVDD2_ON, NVDD3_OFF, NVDD4_OFF
8. LVDD means LVDD1_OFF and LVDD2_ON

3.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for theMPC8315E. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value[1]	Unit	Status in D3 Warm mode	Note
SerDes internal digital power	XCOREVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes internal digital power	XCOREVSS	0.0	V	—	—
SerDes I/O digital power	XPADVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes I/O digital power	XPADVSS	0.0	V	—	—
SerDes analog power for PLL	SDAVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes analog power for PLL	SDAVSS	0.0	V	—	—
Dedicated 3.3 V analog power for USB PLL	USB_PLL_PWR3	3.3 ± 165mv	V	Switched Off	—
Dedicated 1.0 Vanalog power for USB PLL	USB_PLL_PWR1	1.0 ± 50 mv	V	Switched Off	—
Dedicated analog ground for USB PLL	USB_PLL_GND	0.0	V	—	—
Dedicated USB power for USB bias circuit	USB_VDDA_BIAS	3.3 ± 300 mv	V	Switched Off	—

Table 3. Output Drive Capability (continued)

Driver Type	Output Impedance (Ω)	Supply Voltage
DUART, system control, I^2C, JTAG,SPI	42	NVDD = 3.3 V
GPIO signals	42	NVDD = 3.3 V
eTSEC	42	LVDD = 3.3 V / 2.5 V

1 Output Impedance can also be adjusted through configurable options in DDR Control Driver Register (DDRCDR). See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.

3.2 Power Sequencing

The MPC8315E does not require the core supply voltage (VDD and VDDC) and I/O supply voltages (GVDD, LVDDx_ON, LVDDx_OFF, NVDDx_ON and NVDDx_OFF) to be applied in any particular order. During the power ramp up, before the power supplies are stable, if the I/O voltages are supplied before the core voltage, there may be a period of time when all input and output pins be actively driven and cause contention and/or excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the continuous core voltage (VDDC) before the continuous I/O voltages (LVDDx_ON and NVDDx_ON) and switchable core voltage (VDD) before the switchable I/O voltages (GVDD, LVDDx_OFF, and NVDDx_OFF). PORESET should be asserted before the continuous power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V, see Figure 3. Once all the power supplies are stable, wait for a minimum of 32 clock cycles before negating PORESET.

The I/O power supply ramp-up slew rate should be slower than 4V/100 μs, this requirement is for ESD circuit.

This figure shows the power-up sequencing for switchable and continuous supplies.

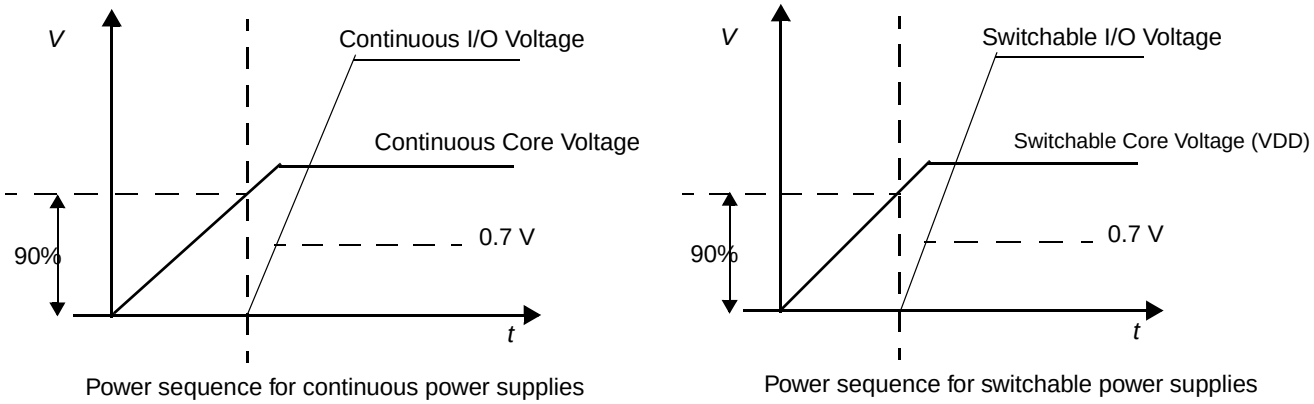

Figure 3. Power-Up Sequencing

When switching from normal mode to D3 warm (standby) mode, first turn off the switchable I/O voltage supply and then turn off the switchable core voltage supply. Similarly, when switching from D3 warm (standby) mode to normal mode, first turn on the switchable core voltage supply and then turn on the switchable I/O voltage supply.

This figure shows the SATA power supplies.

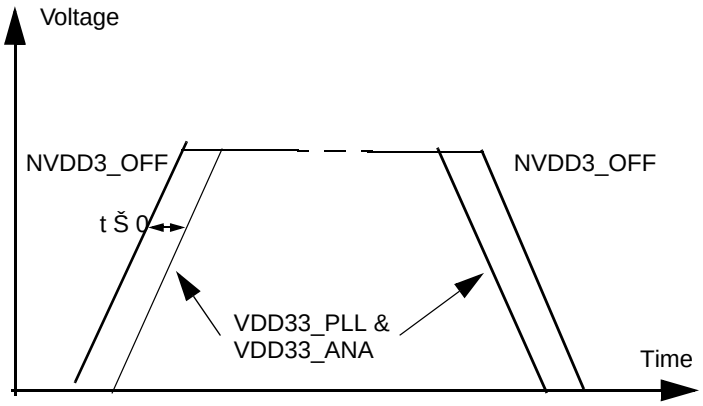

Figure 5. SATA Power Supplies

4 Power Characteristics

This table shows the estimated typical power dissipation for this family of devices.

Table 4. MPC8315E Power Dissipation

(Does not include I/O power dissipation)

Core Frequency (MHz)	CSB Frequency (MHz)	Typical [1,3]	Maximum [1,2]	Unit
266	133	1.116	1.646	W
333	133	1.142	1.665	W
400	133	1.167	1.690	W

Note:

1. The values do not include I/O supply power, but do include core, AVDD, USB PLL, digital SerDes power, and SATA PHY power.
2. Maximum power is based on a voltage of V_{dd} = 1.05V, a junction temperature of T_j = 105°C, and an artificial smoker test.
3. Typical power is based on a voltage of V_{dd} = 1.05V, and an artificial smoker test running at room temperature.

This table shows the estimated typical I/O power dissipation for this family of devices.

Table 5. MPC8315E Power Dissipation

Interface	Frequency	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	NV_{DD} (3.3 V)	LVDD1_OFF/ LVDD2_ON (3.3V)	LVDD2 _ON (3.3V)	VDD33PLL, VDD33ANA (3.3V)	SATA_VDD, VDD1IO, VDD1ANA (1.0V)	XCOREVDD, XPADVDD, SDAVDD (1.0V)	Unit
DDR 1 Rs = 22Ω Rt = 50Ω	266MHz, 32 bits	—	0.323	—	—	—	—	—	—	W
	200MHz, 32 bits	—	0.291	—	—	—	—	—	—	W

Table 9. RESET Initialization Timing Specifications (continued)

Note:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the SYS_CLK_IN input, and PCI_SYNC_IN period depends on the value of CFG_SYS_CLKIN_DIV.
2. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN. It is only valid when the device is in PCI host mode.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:3] and CFG_SYS_CLKIN_DIV.
4. The parameter names CFG_SYS_CLKIN_DIV and CFG_CLKIN_DIV are used interchangeably in this document.

This table provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
System PLL lock times	—	100	μs	—
e300 core PLL lock times	—	100	μs	—
SerDes (SGMII/PCI Exp Phy) PLL lock times	—	100	μs	—
USB phy PLL lock times	—	100	μs	—
SATA phy PLL lock times	—	100	μs	—

7 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8315E. Note that DDR SDRAM is GVDD(typ) = 2.5 V and DDR2 SDRAM is GVDD(typ) = 1.8 V.

7.1 DDR and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8315E when GVDD(typ) = 1.8 V.

Table 11. DDR2 SDRAM DC Electrical Characteristics for GVDD(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GVDD	1.7	1.9	V	1
I/O reference voltage	MVREF	0.49 × GVDD	0.51 × GVDD	V	2
I/O termination voltage	V_{TT}	MVREF – 0.04	MVREF + 0.04	V	3
Input high voltage	V_{IH}	MVREF+ 0.125	GVDD + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.420 V, GVDD= 1.7V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	

9.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

9.2.2.1 RMII Transmit AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications. This table provides the RMII transmit AC timing specifications.

Table 27. RMII Transmit AC Timing Specifications

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	10	ns
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

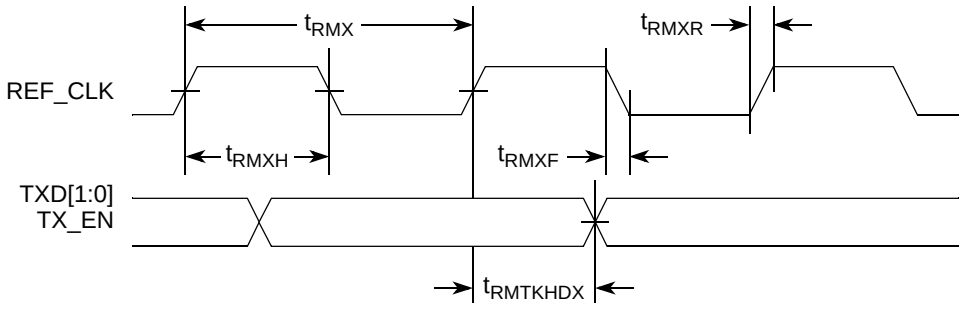

Figure 13. RMII Transmit AC Timing Diagram

9.2.2.2 RMII Receive AC Timing Specifications

This table provides the RMII receive AC timing specifications.

Table 28. RMII Receive AC Timing Specifications

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%

Table 30. MII Management DC Electrical Characteristics Powered at 3.3 V (continued)

Parameter	Symbol	Conditions		Min	Max	Unit
Input low current	I_{IL}	NVDD = Max	V_{IN} = 0.5 V	–600	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

9.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 31. MII Management AC Timing Specifications

At recommended operating conditions with NVDD is 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	170	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 133 MHz, the maximum frequency is 4.16 MHz and the minimum frequency is 0.593 MHz).
3. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 133 MHz, the delay is 60 ns).

12.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface. This table provides the JTAG AC timing specifications as defined in Figure 29 through Figure 32.

Table 46. JTAG AC Timing Specifications (Independent of SYS_CLK_IN) [1]

At recommended operating conditions (see Table 2)

Parameter	Symbol [2]	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5, 6

Note:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Table 28). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

assumes that the LVPECL clock driver's output impedance is 50Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140Ω to 240Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8315E SerDes reference clock's differential input amplitude requirement (between 200mV and 800mV differential peak). For example, if the LVPECL output's differential peak is 900mV and the desired SerDes reference clock input amplitude is selected as 600mV, the attenuation factor is 0.67, which requires R2 = 25Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

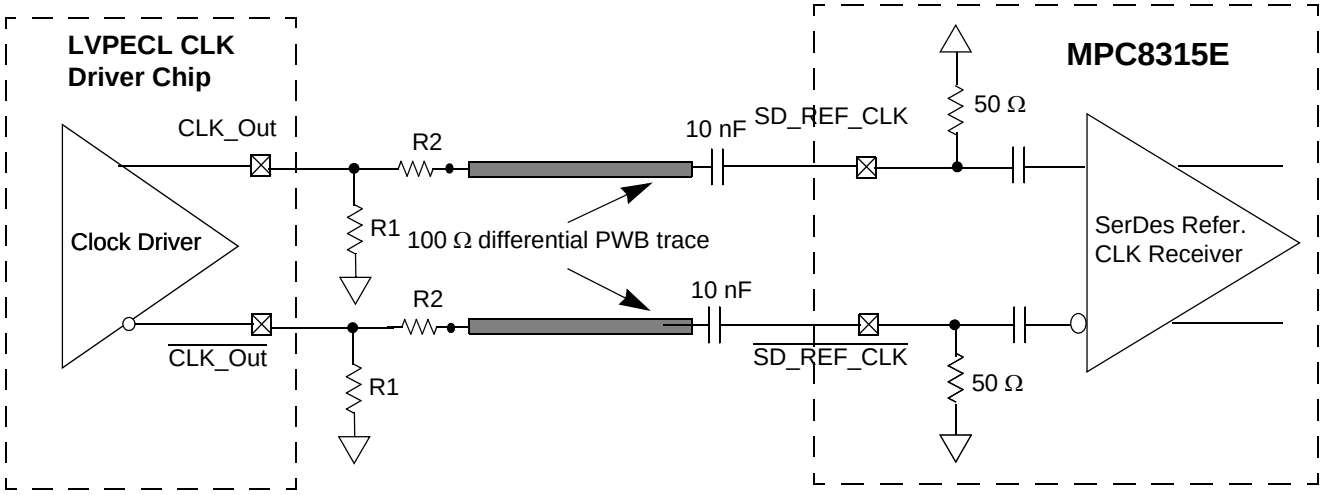

Figure 45. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8315E SerDes reference clock input's DC requirement.

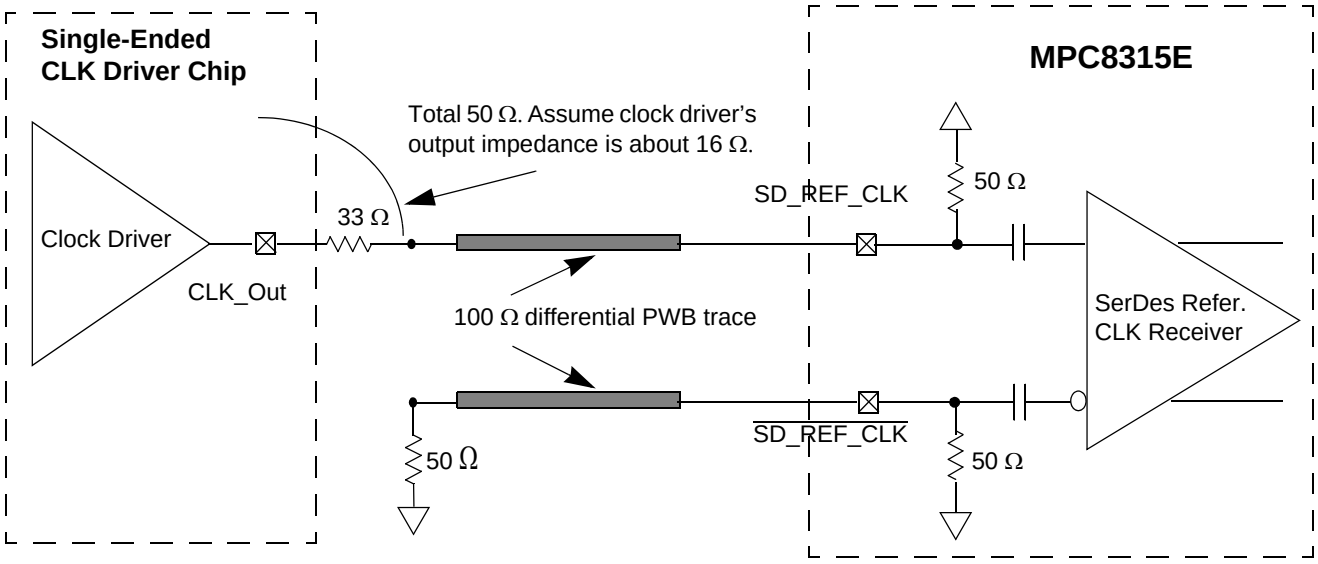

Figure 46. Single-Ended Connection (Reference Only)

17.3 Out-of-Band (OOB) Electrical Characteristics

This table provides the out-of-band (OOB) electrical characteristics for the SATA interface of the MPC8315.

Table 59. Out-of-Band (OOB) Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Note
OOB Signal Detection Threshold 1.5G 3.0G	$V_{SATA\_OOBDETE}$	 50 75	 100 125	 200 200	mVp-p	—
UI During OOB Signaling	T_{SATA_UIOOB}	—	666.67	—	ps	—
COMINIT/ COMRESET and COMWAKE Transmit Burst Length	$T_{SATA\_UIOOBTXB}$	—	160	—	UI	—
COMINIT/ COMRESET Transmit Gap Length	$T_{SATA\_UIOOBTXGap}$	—	480	—	UI	—
COMWAKE Transmit Gap Length	$T_{SATA\_UIOOBTX WakeGap}$	—	160	—	UI	—

18 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8315E.

18.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 60. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le$ NVDD	—	± 5	μA

18.2 Timers AC Timing Specifications

This table provides the timers input and output AC timing specifications.

Table 61. Timers Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

This figure provides the AC test load for the GPIO.

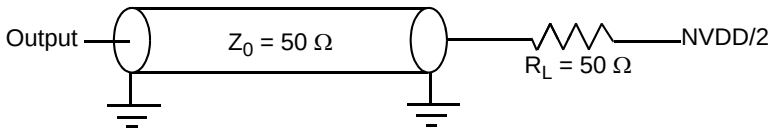

Figure 55. GPIO AC Test Load

20 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8315E.

20.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins.

Table 64. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

20.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 65. IPIC Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Note:

1. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

21 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8315E.

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MEMC_MDM3	AF6	O	GVDD	—
MEMC_MDQS[0]	AF17	I/O	GVDD	—
MEMC_MDQS[1]	AG21	I/O	GVDD	—
MEMC_MDQS[2]	AG9	I/O	GVDD	—
MEMC_MDQS[3]	AF7	I/O	GVDD	—
MEMC_MBA[0]	AH16	O	GVDD	—
MEMC_MBA[1]	AH15	O	GVDD	—
MEMC_MBA[2]	AG15	O	GVDD	—
MEMC_MA0	AD15	O	GVDD	—
MEMC_MA1	AE15	O	GVDD	—
MEMC_MA2	AH14	O	GVDD	—
MEMC_MA3	AG14	O	GVDD	—
MEMC_MA4	AF14	O	GVDD	—
MEMC_MA5	AE14	O	GVDD	—
MEMC_MA6	AH13	O	GVDD	—
MEMC_MA7	AH12	O	GVDD	—
MEMC_MA8	AF13	O	GVDD	—
MEMC_MA9	AD13	O	GVDD	—
MEMC_MA10	AG12	O	GVDD	—
MEMC_MA11	AH11	O	GVDD	—
MEMC_MA12	AH10	O	GVDD	—
MEMC_MA13	AE12	O	GVDD	—
MEMC_MA14	AF11	O	GVDD	—
$\overline{\text{MEMC\_MWE}}$	AE5	O	GVDD	—
$\overline{\text{MEMC\_MRAS}}$	AD7	O	GVDD	—
$\overline{\text{MEMC\_MCAS}}$	AG4	O	GVDD	—
$\overline{\text{MEMC\_MCS}}$[0]	AH3	O	GVDD	—
$\overline{\text{MEMC\_MCS}}$[1]	AD5	O	GVDD	—
MEMC_MCKE	AE4	O	GVDD	3
MEMC_MCK[0]	AF4	O	GVDD	—
$\overline{\text{MEMC\_MCK}}$[0]	AF3	O	GVDD	—
MEMC_MCK[1]	AF1	O	GVDD	—
$\overline{\text{MEMC\_MCK}}$[1]	AE1	O	GVDD	—
MEMC_MODT[0]	AE3	O	GVDD	—
MEMC_MODT[1]	AD4	O	GVDD	—
MEMC_MVREF	AD12	I	GVDD	—

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_REQ0	E18	I/O	$NVDD2_{OFF}$	—
PCI_REQ1/CPCI_HS_ES	C18	I	$NVDD2_{OFF}$	—
PCI_REQ2	E17	I	$NVDD2_{OFF}$	—
PCI_GNT0	B20	I/O	$NVDD2_{OFF}$	—
PCI_GNT1/CPCI_HS_LED	D17	O	$NVDD2_{OFF}$	—
PCI_GNT2/CPCI_HS_ENUM	E15	O	$NVDD2_{OFF}$	—
M66EN	L24	I	$NVDD2_{OFF}$	—
PCI_CLK0	E23	O	$NVDD2_{OFF}$	—
PCI_CLK1	F24	O	$NVDD2_{OFF}$	—
PCI_CLK2	E25	O	$NVDD2_{OFF}$	—
PCI_PME	B23	I/O	$NVDD2_{OFF}$	2
ETSEC1/_USBULPI				
GPIO_24/TSEC1_COL/USBDR_TXDRXD0	J1	I/O	$LVDD1_{OFF}$	—
GPIO_25/TSEC1_CRS/USBDR_TXDRXD1	H1	I/O	$LVDD1_{OFF}$	—
TSEC1_GTX_CLK/USBDR_TXDRXD2	K5	I/O	$LVDD1_{OFF}$	3
TSEC1_RX_CLK/USBDR_TXDRXD3	J4	I/O	$LVDD1_{OFF}$	—
TSCE1_RX_DV/USBDR_TXDRXD4	J2	I/O	$LVDD1_{OFF}$	—
TSEC1_RXD[3]/USBDR_TXDRXD5	G1	I/O	$LVDD1_{OFF}$	—
TSEC1_RXD[2]/USBDR_TXDRXD6	H3	I/O	$LVDD1_{OFF}$	—
TSEC1_RXD[1]/USBDR_TXDRXD7/TSEC_TMR_CLK	J5	I/O	$LVDD1_{OFF}$	—
TSEC1_RXD[0]/USBDR_NXT/TSEC_TMR_TRIG1	H2	I	$LVDD1_{OFF}$	—
TSEC1_RX_ER/USBDR_DIR/TSEC_TMR_TRIG2	H5	I	$LVDD1_{OFF}$	—
TSEC1_TX_CLK/USBDR_CLK	G2	I	$LVDD1_{OFF}$	—
GPIO_28/TSEC1_TXD[3]/TSEC_TMR_GCLK	F3	I/O	$LVDD1_{OFF}$	—
GPIO_29/TSEC1_TXD[2]/TSEC_TMR_PP1	F2	I/O	$LVDD1_{OFF}$	—
GPIO_30/TSEC1_TXD[1]/TSEC_TMR_PP2	F1	I/O	$LVDD1_{OFF}$	—
TSEC1_TXD[0]/USBDR_STP/ TSEC_TMR_PP3	G4	O	$LVDD1_{OFF}$	12
GPIO_31/TSEC1_TX_EN/TSEC_TMR_ALARM1	F4	I/O	$LVDD1_{OFF}$	—
TSEC1_TX_ER/TSEC_TMR_ALARM2	G5	O	$LVDD1_{OFF}$	—
TSEC_GTX_CLK125	D1	I	$NVDD1_{ON}$	—
TSEC_MDC/LB_POR_CFG_BOOT_ECC	E3	I/O	$NVDD1_{ON}$	9
TSEC_MDIO	E2	I/O	$NVDD1_{ON}$	

The primary clock source can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the device is configured as a PCI host device, SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the SYS_CLK_IN signal should be tied to GND.

As shown in Figure 62, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbiu_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{\text{PCI\_SYNC\_IN} \times (1 + \sim \overline{\text{CFG\_SYS\_CLKIN\_DIV}})\} \times \text{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + ~ $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$) is the SYS_CLK_IN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + \text{RCWL[DDRCM]})$$

Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbiu_clk* frequency is determined by the following equation:

$$lbiu\_clk = csb\_clk \times (1 + \text{RCWL[LBCM]})$$

Note that *lbiu_clk* is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LCLK[0:1]). The LBIU clock divider ratio is controlled by LCRR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 71 specifies which units have a configurable clock frequency.

Table 71. Configurable Clock Units

Unit	Default Frequency	Options
eTSEC1	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*
eTSEC2	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*
Security Core, I2C, SAP, TPR	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*
USB DR	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*
PCI and DMA complex	*csb_clk*	Off, *csb_clk*
PCI Express	*csb_clk*	Off, *csb_clk*
Serial ATA	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*

This table provides the operating frequencies for the TEPBGA II under recommended operating conditions (see Table 2).

Table 72. Operating Frequencies for TEPBGA II

Characteristic[1]	Max Operating Frequency	Unit
e300 core frequency (*core_clk*)	400	MHz
Coherent system bus frequency (*csb_clk*)	133	MHz
DDR1/2 memory bus frequency (MCK)[2]	133	MHz
Local bus frequency (LCLK*n*)[3]	66	MHz
PCI input frequency (SYS_CLK_IN or PCI_CLK)	24-66	MHz

Note:
1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK[0:1], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The DDR data rate is 2x the DDR memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the *lbiu_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

24.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 73 shows the multiplication factor encodings for the system PLL.

NOTE

If RCWL[DDRCM] and RCWL[LBCM] are both cleared, the system PLL VCO frequency = (CSB frequency) × (System PLL VCO Divider).

If either RCWL[DDRCM] or RCWL[LBCM] are set, the system PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO Divider).

The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.

25.2 Thermal Management Information

For the following sections, $P_D = (VDD \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers.

25.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity T_J - T_A) are possible.

25.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction to ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JB}$ = junction to board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

25.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

25.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Power and ground connections must be made to all external VDD, GVDD, LVDD, NVDD, and GND pins of the device.

26.5 Output Buffer DC Impedance

The MPC8315E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to NVDD or GND. Then, the value of each resistor is varied until the pad voltage is NVDD/2 (see Figure 64). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals NVDD/2. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

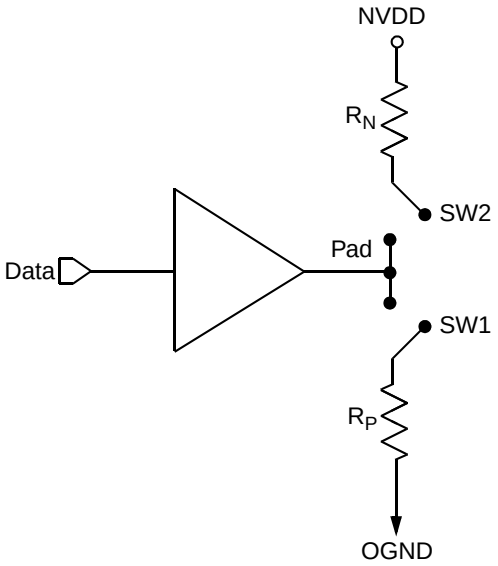

Figure 64. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

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