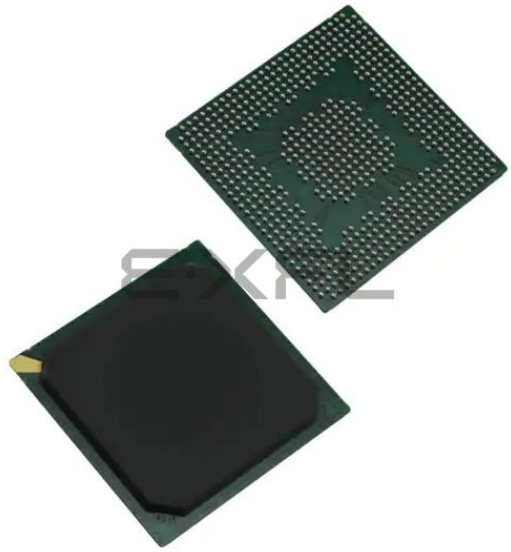

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8315cvragda

  - Combines a True Random Number Generator (TRNG) and a NIST-approved Pseudo-Random Number Generator (PRNG) (as described in Annex C of FIPS140-2 and ANSI X9.62).
- Cyclical Redundancy Check Hardware Accelerator (CRCA)
  - Implements CRC32C as required for iSCSI header and payload checksums, CRC32 as required for IEEE 802 packets, as well as for programmable 32 bit CRC polynomials

2.4 DDR Memory Controller

The DDR1/DDR2 memory controller includes the following features:

- Single 16- or 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 266 MHz data rate
- Support for two physical banks (chip selects), each bank independently addressable
- 64-Mbit to 2-Gbit (for DDR1) and to 4-Gbit (for DDR2) devices with x8/x16 data ports (no direct x4 support)
- Support for one 16-bit device or two 8-bit devices on a 16-bit bus or two 16-bit devices on a 32-bit bus
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

2.5 PCI Controller

The PCI controller includes the following features:

- Designed to comply with *PCI Local Bus Specification Revision 2.3*
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

2.6 TDM Interface

The TDM interface includes the following features:

- Independent receive and transmit with dedicated data, clock and frame sync line
- Separate or shared RCK and TCK whose source can be either internal or external
- Glueless interface to E1/T1 frames and MVIP, SCAS, and H.110 buses
- Up to 128 time slots, where each slot can be programmed to be active or inactive
- 8- or 16-bit word widths
- The TDM Transmitter Sync Signal (TFS), Transmitter Clock Signal (TCK) and Receiver Clock

2.9 Dual Serial ATA (SATA) Controllers

The SATA controllers have the following features:

- Designed to comply with *Serial ATA Rev 2.5 Specification*
- ATAPI 6+
- Spread spectrum clocking on receive
- Asynchronous notification
- Hot plug including asynchronous signal recovery
- Link power management
- Native command queuing
- Staggered spin-up and port multiplier support
- SATA 1.5 and 3.0 Gbps operation
- Interrupt driven
- Power management support
- Error handling and diagnostic features
  - Far end/near end loopback
  - Failed CRC error reporting
  - Increased ALIGN insertion rates
  - Scrambling and CONT override

2.10 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The eTSECs include the following features:

- Two SGMII/RGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Std 802.3™, IEEE 802.3u™, IEEE 802.3x™, IEEE 802.3z™, IEEE 802.3au™, IEEE 802.3ab™, and IEEE Std 1588™
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status.

2.11 Integrated Programmable Interrupt Controller (IPIC)

The integrated programmable interrupt controller (IPIC) provides a flexible solution for general-purpose interrupt control. The IPIC programming model is compatible with the MPC8260 interrupt controller and supports external and internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value[1]	Unit	Status in D3 Warm mode	Note
Dedicated USB ground for USB bias circuit	USB_VSSA_BIAS	0.0	V	—	—
Dedicated power for USB transceiver	USB_VDDA	3.3 ± 300 mv	V	Switched Off	—
Dedicated ground for USB transceiver	USB_VSSA	0.0	V	—	—
SATA digital power	SATA_VDD	1.0 ± 50 mv	V	Switched Off	—
SATA digital ground	SATA_VSS	0.0	V	—	—
SATA analog I/O power	VDD1IO	1.0 ± 50 mv	V	Switched Off	—
SATA analog I/O ground	VSS1IO	0.0	V	—	—
SATA core analog power	VDD1ANA	1.0 ± 50 mv	V	Switched Off	—
SATA analog ground	VSS1ANA	0.0	V	—	—
SATA analog power PLL	VDD33PLL	3.3 ± 165 mv	V	Switched Off	—
SATA 3.3 analog power	VDD33ANA	3.3 ± 165 mv	V	Switched Off	—
SATA reference analog ground	VSSRESREF	0.0	V	—	—
Core supply voltage	VDD	1.0 ± 50 mv	V	Switched Off	—
Core supply voltage	VDDC	1.0 ± 50 mv	V	Switched On	—
Analog power for e300 core APLL	AVDD1	1.0 ± 50 mv	V	Switched Off	6
Analog power for system APLL	AVDD2	1.0 ± 50 mv	V	Switched On	6
DDR and DDR2 DRAM I/O voltage	GVDD	2.5 ± 200 mv 1.8 ± 100 mv	V	Switched Off	—
Differential reference voltage for DDR and DDR2 controller	MVREF	GVDD /2	V	Switched Off	—
Standard I/O voltage	NVDD1_ON	3.3 ± 300 mv	V	Switched On	1
Standard I/O voltage	NVDD2_ON	3.3 ± 300 mv	V	Switched On	1
Standard I/O voltage	NVDD1_OFF	3.3 ± 300 mv	V	Switched Off	2
Standard I/O voltage	NVDD2_OFF	3.3 ± 300 mv	V	Switched Off	2
Standard I/O voltage	NVDD3_OFF	3.3 ± 300 mv	V	Switched Off	2
Standard I/O voltage	NVDD4_OFF	3.3 ± 300 mv	V	Switched Off	2
eTSEC/USBdr I/O supply	LVDD1_OFF	2.5 ± 125 mv 3.3 ± 300 mv	V	Switched Off	—
eTSEC I/O supply	LVDD2_ON	2.5 ± 125 mv 3.3 ± 300 mv	V	Switched On	—
Analog and digital ground	VSS	0.0	V	—	—
Junction temperature range	T_A/T_J	0 to105	°C	—	3

7.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions

Parameter	Symbol [1]	Min	Max	Unit	Note
MCK[n] cycle time at MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	7.5	10	ns	2
ADDR/CMD output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHAS}	 2.9 3.5	 — —	ns	3
ADDR/CMD output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHAX}	 3.15 4.20	 — —	ns	3
$\overline{\text{MCS}}$[n] output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHCS}	 3.15 4.20	 — —	ns	3
$\overline{\text{MCS}}$[n] output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHCX}	 3.15 4.20	 — —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ//MDM output setup with respect to MDQS 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 900 1000	 — —	ps	5
MDQ//MDM output hold with respect to MDQS 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 1100 1200	 — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

This figure provides the AC test load for the DDR bus.

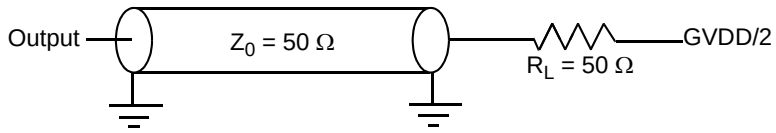


Figure 9. DDR AC Test Load

8 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

8.1 DUART DC Electrical Characteristics

This table lists the DC electrical characteristics for the DUART interface.

Table 21. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2.1	NVDD + 0.3	V
Low-level input voltage NVDD	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	NVDD – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V
Input current (0 V ≤V_{IN} ≤ NVDD)	I_{IN}	—	± 5	μA

8.2 DUART AC Electrical Specifications

This table lists the AC timing parameters for the DUART interface.

Table 22. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Note:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

9 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

Table 28. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load.

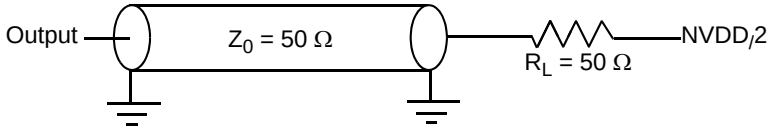


Figure 14. AC Test Load

This figure shows the RMII receive AC timing diagram.

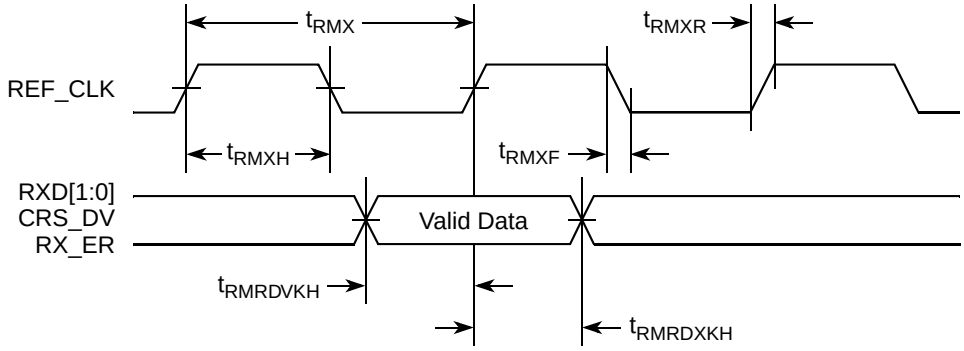


Figure 15. RMII Receive AC Timing Diagram

9.2.3 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 29. RGMII and RTBI AC Timing Specifications

At recommended operating conditions (see Table 2)

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	–0.6	—	0.6	ns
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.6	ns

Table 29. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions (see Table 2)

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Clock cycle duration [3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12} [6]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Note:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the RTBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is LVDD/2.
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention. GTX_CLK supply voltage is fixed at 3.3V inside the chip. If PHY supplies a 2.5 V Clock signal on this input, set TSCOMOBI bit of System I/O configuration register (SICRH) as 1. See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
7. The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm

Table 38. SGMII Receive AC Timing Specifications

At recommended operating conditions with XCOREVDD = 1.0V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal Jitter Tolerance	JSIN	0.1	—	—	UI p-p	1
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1
Bit Error Ratio	BER	—	—	10^{-12}		—
Unit Interval	UI	799.92	800	800.08	ps	2
AC Coupling Capacitor	C_{TX}	5	—	200	nF	3

Note:

1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It's recommended to be placed near the device transmitter outputs.
4. Refer to RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications.

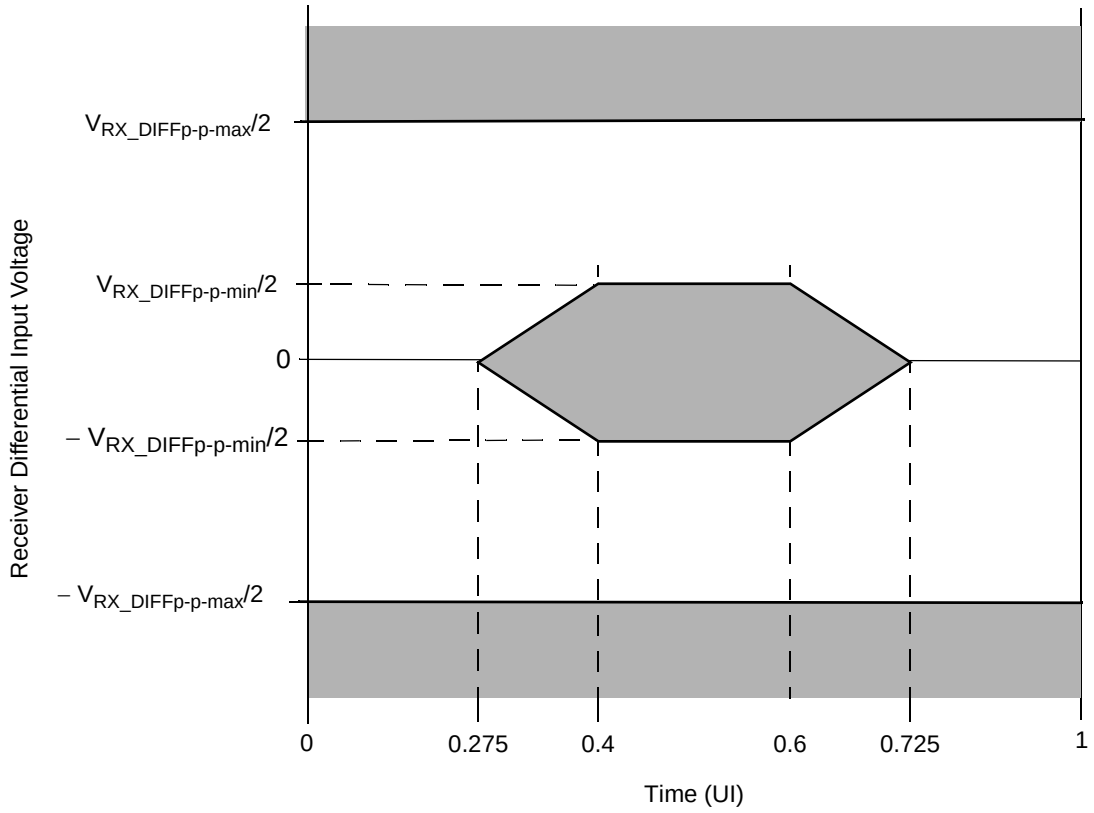


Figure 20. SGMII Receiver Input Compliance Mask

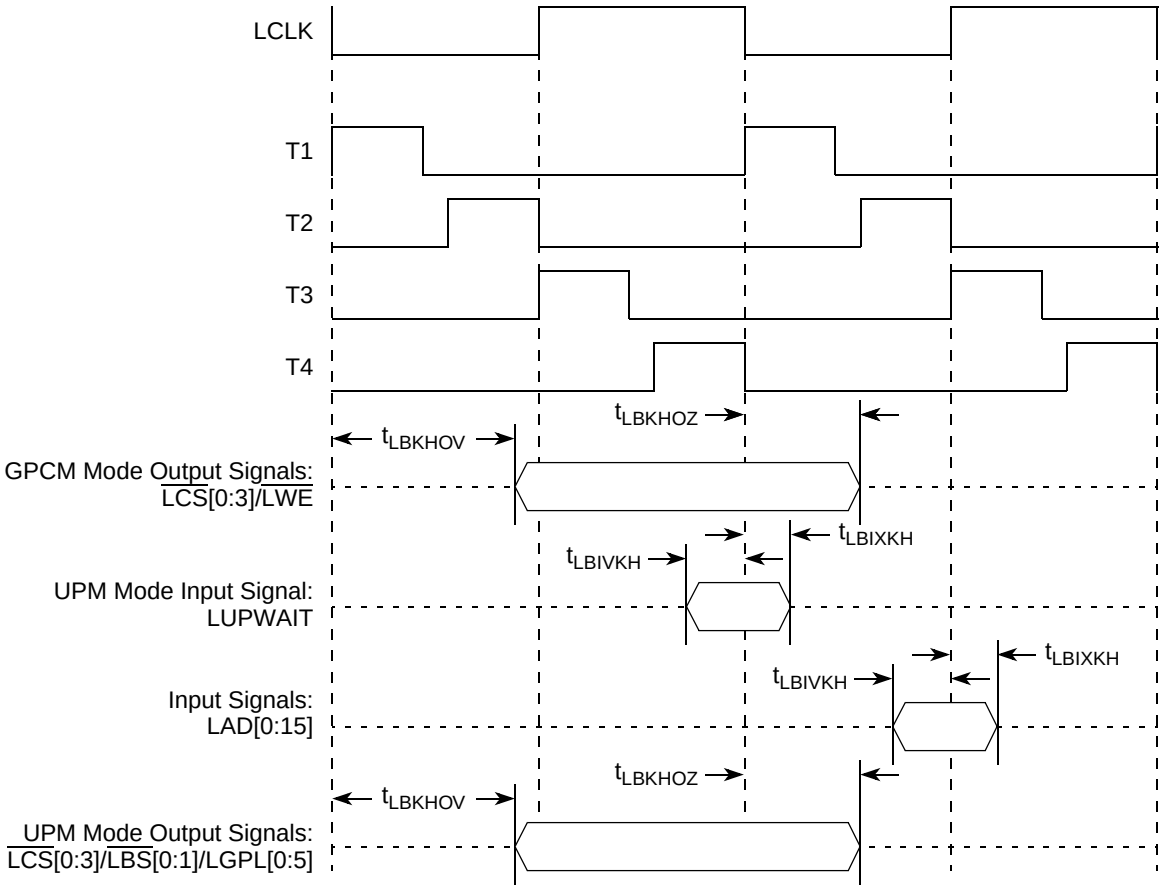


Figure 27. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

12 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface.

12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface.

Table 45. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

13.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interface.

Table 48. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 47)

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0 [2]	 — 0.9 [3]	μs
Fall time of both SDA and SCL signals	t_{I2CF} [4]	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × NVDD	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × NVDD	—	V

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8315E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. MPC8315E does not follow the *I2C-BUS Specifications* version 2.1 regarding the tI2CF AC parameter.

This figure provides the AC test load for the I²C.

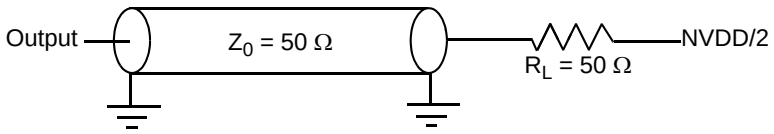


Figure 33. I²C AC Test Load

17.3 Out-of-Band (OOB) Electrical Characteristics

This table provides the out-of-band (OOB) electrical characteristics for the SATA interface of the MPC8315.

Table 59. Out-of-Band (OOB) Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Note
OOB Signal Detection Threshold 1.5G 3.0G	$V_{SATA\_OOBDETE}$	 50 75	 100 125	 200 200	mVp-p	—
UI During OOB Signaling	T_{SATA_UIOOB}	—	666.67	—	ps	—
COMINIT/ COMRESET and COMWAKE Transmit Burst Length	$T_{SATA\_UIOOBTXB}$	—	160	—	UI	—
COMINIT/ COMRESET Transmit Gap Length	$T_{SATA\_UIOOBTXGap}$	—	480	—	UI	—
COMWAKE Transmit Gap Length	$T_{SATA\_UIOOBTX WakeGap}$	—	160	—	UI	—

18 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8315E.

18.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 60. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le$ NVDD	—	± 5	μA

18.2 Timers AC Timing Specifications

This table provides the timers input and output AC timing specifications.

Table 61. Timers Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

This figure provides the AC test load for the GPIO.

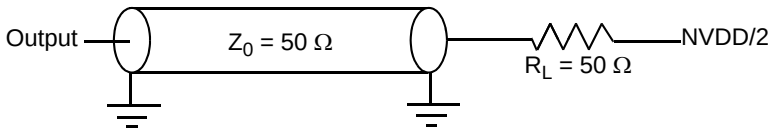


Figure 55. GPIO AC Test Load

20 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8315E.

20.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins.

Table 64. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

20.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 65. IPIC Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Note:

1. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

21 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8315E.

22.2 TDM AC Electrical Characteristics

This table provides the TDM AC timing specifications.

Table 69. TDM AC Timing specifications

Parameter/Condition	Symbol	Min	Max	Unit
TDMxRCK/TDMxTCK	t_{DM}	20.0	—	ns
TDMxRCK/TDMxTCK high pulse width	t_{DM_HIGH}	8.0	—	ns
TDMxRCK/TDMxTCK low pulse width	t_{DM_LOW}	8.0	—	ns
TDMxRCK/TDMxTCK rise time (20% to 80%)	t_{DMKH}	1.0	4.0	ns
TDMxRCK/TDMxTCK fall time (80% to 20%)	t_{DMKL}	1.0	4.0	ns
TDM all input setup time	t_{DMIVKH}	3.0	—	ns
TDMxRD hold time	$t_{DMRDIXKH}$	3.5	—	ns
TDMxTFS/TDMxRFS input hold time	$t_{DMFSIXKH}$	2.0	—	ns
TDMxTCK High to TDMxTD output active	t_{DM_OUTAC}	4.0	—	ns
TDMxTCK High to TDMxTD output valid	$t_{DMTKHOV}$	—	14.0	ns
TDMxTD hold time	$t_{DMTKHOX}$	2.0	—	ns
TDMxTCK High to TDMxTD output high impedance	t_{DM_OUTHI}	—	10.0	ns
TDMxTFS/TDMxRFS output valid	$t_{DMFSKHOV}$	—	13.5	ns
TDMxTFS/TDMxRFS output hold time	$t_{DMFSKHOX}$	2.5	—	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{TDMIVKH}$ symbolizes TDM timing (DM) with respect to the time the input signals (I) reach the valid state (V) relative to the TDM Clock, t_{TC}, reference (K) going to the high (H) state or setup time. Also, output signals (O), hold (X).
2. Output values are based on 30 pF capacitive load.
3. Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. TDMxTCK and TDMxRCK are shown using the rising edge.

This figure shows the TDM receive signal timing.

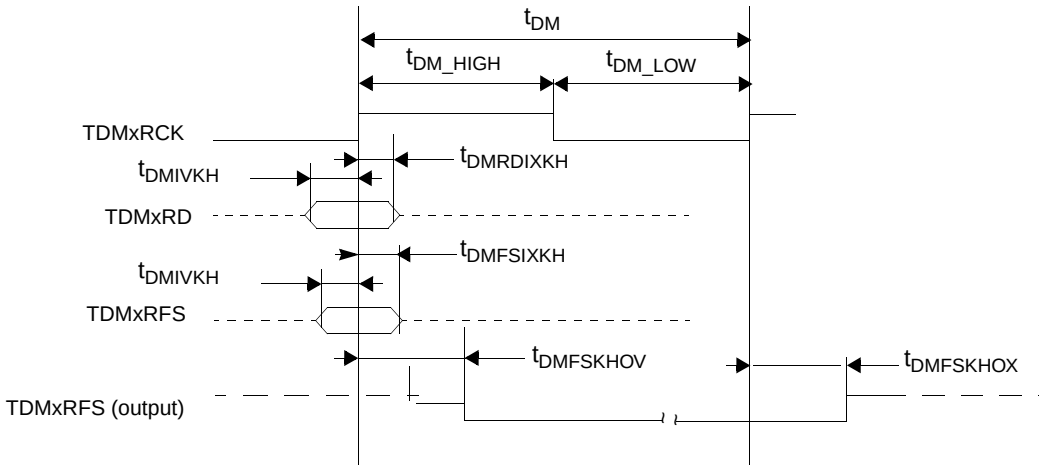
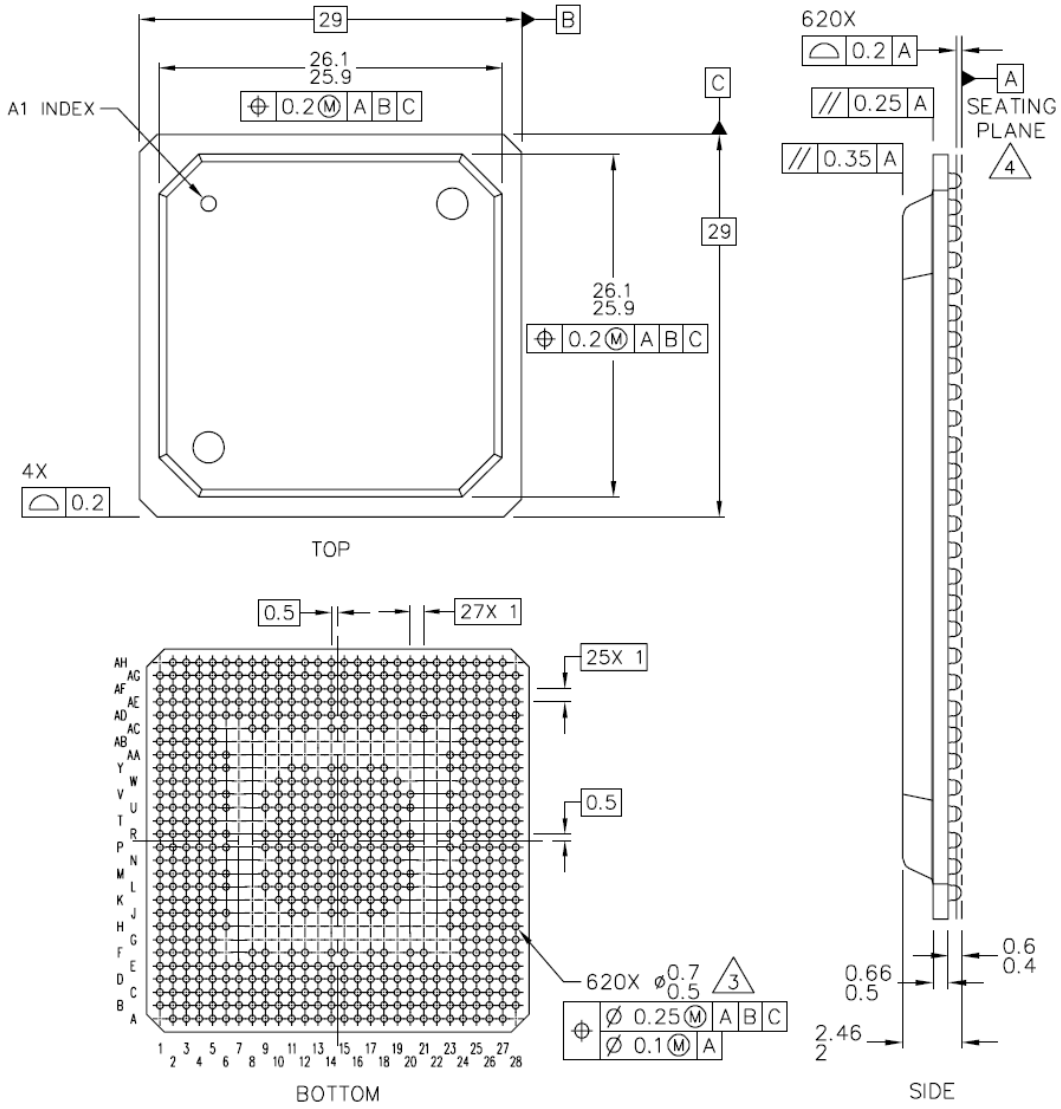


Figure 59. TDM Receive Signals

23.2 Mechanical Dimensions of the TEPBGA II

This figure shows the mechanical dimensions and bottom surface nomenclature of the 620-pin TEPBGA II package.



Notes:
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 61. Mechanical Dimensions and Bottom Surface Nomenclature of the TEPBGA II

23.3 Pinout Listings

This table provides the pin-out listing for the TEPBGA II package.

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
ETSEC2				
GPIO_26/TSEC2_COL	A8	I/O	$LVDD2_{ON}$	—
GPIO_27/TSEC2_CRS	E9	I/O	$LVDD2_{ON}$	—
TSEC2_GTX_CLK	B10	O	$LVDD2_{ON}$	—
TSEC2_RX_CLK	B8	I	$LVDD2_{ON}$	—
TSCE2_RX_DV	C9	I	$LVDD2_{ON}$	—
TSEC2_RXD[3]	C10	I	$LVDD2_{ON}$	—
TSEC2_RXD[2]	D10	I	$LVDD2_{ON}$	—
TSEC2_RXD[1]	A9	I	$LVDD2_{ON}$	—
TSEC2_RXD[0]	B9	I	$LVDD2_{ON}$	—
TSEC2_RX_ER	A10	I	$LVDD2_{ON}$	—
TSEC2_TX_CLK	D8	I	$LVDD2_{ON}$	—
TSEC2_TXD[3]/CFG_RESET_SOURCE[0]	D11	I/O	$LVDD2_{ON}$	—
TSEC2_TXD[2]/CFG_RESET_SOURCE[1]	C7	I/O	$LVDD2_{ON}$	—
TSEC2_TXD[1]/CFG_RESET_SOURCE[2]	E8	I/O	$LVDD2_{ON}$	—
TSEC2_TXD[0]/CFG_RESET_SOURCE[3]	B7	I/O	$LVDD2_{ON}$	—
TSEC2_TX_EN	D12	O	$LVDD2_{ON}$	—
TSEC2_TX_ER	B11	O	$LVDD2_{ON}$	—
SGMII / PCI Express PHY				
TXA	P4	O	XPADVDD	—
$\overline{\text{TXA}}$	N4	O	XPADVDD	—
RXA	R1	I	XCOREVDD	—
$\overline{\text{RXA}}$	P1	I	XCOREVDD	—
TXB	U4	O	XPADVDD	—
$\overline{\text{TXB}}$	V4	O	XPADVDD	—
RXB	U1	I	XCOREVDD	—
$\overline{\text{RXB}}$	V1	I	XCOREVDD	—
SD_IMP_CAL_RX	N3	I	XCOREVDD	—
$\overline{\text{SD\_REF\_CLK}}$	R4	I	XCOREVDD	—
SD_REF_CLK	R5	I	XCOREVDD	—
SD_PLL_TPD	T2	O	—	—
SD_IMP_CAL_TX	V5	I	XPADVDD	—
SDAVDD	T3	I	—	—
SD_PLL_TPA_ANA	T4	O	—	—
SDAVSS	T5	I	—	—
USB Phy				

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
VSS1IO	M24, N24, P19, P20, P25, P27, R25, R27, T24	I	—	—
XCOREVDD	P2, P10, R2, T1	I	—	—
XCOREVSS	R3, R10, U2, V2	I	—	—
XPADVDD	P3, R9, U3	I	—	—
XPADVSS	P5, P9, V3	I	—	—

Note:

1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to NVDD.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to NVDD.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. This pin must always be tied to VSS.
7. Thermal sensitive resistor.
8. This pin should be connected to USB_VSSA_BIAS through 10K precision resistor.
9. The LB_POR_CFG_BOOT_ECC functionality for this pin is only available in MPC8315E revision 1.1 and later. The LB_POR_CFG_BOOT_ECC is sampled only during the $\overline{\text{PORESET}}$ negation. This pin with an internal pull down resistor enables the ECC by default. To disable the ECC an external strong pull up resistor or a tristate buffer is needed.
10. This pin should be connected to an external 2.7 K ±1% resistor connected to VSS. The resistor should be placed as close as possible to the input.
11. This pin has a weak internal pull-down.
12. This pin has a weak internal pull-up.

Table 71. Configurable Clock Units

Unit	Default Frequency	Options
eTSEC1	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*
eTSEC2	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*
Security Core, I2C, SAP, TPR	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*
USB DR	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*
PCI and DMA complex	*csb_clk*	Off, *csb_clk*
PCI Express	*csb_clk*	Off, *csb_clk*
Serial ATA	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*

This table provides the operating frequencies for the TEPBGA II under recommended operating conditions (see Table 2).

Table 72. Operating Frequencies for TEPBGA II

Characteristic[1]	Max Operating Frequency	Unit
e300 core frequency (*core_clk*)	400	MHz
Coherent system bus frequency (*csb_clk*)	133	MHz
DDR1/2 memory bus frequency (MCK)[2]	133	MHz
Local bus frequency (LCLK*n*)[3]	66	MHz
PCI input frequency (SYS_CLK_IN or PCI_CLK)	24-66	MHz

Note:
1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK[0:1], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The DDR data rate is 2x the DDR memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the *lbiu_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

24.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 73 shows the multiplication factor encodings for the system PLL.

NOTE

If RCWL[DDRCM] and RCWL[LBCM] are both cleared, the system PLL VCO frequency = (CSB frequency) × (System PLL VCO Divider).

If either RCWL[DDRCM] or RCWL[LBCM] are set, the system PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO Divider).

The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.

24.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 76 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 76 should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider
VCO divider has to be set properly so that the core VCO frequency is in the range of 400–800 MHz.

Table 76. e300 Core PLL Configuration

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider[1]
0–1	2–5	6		
nn	0000	0	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
11	nnnn	n	N/A	N/A
00	0001	0	1:1	2
01	0001	0	1:1	4
00	0001	1	1.5:1	2
01	0001	1	1.5:1	4
00	0010	0	2:1	2
01	0010	0	2:1	4
00	0010	1	2.5:1	2
01	0010	1	2.5:1	4
00	0011	0	3:1	2
01	0011	0	3:1	4

1 Core VCO frequency = core frequency × VCO divider.

24.3 Suggested PLL Configurations

To simplify the PLL configurations, the MPC8315E might be separated into two clock domains. The first domain contain the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. Table 77 shows suggested PLL configurations for 33, 25, and 66 MHz input clocks.

Table 77. Suggested PLL Configurations

Conf. No.	SPMF	Core\PLL	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)
1	0100	0000100	33.33	133.33	266.66
3	0010	0000100	66.67	133.33	266.66
4	0100	0000101	33.33	133.33	333.33
5	0101	0000101	25	125	312.5

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum VDD, nominal NVDD, 105°C.

Table 80. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI Signals (not including PCI Output Clocks)	PCI Output Clocks (including PCI_SYNC_OUT)	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
R_P	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
Differential	NA	NA	NA	NA	Z_{DIFF}	Ω

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

26.6 Configuration Pin Multiplexing

The MPC8315E provides the user with power-on configuration options that can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{PORESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

26.7 Pull-Up Resistor Requirements

The MPC8315E requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C pins and EPIC interrupt pins.

For more information on required pull up resistors and the connections required for JTAG interface, see AN3438, MPC8315 Design Checklist

27 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 27.1, “Part Numbers Fully Addressed by this Document.”

27.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the MPC8315E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme

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