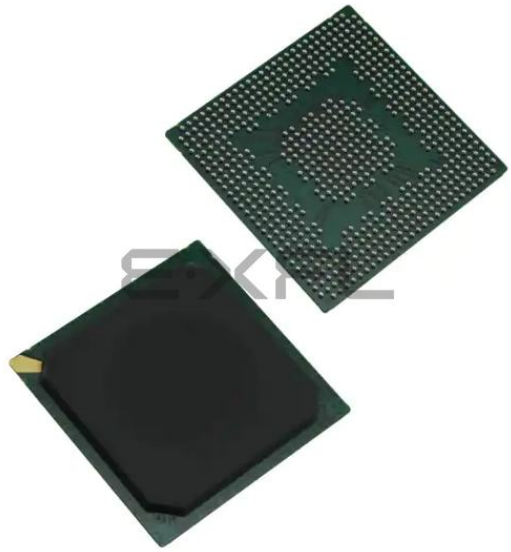

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Security; SEC 3.3
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8315ecvrafda

- Signal (RCK) can be configured as either input or output
- Frame sync and data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock
- Frame sync can be programmed as active low or active high
- Selectable delay (0–3 bits) between the Frame Sync signal and the beginning of the frame
- MSB or LSB first support

2.7 USB Dual-Role Controller

The USB controller includes the following features:

- Designed to comply with *USB Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports UTMI+ low pin interface (ULPI) or on-chip USB-2.0 full-speed/high-speed PHY
- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI PHY

2.8 Dual PCI Express Interfaces

The PCI Express interfaces have the following features:

- PCI Express 1.0a compatible
- x1 link width
- Selectable operation as root complex or endpoint
- Both 32- and 64-bit addressing
- 128-byte maximum payload size
- Support for MSI and INTx interrupt messages
- Virtual channel 0 only
- Selectable Traffic Class
- Full 64-bit decode with 32-bit wide windows
- Dedicated descriptor based DMA engine per interface with separate read and write channels

using a simple handshake protocol. The three user programmable machines (UPMs) can be programmed to interface to synchronous devices or custom ASIC interfaces. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM or UPM controller. Both may exist in the same system. The local bus can operate at up to 66 MHz.

The system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

3 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8315E, which is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but they are included for complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

3.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings [1]

Characteristic		Symbol	Max Value	Unit	Note
Core supply voltage		VDD	–0.3 to 1.26	V	—
PLL supply voltage		AVDD	–0.3 to 1.26	V	—
DDR1 DRAM I/O supply voltage		GVDD	–0.3 to 2.7	V	—
DDR2 DRAM I/O supply voltage		GVDD	–0.3 to 1.9	V	—
PCI, local bus, DUART, system control and power management, I^2C, Ethernet management, 1588 timer and JTAG I/O voltage		NVDD	–0.3 to 3.6	V	7
USB, and eTSEC I/O voltage		LVDD	–0.3 to 2.75 or –0.3 to 3.6	V	6, 8
PHY voltage	USB PHY	USB_PLL_PWR1	–0.3 to 1.26	V	—
		USB_PLL_PWR3, USB_VDDA_BIAS, VDDA	–0.3 to 3.6	V	—
	SERDES PHY	XCOREVDD, XPADVDD, SDAVDD	–0.3 to 1.26	V	—
	SATA PHY	SATA_VDD, VDD1IO, VDD1ANA	–0.3 to 1.26	V	—
		VDD33PLL, VDD33ANA	–0.3 to 3.6	V	—

Table 9. RESET Initialization Timing Specifications (continued)

Note:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the SYS_CLK_IN input, and PCI_SYNC_IN period depends on the value of CFG_SYS_CLKIN_DIV.
2. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN. It is only valid when the device is in PCI host mode.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:3] and CFG_SYS_CLKIN_DIV.
4. The parameter names CFG_SYS_CLKIN_DIV and CFG_CLKIN_DIV are used interchangeably in this document.

This table provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
System PLL lock times	—	100	μs	—
e300 core PLL lock times	—	100	μs	—
SerDes (SGMII/PCI Exp Phy) PLL lock times	—	100	μs	—
USB phy PLL lock times	—	100	μs	—
SATA phy PLL lock times	—	100	μs	—

7 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8315E. Note that DDR SDRAM is GVDD(typ) = 2.5 V and DDR2 SDRAM is GVDD(typ) = 1.8 V.

7.1 DDR and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8315E when GVDD(typ) = 1.8 V.

Table 11. DDR2 SDRAM DC Electrical Characteristics for GVDD(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GVDD	1.7	1.9	V	1
I/O reference voltage	MVREF	0.49 × GVDD	0.51 × GVDD	V	2
I/O termination voltage	V_{TT}	MVREF – 0.04	MVREF + 0.04	V	3
Input high voltage	V_{IH}	MVREF+ 0.125	GVDD + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.420 V, GVDD= 1.7V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	

9.1 eTSEC (10/100/1000 Mbps)—MII/RMII/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all the media-independent interface (MII), reduced gigabit MII (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII and RMII is defined for 3.3 V, while the RGMII, and RTBI can operate at 2.5 V. The RGMII and RTBI follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 9.3, "Ethernet Management Interface Electrical Characteristics."

9.1.1 MII, RMII, RGMII, and RTBI DC Electrical Characteristics

All MII, RMII drivers and receivers comply with the DC parametric attributes specified in Table 23 for 3.3-V operation and RGMII, RTBI drivers and receivers comply with the DC parametric attributes specified in Table 24. The RGMII and RTBI signals are based on a 2.5 V CMOS interface voltage as defined by JEDEC EIA/JESD8–5.

NOTE

eTSEC should be interfaced with peripheral operating at same voltage level.

Table 23. MII/RMII (When Operating at 3.3 V) DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LVDD	—	—	3.0	3.6	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	LVDD = Min	2.40	LVDD + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	LVDD = Min	V_{SS}	0.50	V
Input high voltage	V_{IH}	—	—	2.1	LVDD + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input high current	I_{IH}	V_{IN} [1] = LVDD		—	40	μA
Input low current	I_{IL}	V_{IN} [1] = VSS		–600	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Table 24. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LVDD	—	—	2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LVDD = Min	2.00	LVDD + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LVDD = Min	V_{SS} – 0.3	0.40	V
Input high voltage	V_{IH}	—	LVDD = Min	1.7	LVDD + 0.3	V
Input low voltage	V_{IL}	—	LVDD =Min	–0.3	0.70	V
Input high current	I_{IH}	V_{IN} [1] = LVDD		—	15	μA
Input low current	I_{IL}	V_{IN} [1] = VSS		–15	—	μA

Table 29. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions (see Table 2)

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Clock cycle duration [3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12} [6]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Note:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the RTBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is LVDD/2.
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention. GTX_CLK supply voltage is fixed at 3.3V inside the chip. If PHY supplies a 2.5 V Clock signal on this input, set TSCOMOBI bit of System I/O configuration register (SICRH) as 1. See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
7. The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm

Table 40. USB General Timing Parameters (continued)

Parameter	Symbol [1]	Min	Max	Unit	Note
USB clock to output valid—all outputs	t_{USKHOV}	—	9	ns	1
Output hold from USB clock—all outputs	t_{USKHOX}	1	—	ns	1

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the us clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from NVDD/2 of the rising edge of USB clock to 0.4 × NVDD of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 22 and Figure 23 provide the AC test load and signals for the USB, respectively.

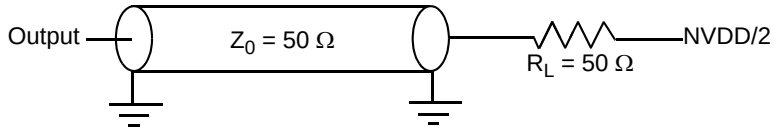

Figure 22. USB AC Test Load

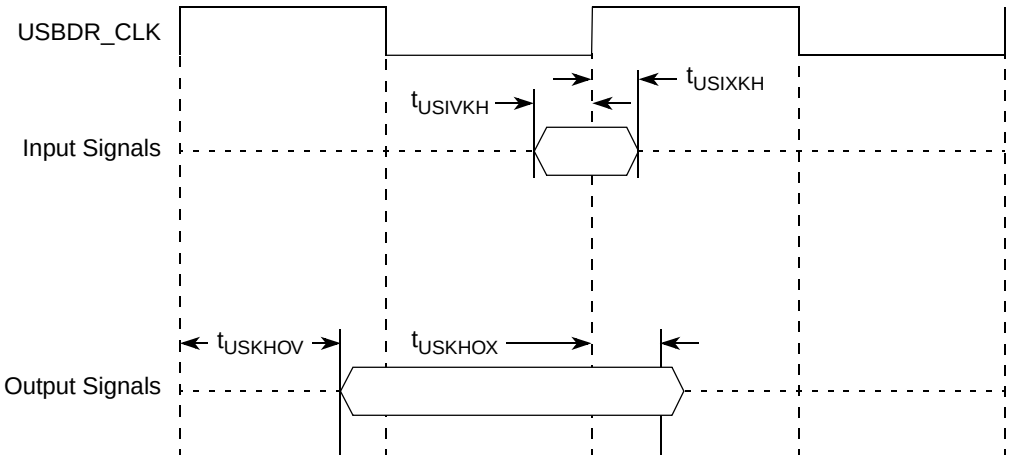

Figure 23. USB Signals

10.2 On-Chip USB PHY

This section provides the AC and DC electrical specifications for the USB PHY interface of the MPC8315E.

For details refer to Tables 7-7 through 7-10, and Table 7-14 in the *USB 2.0 Specifications document*, and the pull-up/down resistors ECN updates, all available at www.usb.org.

This table provides the USB clock input (USB_CLK_IN) DC timing specifications.

12.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface. This table provides the JTAG AC timing specifications as defined in Figure 29 through Figure 32.

Table 46. JTAG AC Timing Specifications (Independent of SYS_CLK_IN) [1]

At recommended operating conditions (see Table 2)

Parameter	Symbol [2]	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5, 6

Note:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Table 28). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

This figure provides the test access port timing diagram.

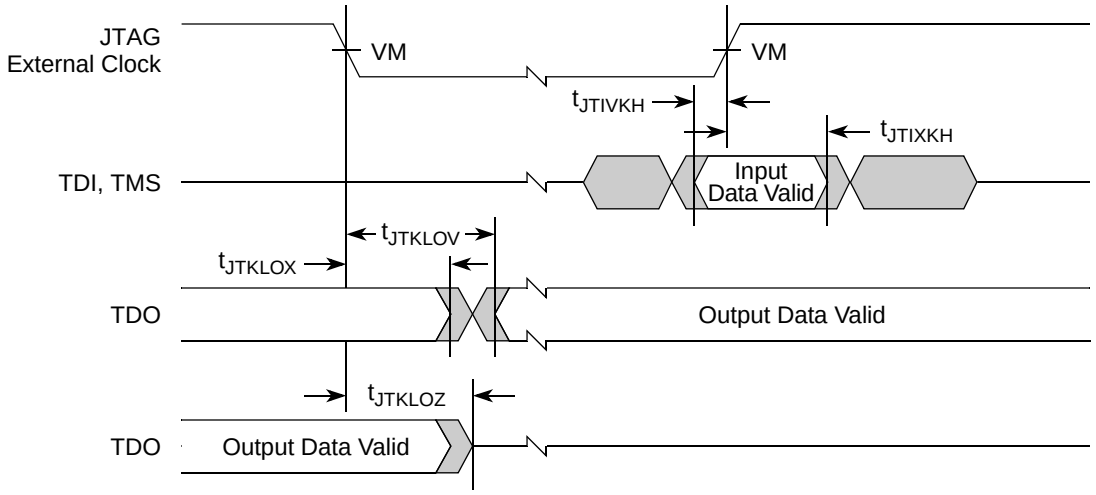

Figure 32. Test Access Port Timing Diagram

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8315E.

13.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interface.

Table 47. I²C DC Electrical Characteristics

At recommended operating conditions with NVDD of 3.3 V ± 300 mv

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage level	V_{IH}	0.7 × NVDD	NVDD + 0.3	V	—
Input low voltage level	V_{IL}	–0.3	0.3 × NVDD	V	—
Low level output voltage	V_{OL}	0	0.2 × NVDD	V	1
High level output voltage	V_{OH}	0.8 × NVDD	NVDD + 0.3	V	—
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	20 + 0.1 × C_B	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current (0 V ≤V_{IN} ≤ NVDD)	I_{IN}	—	± 5	μA	4

Note:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if NVDD is switched off.

15.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15MHz is filtered by the PLL. The most problematic phase noise occurs in the 1-15MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters common to SGMII and PCI Express protocols.

Table 52. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XCOREVDD= 1.0V ± 5%

Parameter	Symbol	Min	Max	Unit	Note
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	+200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{\text{SDn\_REF\_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Note:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from -200 mV to +200 mV on the differential waveform (derived from SDn_REF_CLK minus $\overline{\text{SDn\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 47.
4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for $\overline{\text{SDn\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SDn\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SDn_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SDn\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 48.

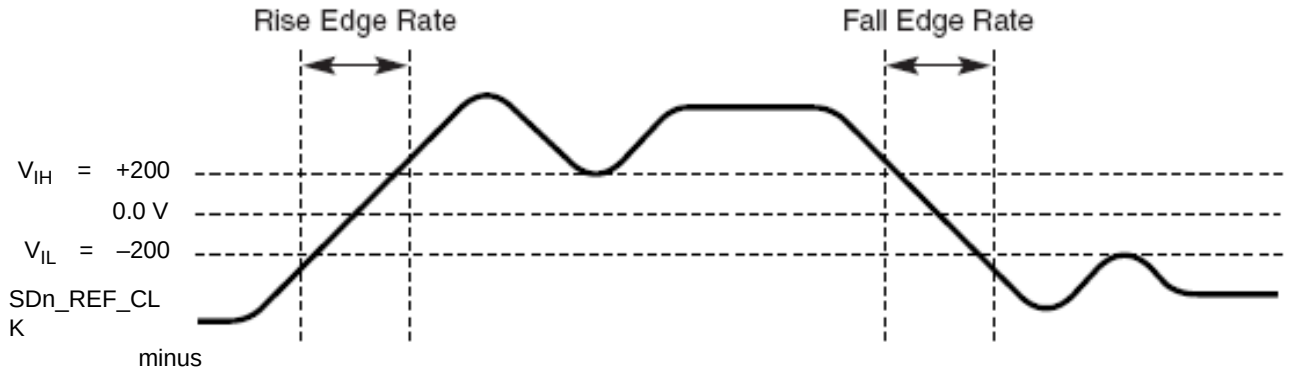

Figure 47. Differential Measurement Points for Rise and Fall Time

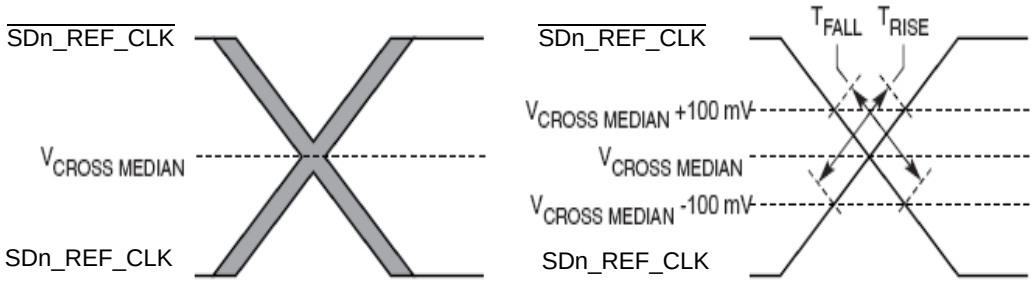

Figure 48. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- Section 9.5.2, “AC Requirements for SGMII SD_REF_CLK and SD_REF_CLK”
- Section 16.2, “AC Requirements for PCI Express SerDes Clocks”

15.2.4.1 Spread Spectrum Clock

SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

15.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane’s transmitter and receiver.

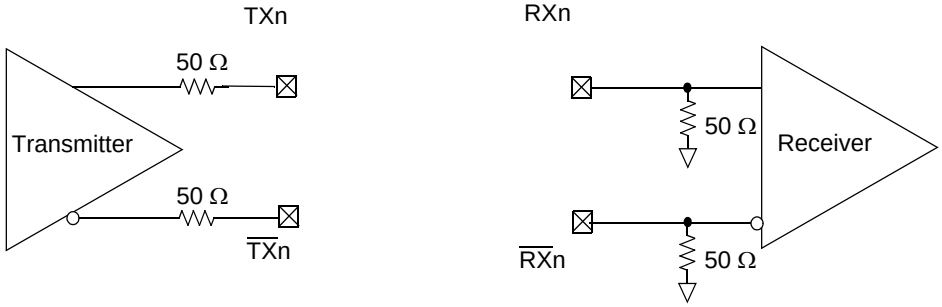

Figure 49. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express or SGMII) in this document based on the application usage:

- Section 9.5, “SGMII Interface Electrical Characteristics”
- Section 16, “PCI Express”

Note that external AC Coupling capacitor is required for the above two serial transmission protocols with the capacitor value defined in specification of each protocol section.

Table 54. Differential Transmitter (TX) Output Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Unit	Note
Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	$T_{TX-IDLE-SET-TO-IDLE}$	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.	—	—	20	UI	—
Maximum time to transition to valid TX specifications after leaving an electrical idle condition	$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle	—	—	20	UI	—
Differential return loss	$RL_{TX-DIFF}$	Measured over 50 MHz to 1.25 GHz.	12	—	—	dB	4
Common mode return loss	RL_{TX-CM}	Measured over 50 MHz to 1.25 GHz.	6	—	—	dB	4
DC differential TX impedance	$Z_{TX-DIFF-DC}$	TX DC Differential mode Low Impedance	80	100	120	Ω	—
Transmitter DC impedance	Z_{TX-DC}	Required TX D+ as well as D- DC Impedance during all states	40	—	—	Ω	—
Lane-to-Lane output skew	$L_{TX-SKEW}$	Static skew between any two Transmitter Lanes within a single Link	—	—	500 + 2 UI	ps	—
AC coupling capacitor	C_{TX}	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.	75	—	200	nF	8
Crosslink random timeout	$T_{crosslink}$	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port.	0	—	1	ms	7

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 52 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 50.)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 52). Note that the series capacitors, C_{TX}, is optional for the return loss measurement.
5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 52 for both V_{TX-D+} and V_{TX-D-}.
6. See Section 4.3.1.8 of the *PCI Express Base Specifications*, Rev 1.0a.
7. See Section 4.2.6.3 of the *PCI Express Base Specifications*, Rev 1.0a.
8. MPC8315E SerDes transmitter does not have C_{TX} built-in. An external AC Coupling capacitor is required

16.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 51 is specified using the passive compliance/test measurement load (see Figure 52) in place of any real PCI Express RX component. In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 52) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 51) expected at the input receiver based on an adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 Ω probes—see Figure 52). Note that the series capacitors, $C_{PEACCTX}$, are optional for the return loss measurement.

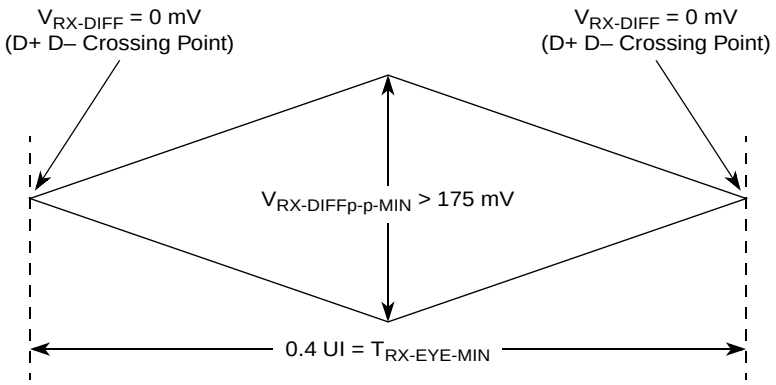

Figure 51. Minimum Receiver Eye Timing and Voltage Compliance Specification

16.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 52.

17.3 Out-of-Band (OOB) Electrical Characteristics

This table provides the out-of-band (OOB) electrical characteristics for the SATA interface of the MPC8315.

Table 59. Out-of-Band (OOB) Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Note
OOB Signal Detection Threshold 1.5G 3.0G	$V_{SATA\_OOBDETE}$	 50 75	 100 125	 200 200	mVp-p	—
UI During OOB Signaling	T_{SATA_UIOOB}	—	666.67	—	ps	—
COMINIT/ COMRESET and COMWAKE Transmit Burst Length	$T_{SATA\_UIOOBTXB}$	—	160	—	UI	—
COMINIT/ COMRESET Transmit Gap Length	$T_{SATA\_UIOOBTXGap}$	—	480	—	UI	—
COMWAKE Transmit Gap Length	$T_{SATA\_UIOOBTX WakeGap}$	—	160	—	UI	—

18 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8315E.

18.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 60. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le$ NVDD	—	± 5	μA

18.2 Timers AC Timing Specifications

This table provides the timers input and output AC timing specifications.

Table 61. Timers Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

This figure shows the TDM transmit signal timing.

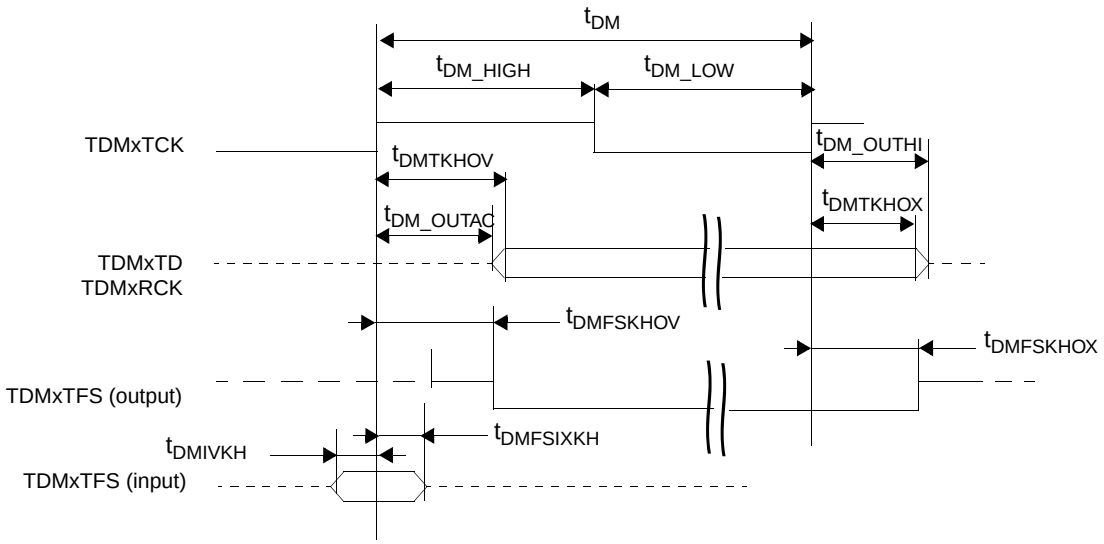

Figure 60. TDM Transmit Signals

23 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8315E is available in a thermally enhanced plastic ball grid array (TEPBGA II), see Section 23.1, "Package Parameters for the MPC8315E TEPBGA II," and Section 23.2, "Mechanical Dimensions of the TEPBGA II," for information on the TEPBGA II.

23.1 Package Parameters for the MPC8315E TEPBGA II

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, TEPBGA II.

Package outline	29 mm × 29 mm
Interconnects	620
Pitch	1 mm
Module height (typical)	2.23 mm
Solder balls	96.5 Sn/3.5 Ag (VR package)
Ball diameter (typical)	0.6 mm

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
ETSEC2				
GPIO_26/TSEC2_COL	A8	I/O	$LVDD2_{ON}$	—
GPIO_27/TSEC2_CRS	E9	I/O	$LVDD2_{ON}$	—
TSEC2_GTX_CLK	B10	O	$LVDD2_{ON}$	—
TSEC2_RX_CLK	B8	I	$LVDD2_{ON}$	—
TSCE2_RX_DV	C9	I	$LVDD2_{ON}$	—
TSEC2_RXD[3]	C10	I	$LVDD2_{ON}$	—
TSEC2_RXD[2]	D10	I	$LVDD2_{ON}$	—
TSEC2_RXD[1]	A9	I	$LVDD2_{ON}$	—
TSEC2_RXD[0]	B9	I	$LVDD2_{ON}$	—
TSEC2_RX_ER	A10	I	$LVDD2_{ON}$	—
TSEC2_TX_CLK	D8	I	$LVDD2_{ON}$	—
TSEC2_TXD[3]/CFG_RESET_SOURCE[0]	D11	I/O	$LVDD2_{ON}$	—
TSEC2_TXD[2]/CFG_RESET_SOURCE[1]	C7	I/O	$LVDD2_{ON}$	—
TSEC2_TXD[1]/CFG_RESET_SOURCE[2]	E8	I/O	$LVDD2_{ON}$	—
TSEC2_TXD[0]/CFG_RESET_SOURCE[3]	B7	I/O	$LVDD2_{ON}$	—
TSEC2_TX_EN	D12	O	$LVDD2_{ON}$	—
TSEC2_TX_ER	B11	O	$LVDD2_{ON}$	—
SGMII / PCI Express PHY				
TXA	P4	O	XPADVDD	—
$\overline{\text{TXA}}$	N4	O	XPADVDD	—
RXA	R1	I	XCOREVDD	—
$\overline{\text{RXA}}$	P1	I	XCOREVDD	—
TXB	U4	O	XPADVDD	—
$\overline{\text{TXB}}$	V4	O	XPADVDD	—
RXB	U1	I	XCOREVDD	—
$\overline{\text{RXB}}$	V1	I	XCOREVDD	—
SD_IMP_CAL_RX	N3	I	XCOREVDD	—
$\overline{\text{SD\_REF\_CLK}}$	R4	I	XCOREVDD	—
SD_REF_CLK	R5	I	XCOREVDD	—
SD_PLL_TPD	T2	O	—	—
SD_IMP_CAL_TX	V5	I	XPADVDD	—
SDAVDD	T3	I	—	—
SD_PLL_TPA_ANA	T4	O	—	—
SDAVSS	T5	I	—	—
USB Phy				

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
Power and Ground Supplies				
GVDD	Y11, Y12, Y14, Y15, Y17, AC8, AC11, AC14, AC17, AD6, AD9, AD17, AE8, AE13, AE19, AF10, AF15, AF21, AG2, AG3, AG8, AG13, AG19, AH2	I	—	—
LVDD1_OFF	H6, J3, L6, L9, M9	I	—	—
LVDD2_ON	C11, D9, E10, F11, J12	I	—	—
NVDD1_OFF	U9, V9, W10, Y4, Y6, AA3, AB4	I	—	—
NVDD1_ON	B1, B2, C1, D5, E7, F5, F9, J11, K10	I	—	—
NVDD2_OFF	B22, B27, C19, E16, F15, F18, F21, F25, H25, J17, J18, J23, L20, M20	I	—	—
NVDD2_ON	L26, N19	I	—	—
NVDD3_OFF	U20, V20, V23, V26, W19, Y18, Y26, AA23, AA25, AC20, AC25, AD23, AE25, AG25, AG27	I	—	—
NVDD4_OFF	K4, L2, M6, N10	I	—	—
VDD	J15, K15, K16, K17, K18, K19, L10, L19, M10, T10, U10, U19, V10, V19, W11, W12, W13, W14, W15, W16, W17, W18	I	—	—
VDD1ANA	P23, R23, T19	I	—	—
VDD1IO	M26, N26, P28, R28	I	—	—
VDDC	J14, K11, K12, K13, K14, M19	I	—	—
VSS	A3, A27, B3, B12, B24, B28, C6, C8, C13, C17, C21, C23, C26, D2, D7, D15, D18, D20, D22, E4, E6, E11, E24, E26, F8, F12, F14, F17, F20, G3, G26, H4, H23, J6, J26, K25, L4, L11, L12, L13, L14, L15, L16, L17, L18, L23, L28, M3, M11, M12, M13, M14, M15, M16, M17, M18, N5, N11, N12, N13, N14, N15, N16, N17, N18, P6, P11, P12, P13, P14, P15, P16, P17, P18, R6, R11, R12, R13, R14, R15, R16, R17, R18, T11, T12, T13, T14, T15, T16, T17, T18, U5, U6, U11, U12, U13, U14, U15, U16, U17, U18, V6, V11, V12, V13, V14, V15, V16, V17, V18, W5, W25, W27, Y2, Y23, AA6, AA27, AB2, AB26, AC5, AC9, AC12, AC18, AC21, AD3, AD14, AD16, AD20, AD26, AE2, AE7, AE11, AE16, AE22, AE24, AF2, AF9, AF12, AF18, AF20, AF23, AF27, AG1, AG5, AG11, AG16, AG22, AG28, AH27	I	—	—
VSS1ANA	P24, R19, R20, R24	I	—	—

The primary clock source can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the device is configured as a PCI host device, SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the SYS_CLK_IN signal should be tied to GND.

As shown in Figure 62, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbiu_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{\text{PCI\_SYNC\_IN} \times (1 + \sim \overline{\text{CFG\_SYS\_CLKIN\_DIV}})\} \times \text{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + ~ $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$) is the SYS_CLK_IN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + \text{RCWL[DDRCM]})$$

Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbiu_clk* frequency is determined by the following equation:

$$lbiu\_clk = csb\_clk \times (1 + \text{RCWL[LBCM]})$$

Note that *lbiu_clk* is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LCLK[0:1]). The LBIU clock divider ratio is controlled by LCRR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 71 specifies which units have a configurable clock frequency.

also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 81. Part Numbering Nomenclature

MPC	8315	E	C	VR	AG	D	A
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range [3]**	**Package [1]**	**e300 Core Frequency [2]**	**DDR Frequency**	**Revision Level**
MPC	8315	Blank = Not included E = included	Blank = 0 to 105°C C = –40 to 105°C	VR= Pb Free TEPBGA II	AD = 266 MHz AF = 333 MHz AG = 400 MHz	D = 266 MHz	Contact local Freescale sales office

Note:
1. See Section 23, “Package and Pin Listings,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by electric may support other maximum core frequencies.
3. Contact your local Freescale field applications engineer (FAE).

This table shows the SVR settings by device and package type.

Table 82. SVR Settings

Device	Package	SVR (Rev 1.0)	SVR (Rev 1.1)	SVR (Rev 1.2)
MPC8315E	TEPBGA II	0x80B4_0010	0x80B4_0011	0x80B4_0012
MPC8315	TEPBGA II	0x80B5_0010	0x80B5_0011	0x80B5_0012

Note:
1. PVR = 8085_0020 for all devices and revisions in this table.

28 Revision History

This table summarizes a revision history for this document.

Table 83. Revision History

Revision	Date	Substantive Change(s)
2	11/2011	• In Table 70: – Corrected Note 11 to pull down. – Note 10 added to RESREF pin. Removed all other instances of Note 10. – Added pull up information.
1	11/2011	• Added Notes 4, 5, 6, and 7 in Table 2. • In Table 6: – Decoupled PCI_CLK and SYS_CLK_IN rise and fall times. – Relaxed maximum rise/fall time of SYS_CLK_IN from 1.2 ns to 4 ns. – Modified Note 2. – Updated SYS_CLK_IN/PCI_CLK frequency from 66 MHz to 66.67 MHz. • Added Note 4 to Table 9. • Added a note stating “eTSEC should be interfaced with peripheral operating at same voltage level.” in Section 9.1.1, “MII, RMII, RGMII, and RTBI DC Electrical Characteristics.” • Added a note in Table 26 stating “The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm." • Added a note in Table 29 stating “The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm • In Table 42, changed min/max values of t_{CLK_TOL} from 0.05 to 0.005. • Added $t_{LALEHOV}$ parameter to Table 44 • Replaced 50 with 50 Ω in Section 16.5, “Receiver Compliance Eye Diagrams.” • In Table 70: – Added Pull up and Pull down information. – Removed Note 2 from TSEC_MDIO. • Removed configuration 2 from Table 77. • Removed Preliminary from Section 25, “Thermal.” • Removed MDIO signal from Section 26.7, “Pull-Up Resistor Requirements” as this signal is not open drain. • Replaced LCCR with LCRR throughout. • Replaced SYS_CLKIN with SYS_CLK_IN throughout. • Replaced all LBIUCM with LBCM. • Replaced all SYS_CR_CLK_IN and SYS_CR_CLK_OUT with SYS_XTAL_IN and SYS_XTAL_OUT, respectively. Replaced all USB_CR_CLK_IN and USB_CR_CLK_OUT with USB_XTAL_IN and USB_XTAL_OUT, respectively. • Added rise/fall time spec for TDM CLK
0	05/2009	Initial public release

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