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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Security; SEC 3.3
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8315ecvragda

- 16-Kbyte instruction cache, 16-Kbyte data cache
- One floating point unit and two integer units
- Software-compatible with the Freescale processor families implementing the PowerPC Architecture
- Performance monitor

2.2 Serial Interfaces

The following interfaces are supported in the MPC8315E.

- Two enhanced TSECs (eTSECs)
- Two Ethernet interfaces using one RGMII/MII/RMII/RTBI or SGMII (no GMII)
- Dual UART, one I^2C, and one SPI interface

2.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, 802.11i, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are:

- Public key execution unit (PKEU)
  - RSA and Diffie-Hellman (to 4096 bits)
  - Programmable field size up to 2048 bits
  - Elliptic curve cryptography (1023 bits)
  - F2m and F(p) modes
  - Programmable field size up to 511 bits
- Data encryption standard execution unit (DEU)
  - DES, 3DES
  - Two key (K1, K2) or three key (K1, K2, K3)
  - ECB, CBC, CFB-64 and OFB-64 modes for both DES and 3DES
- Advanced encryption standard unit (AESU)
  - Implements the Rinjdael symmetric key cipher
  - Key lengths of 128, 192, and 256 bits
  - ECB, CBC, CCM, CTR, GCM, CMAC, OFB, CFB, XCBC-MAC and LRW modes
  - XOR acceleration
- Message digest execution unit (MDEU)
  - SHA with 160-bit, 256-bit, 384-bit and 512-bit message digest
  - SHA-384/512
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- Random number generator (RNG)

- Signal (RCK) can be configured as either input or output
- Frame sync and data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock
- Frame sync can be programmed as active low or active high
- Selectable delay (0–3 bits) between the Frame Sync signal and the beginning of the frame
- MSB or LSB first support

2.7 USB Dual-Role Controller

The USB controller includes the following features:

- Designed to comply with *USB Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports UTMI+ low pin interface (ULPI) or on-chip USB-2.0 full-speed/high-speed PHY
- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI PHY

2.8 Dual PCI Express Interfaces

The PCI Express interfaces have the following features:

- PCI Express 1.0a compatible
- x1 link width
- Selectable operation as root complex or endpoint
- Both 32- and 64-bit addressing
- 128-byte maximum payload size
- Support for MSI and INTx interrupt messages
- Virtual channel 0 only
- Selectable Traffic Class
- Full 64-bit decode with 32-bit wide windows
- Dedicated descriptor based DMA engine per interface with separate read and write channels

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GVDD + 0.3)	V	2, 4
	DDR DRAM reference	MVREF	–0.3 to (GVDD + 0.3)	V	2, 4
	eTSEC signals	LV_{IN}	–0.3 to (LVDD + 0.3)	V	3, 4
	Local bus, DUART, SYS_CLK_IN, system control and power management, I^2C, and JTAG signals	NV_{IN}	–0.3 to (NVDD + 0.3)	V	3, 4
	PCI	NV_{IN}	–0.3 to (NVDD + 0.3)	V	5
	SATA_CLKIN	NV_{IN}	–0.3 to (NVDD + 0.3)	V	3, 4
Storage temperature range		T_{STG}	–55 to150	°C	—

Note:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** (N,L)V_{IN} must not exceed (N,L)VDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. (M,N,L)V_{IN} and MVREF may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
5. NV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 2.
6. The max value of supply voltage should be selected based on the RGMII mode.
7. NVDD means NVDD1_OFF, NVDD1_ON, NVDD2_OFF, NVDD2_ON, NVDD3_OFF, NVDD4_OFF
8. LVDD means LVDD1_OFF and LVDD2_ON

3.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for theMPC8315E. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value[1]	Unit	Status in D3 Warm mode	Note
SerDes internal digital power	XCOREVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes internal digital power	XCOREVSS	0.0	V	—	—
SerDes I/O digital power	XPADVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes I/O digital power	XPADVSS	0.0	V	—	—
SerDes analog power for PLL	SDAVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes analog power for PLL	SDAVSS	0.0	V	—	—
Dedicated 3.3 V analog power for USB PLL	USB_PLL_PWR3	3.3 ± 165mv	V	Switched Off	—
Dedicated 1.0 Vanalog power for USB PLL	USB_PLL_PWR1	1.0 ± 50 mv	V	Switched Off	—
Dedicated analog ground for USB PLL	USB_PLL_GND	0.0	V	—	—
Dedicated USB power for USB bias circuit	USB_VDDA_BIAS	3.3 ± 300 mv	V	Switched Off	—

Table 3. Output Drive Capability (continued)

Driver Type	Output Impedance (Ω)	Supply Voltage
DUART, system control, I^2C, JTAG,SPI	42	NVDD = 3.3 V
GPIO signals	42	NVDD = 3.3 V
eTSEC	42	LVDD = 3.3 V / 2.5 V

1 Output Impedance can also be adjusted through configurable options in DDR Control Driver Register (DDRCDR). See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.

3.2 Power Sequencing

The MPC8315E does not require the core supply voltage (VDD and VDDC) and I/O supply voltages (GVDD, LVDDx_ON, LVDDx_OFF, NVDDx_ON and NVDDx_OFF) to be applied in any particular order. During the power ramp up, before the power supplies are stable, if the I/O voltages are supplied before the core voltage, there may be a period of time when all input and output pins be actively driven and cause contention and/or excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the continuous core voltage (VDDC) before the continuous I/O voltages (LVDDx_ON and NVDDx_ON) and switchable core voltage (VDD) before the switchable I/O voltages (GVDD, LVDDx_OFF, and NVDDx_OFF). PORESET should be asserted before the continuous power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V, see Figure 3. Once all the power supplies are stable, wait for a minimum of 32 clock cycles before negating PORESET.

The I/O power supply ramp-up slew rate should be slower than 4V/100 μs, this requirement is for ESD circuit.

This figure shows the power-up sequencing for switchable and continuous supplies.

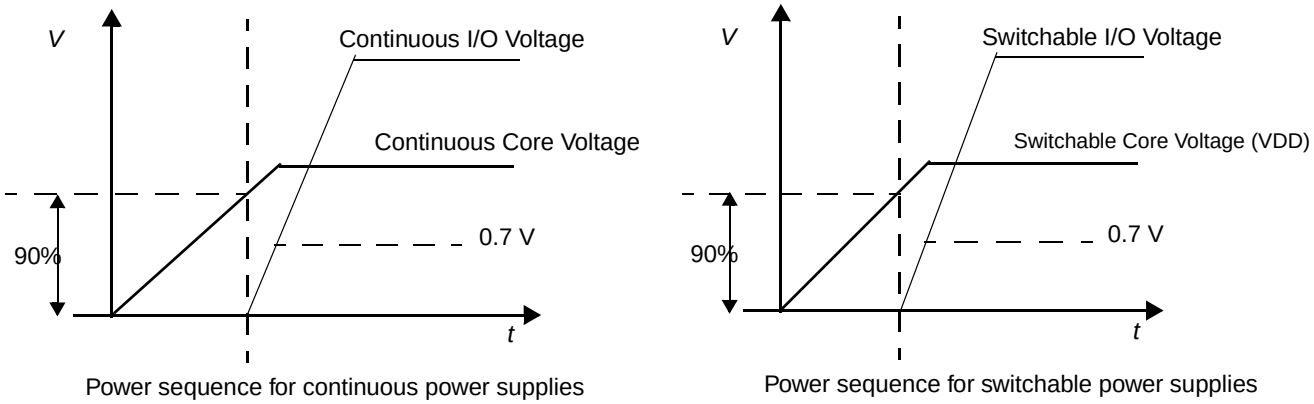


Figure 3. Power-Up Sequencing

When switching from normal mode to D3 warm (standby) mode, first turn off the switchable I/O voltage supply and then turn off the switchable core voltage supply. Similarly, when switching from D3 warm (standby) mode to normal mode, first turn on the switchable core voltage supply and then turn on the switchable I/O voltage supply.

Table 5. MPC8315E Power Dissipation (continued)

Interface	Frequency	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	NV_{DD} (3.3 V)	LVDD1_OFF/ LVDD2_ON (3.3V)	LVDD2 _ON (3.3V)	VDD33PLL, VDD33ANA (3.3V)	SATA_VDD, VDD1IO, VDD1ANA (1.0V)	XCOREVDD, XPADVDD, SDAVDD (1.0V)	Unit
DDR 2 Rs = 22Ω Rt = 75Ω	266MHz, 32 bits	0.246	—	—	—	—	—	—	—	W
	200MHz, 32bits	0.225	—	—	—	—	—	—	—	W
PCI I/O load = 50pF	33 MHz	—	—	0.120	—	—	—	—	—	W
	66 MHz	—	—	0.249	—	—	—	—	—	W
Local bus I/O load = 20pF	66 MHz	—	—	—	—	0.056	—	—	—	W
	50 MHz	—	—	—	—	0.040	—	—	—	W
eTSEC I/O load = 20pF Multiple by number of interface used	MII, 25MHz	—	—	—	0.008	—	—	—	—	W
	RGMII, 125MHz (3.3V)	—	—	—	0.078	—	—	—	—	W
	RGMII, 125MHz (2.5V)	—	—	—	0.044	—	—	—	—	W
USBDR Controller (ULPI mode) load =20pF	60 MHz	—	—	—	0.078	—	—	—	—	W
USBDR+ Internal PHY (UTMI mode)	480 MHz	—	—	—	0.274	—	—	—	—	W
PCI Express two x1lane	2.5 GHz	—	—	—	—	—	—	—	0.190	W
SATA two ports	3.0 GHz	—	—	—	—	—	0.021	0.206	—	W
Other I/O	—	—	—	0.015	—	—	—	—	—	W

5 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8315E.

5.1 DC Electrical Characteristics

This table provides the clock input (SYS_CLK_IN/PCI_SYNC_IN) DC timing specifications for the MPC8315E.

Table 6. SYS_CLK_IN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	NVDD + 0.3	V
Input low voltage	—	V_{IL}	-0.3	0.4	V
SYS_CLK_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
SYS_XTAL_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±40	μA
PCI_SYNC_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
RTC_CLK input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
USB_CLK_IN input current	0 V ≤ V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
USB_XTAL_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±40	μA
SATA_CLK_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA

5.2 AC Electrical Characteristics

The primary clock source for the MPC8315E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (SYS_CLK_IN/PCI_CLK) AC timing specifications for the MPC8315E.

Table 7. SYS_CLK_IN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
SYS_CLK_IN/PCI_CLK frequency	$f_{SYS\_CLK\_IN}$	24	—	66.67	MHz	1, 6, 7
SYS_CLK_IN/PCI_CLK cycle time	$t_{SYS\_CLK\_IN}$	15	—	41.6	ns	6
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	0.6	—	4	ns	2, 6
PCI_CLK rise and fall time	t_{PCH}, t_{PCL}	0.6	0.8	1.2	ns	2
SYS_CLK_IN/PCI_CLK duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3, 6
SYS_CLK_IN/PCI_CLK jitter	—	—	—	±150	ps	4, 5, 6

Note:

1. **Caution:** The system, core, and security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN/PCI_CLK are specified at 20% to 80% of signal swing.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
6. The parameter names PCI_CLK and PCI_SYNC_IN are used interchangeably in this document.
7. Spread spectrum is allowed up to 1% down-spread at 33kHz.(max. rate).

6 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8315E.

6.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins of the MPC8315E.

Table 8. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le$ NVDD	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

6.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications of the MPC8315E.

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to SYS_CLK_IN when the device is in PCI host mode	32	—	$t_{SYS\_CLK\_IN}$	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the device is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3] and $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	$t_{SYS\_CLK\_IN}$	2, 4
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3] and $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to turn on POR config signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Table 14. DDR SDRAM Capacitance for GVDD(typ) = 2.5 V Interface

Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GVDD = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF}.

Table 15. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

7.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

7.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

This table lists the input AC timing specifications for the DDR2 SDRAM (GVDD(typ) = 1.8 V).

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GVDD of 1.8V ± 100 mV

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MVREF – 0.45	V	—
AC input high voltage	V_{IH}	MVREF + 0.45	—	V	—

This table lists the input AC timing specifications for the DDR SDRAM when GVDD(typ)=2.5 V.

Table 17. DDR SDRAM Input AC Timing Specifications for 2.5 V Interface

At recommended operating conditions with GVDD of 2.5V ± 200 mV

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MVREF – 0.51	V	
AC input high voltage	V_{IH}	MVREF + 0.51	—	V	

The following two tables list the input AC timing specifications for the DDR SDRAM interface.

Table 18. DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with GVDD of (1.8 V± 100 mV)

Parameter	Symbol	Min	Max	Unit	Note
Controller Skew for MDQS—MDQ 266 MHz 200 MHz	t_{CISKEW}	 –875 –1250	 875 1250	ps	1, 2, 3

9.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

9.2.2.1 RMII Transmit AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications. This table provides the RMII transmit AC timing specifications.

Table 27. RMII Transmit AC Timing Specifications

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	10	ns
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

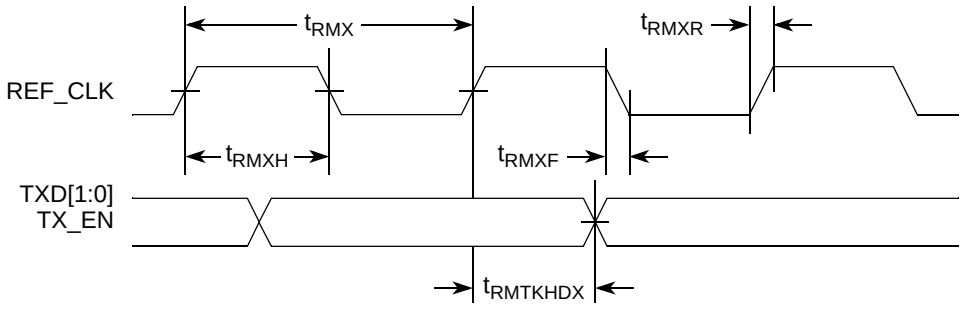


Figure 13. RMII Transmit AC Timing Diagram

9.2.2.2 RMII Receive AC Timing Specifications

This table provides the RMII receive AC timing specifications.

Table 28. RMII Receive AC Timing Specifications

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%

Table 28. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load.

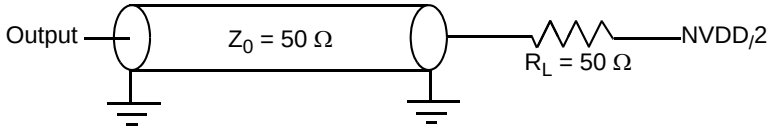


Figure 14. AC Test Load

This figure shows the RMII receive AC timing diagram.

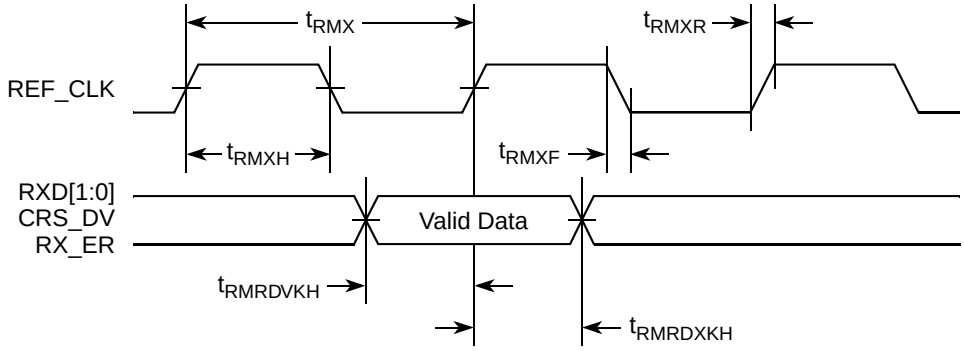


Figure 15. RMII Receive AC Timing Diagram

9.2.3 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 29. RGMII and RTBI AC Timing Specifications

At recommended operating conditions (see Table 2)

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	–0.6	—	0.6	ns
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.6	ns

Table 38. SGMII Receive AC Timing Specifications

At recommended operating conditions with XCOREVDD = 1.0V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal Jitter Tolerance	JSIN	0.1	—	—	UI p-p	1
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1
Bit Error Ratio	BER	—	—	10^{-12}		—
Unit Interval	UI	799.92	800	800.08	ps	2
AC Coupling Capacitor	C_{TX}	5	—	200	nF	3

Note:

1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It's recommended to be placed near the device transmitter outputs.
4. Refer to RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications.

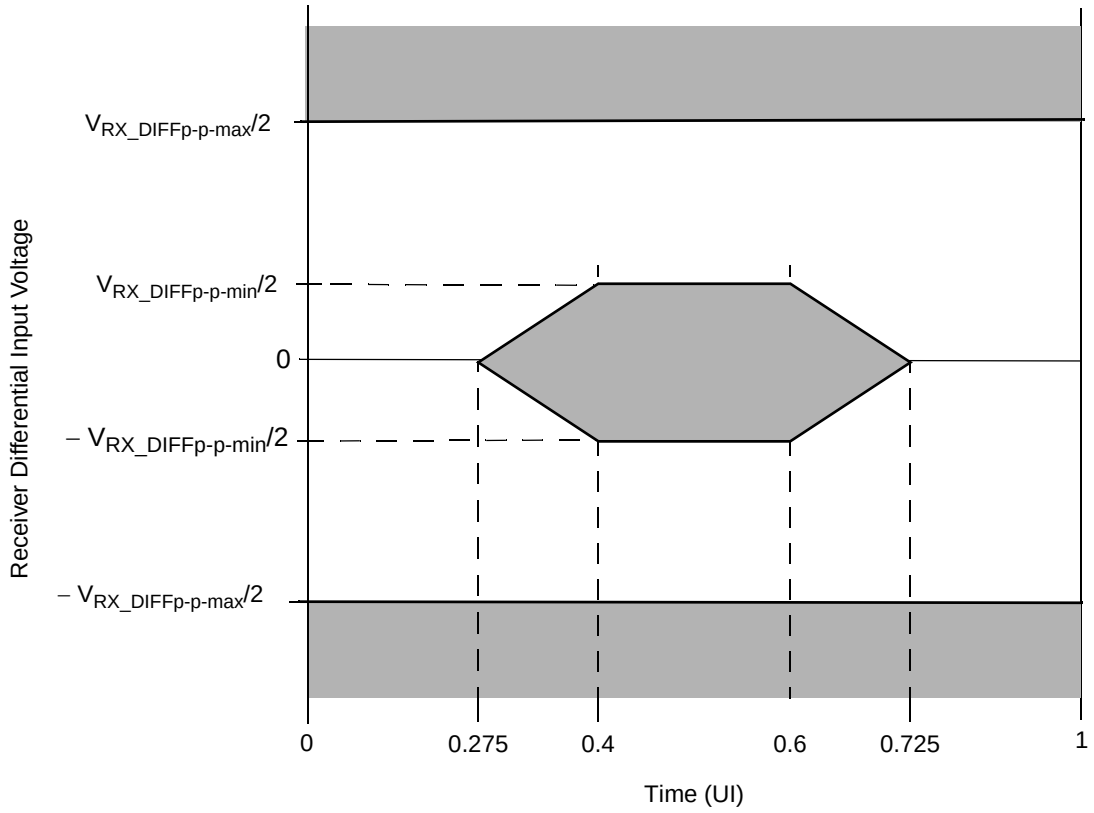


Figure 20. SGMII Receiver Input Compliance Mask

12.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface. This table provides the JTAG AC timing specifications as defined in Figure 29 through Figure 32.

Table 46. JTAG AC Timing Specifications (Independent of SYS_CLK_IN) [1]

At recommended operating conditions (see Table 2)

Parameter	Symbol [2]	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5, 6

Note:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Table 28). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

This figure provides the test access port timing diagram.

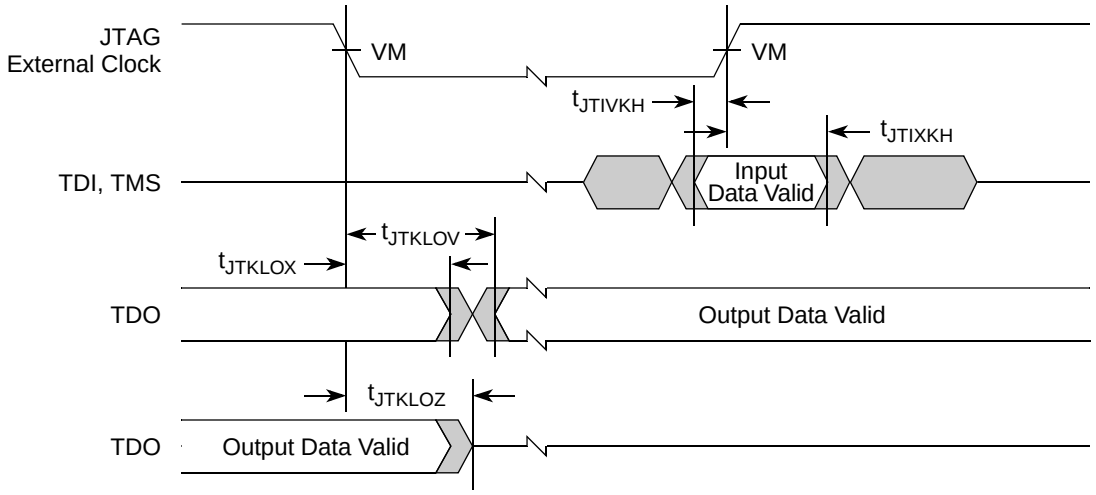


Figure 32. Test Access Port Timing Diagram

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8315E.

13.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interface.

Table 47. I²C DC Electrical Characteristics

At recommended operating conditions with NVDD of 3.3 V ± 300 mv

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage level	V_{IH}	0.7 × NVDD	NVDD + 0.3	V	—
Input low voltage level	V_{IL}	–0.3	0.3 × NVDD	V	—
Low level output voltage	V_{OL}	0	0.2 × NVDD	V	1
High level output voltage	V_{OH}	0.8 × NVDD	NVDD + 0.3	V	—
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	20 + 0.1 × C_B	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current (0 V ≤V_{IN} ≤ NVDD)	I_{IN}	—	± 5	μA	4

Note:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if NVDD is switched off.

Table 55. Differential Receiver (RX) Input Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Unit	Note
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power.	200 k	—	—	Ω	6
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	V_{PEEIDT} = 2*|V_{RX-D+} -V_{RX-D-}| Measured at the package pins of the Receiver	65	—	175	mV	—
Unexpected Electrical Idle Enter Detect Threshold Integration Time	$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	An unexpected Electrical Idle (Vrx-diffp-p < Vrx-idle-det-diffp-p) must be recognized no longer than Trx-idle-det-diff-entertime to signal an unexpected idle condition.	—	—	10	ms	—
Total Skew	$L_{RX-SKEW}$	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (e.g. COM and one to five SKP Symbols) at the RX as well as any delay differences arising from the interconnect itself.	—	—	20	ns	—

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 52 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 51). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 52). Note that the series capacitors, C_{TX}, is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
6. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

Table 56. Reference Clock Input Requirements (continued)

Parameter	Symbol	Conditions	Min	Typical	Max	Unit	Note
Total reference clock jitter, phase noise integration from 100 Hz to 3 MHz	t_{CLK_PJ}	peak to peak jitter at refClk input	—	—	100	ps	—

Note:
1. Only 50/75/100/125/150 MHz have been tested, other in between values will not work correctly with the rest of the system.

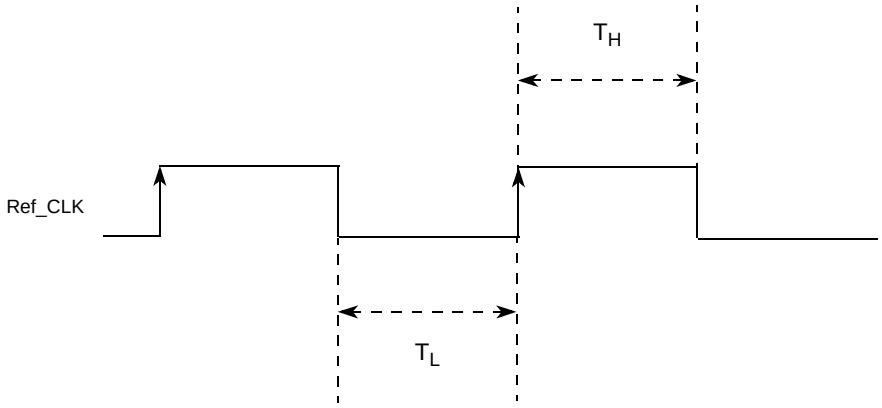


Figure 53. Reference Clock Timing Waveform

17.2 SATA AC Electrical Characteristics

This table provides the general AC parameters for the SATA interface.

Table 57. SATA AC Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Note
Channel Speed 1.5G 3.0G	t_{CH_SPEED}	—	 1.5 3.0	—	Gbps	—
Unit Interval 1.5G 3.0G	T_{UI}	—	 666.4333 333.3333	—	ps	—

This figure provides the AC test load for the GPIO.

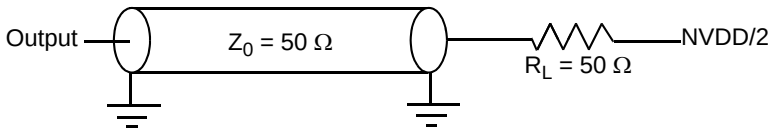


Figure 55. GPIO AC Test Load

20 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8315E.

20.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins.

Table 64. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

20.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 65. IPIC Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Note:

1. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

21 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8315E.

22.2 TDM AC Electrical Characteristics

This table provides the TDM AC timing specifications.

Table 69. TDM AC Timing specifications

Parameter/Condition	Symbol	Min	Max	Unit
TDMxRCK/TDMxTCK	t_{DM}	20.0	—	ns
TDMxRCK/TDMxTCK high pulse width	t_{DM_HIGH}	8.0	—	ns
TDMxRCK/TDMxTCK low pulse width	t_{DM_LOW}	8.0	—	ns
TDMxRCK/TDMxTCK rise time (20% to 80%)	t_{DMKH}	1.0	4.0	ns
TDMxRCK/TDMxTCK fall time (80% to 20%)	t_{DMKL}	1.0	4.0	ns
TDM all input setup time	t_{DMIVKH}	3.0	—	ns
TDMxRD hold time	$t_{DMRDIXKH}$	3.5	—	ns
TDMxTFS/TDMxRFS input hold time	$t_{DMFSIXKH}$	2.0	—	ns
TDMxTCK High to TDMxTD output active	t_{DM_OUTAC}	4.0	—	ns
TDMxTCK High to TDMxTD output valid	$t_{DMTKHOV}$	—	14.0	ns
TDMxTD hold time	$t_{DMTKHOX}$	2.0	—	ns
TDMxTCK High to TDMxTD output high impedance	t_{DM_OUTHI}	—	10.0	ns
TDMxTFS/TDMxRFS output valid	$t_{DMFSKHOV}$	—	13.5	ns
TDMxTFS/TDMxRFS output hold time	$t_{DMFSKHOX}$	2.5	—	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{TDMIVKH}$ symbolizes TDM timing (DM) with respect to the time the input signals (I) reach the valid state (V) relative to the TDM Clock, t_{TC}, reference (K) going to the high (H) state or setup time. Also, output signals (O), hold (X).
2. Output values are based on 30 pF capacitive load.
3. Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. TDMxTCK and TDMxRCK are shown using the rising edge.

This figure shows the TDM receive signal timing.

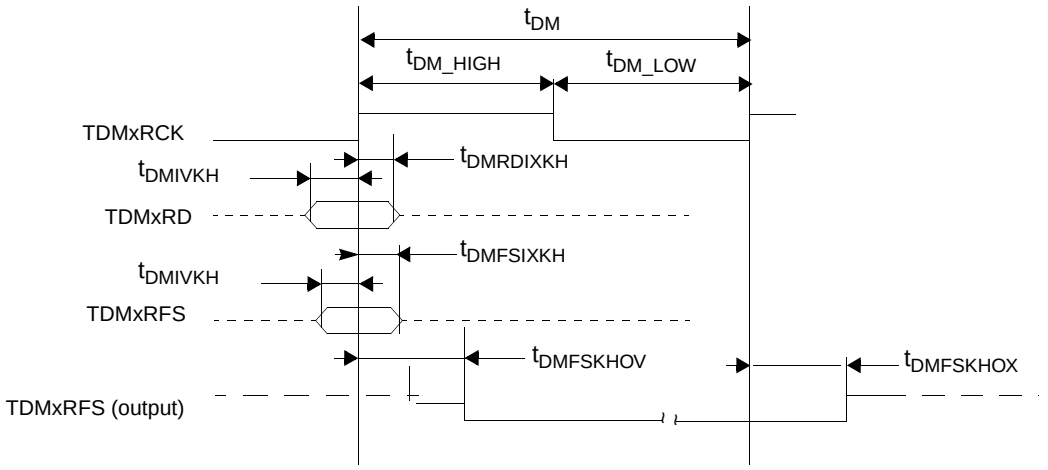
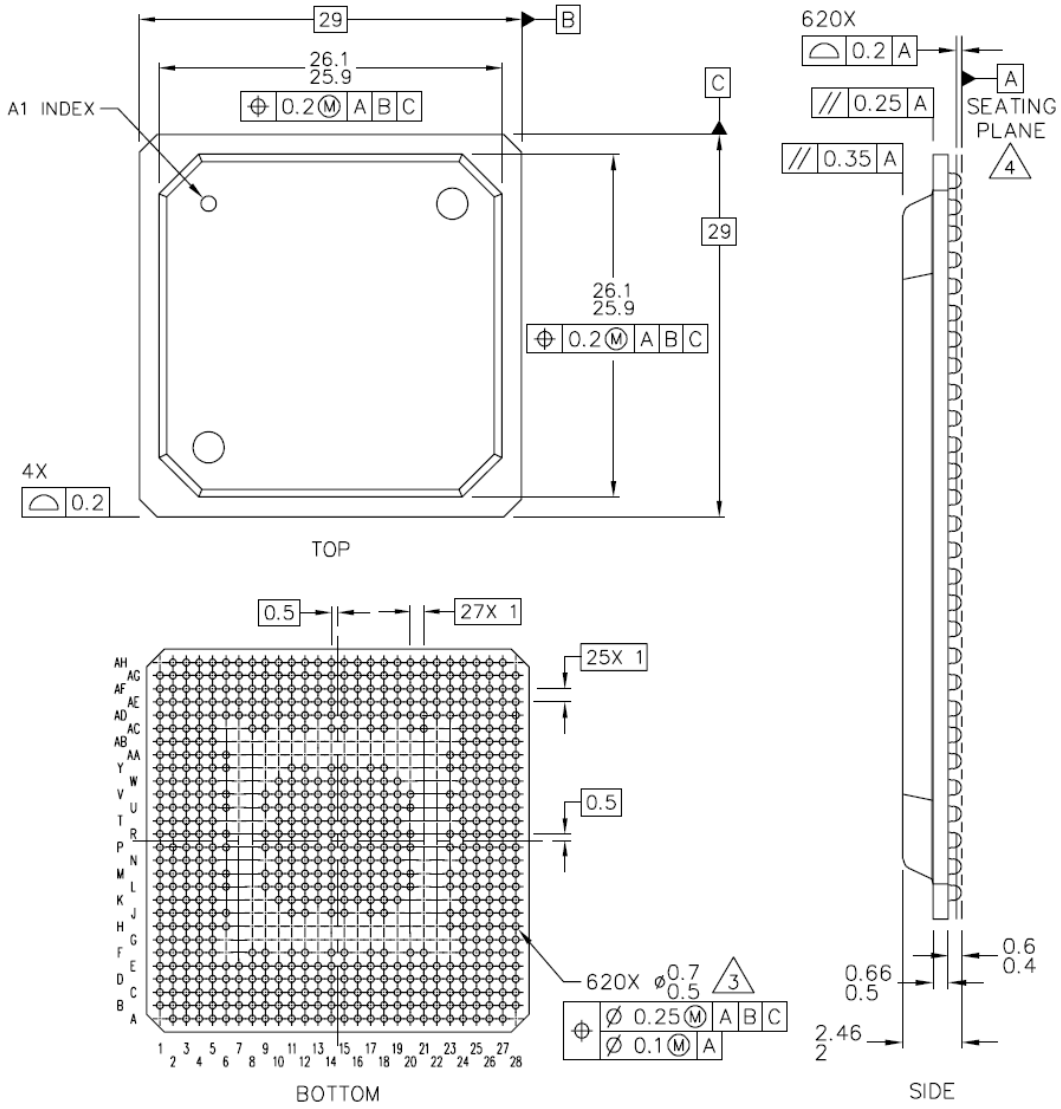


Figure 59. TDM Receive Signals

23.2 Mechanical Dimensions of the TEPBGA II

This figure shows the mechanical dimensions and bottom surface nomenclature of the 620-pin TEPBGA II package.



Notes:
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 61. Mechanical Dimensions and Bottom Surface Nomenclature of the TEPBGA II

23.3 Pinout Listings

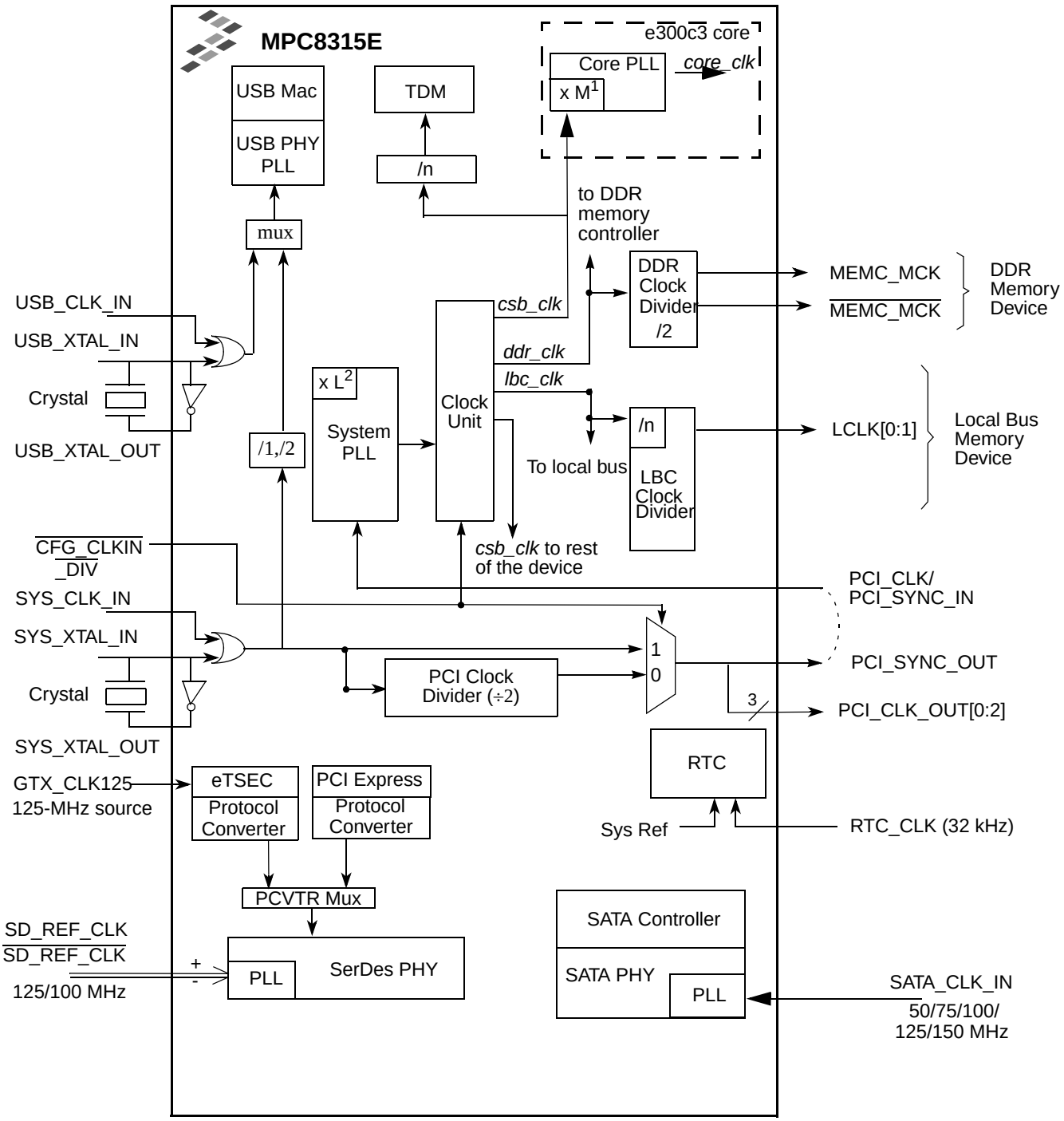
This table provides the pin-out listing for the TEPBGA II package.

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
JTAG				
TCK	E5	I	$NVDD1_{ON}$	—
TDI	B4	I	$NVDD1_{ON}$	4
TDO	C4	O	$NVDD1_{ON}$	3
TMS	C3	I	$NVDD1_{ON}$	4
$\overline{\text{TRST}}$	C2	I	$NVDD1_{ON}$	4
TDM				
GPIO_18/TDM_RCK	AB1	I/O	$NVDD1_{OFF}$	—
GPIO_20/TDM_RD	AC1	I/O	$NVDD1_{OFF}$	—
GPIO_19/TDM_RFS	AB3	I/O	$NVDD1_{OFF}$	—
GPIO_21/TDM_TCK	AB5	I/O	$NVDD1_{OFF}$	—
GPIO_23/TDM_TD	AC3	I/O	$NVDD1_{OFF}$	—
GPIO_22/TDM_TFS	AC2	I/O	$NVDD1_{OFF}$	—
SATA				
PINRXMINUSA	N28	I	VDD1IO	—
PINRXMINUSB	U28	I	VDD1IO	—
PINRXPLUSA	M28	I	VDD1IO	—
PINRXPLUSB	T28	I	VDD1IO	—
PINTXMINUSA	M25	O	VDD1IO	—
PINTXMINUSB	P26	O	VDD1IO	—
PINTXPLUSA	N25	O	VDD1IO	—
PINTXPLUSB	R26	O	VDD1IO	—
SATA_ANAVIZ	U26	O	—	—
SATA_CLK_IN	V27	I	NVDD3_OFF	—
SATA_VDD	N27	I	—	—
SATA_VDD	U23	I	—	—
SATA_VSS	M27	I	—	—
SATA_VSS	V28	I	—	—
VSSRESREF	T26	I	—	—
RESREF	T25	I	—	10
VDD33ANA	U27	I	—	—
VDD33PLL	T27	I	—	—
TEST				
TEST_MODE	D6	I	$NVDD1_{ON}$	6
DEBUG				

24 Clocking

This figure shows the internal distribution of clocks within the MPC8315E.



1 Multiplication factor M = 1, 1.5, 2, 2.5, and 3. Value is decided by RCWLR[COREPLL].

2 Multiplication factor L = 2, 3, 4 and 5. Value is decided by RCWLR[SPMF].

Figure 62. MPC8315E Clock Subsystem