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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Security; SEC 3.3
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8315evradda

- Signal (RCK) can be configured as either input or output
- Frame sync and data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock
- Frame sync can be programmed as active low or active high
- Selectable delay (0–3 bits) between the Frame Sync signal and the beginning of the frame
- MSB or LSB first support

2.7 USB Dual-Role Controller

The USB controller includes the following features:

- Designed to comply with *USB Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports UTMI+ low pin interface (ULPI) or on-chip USB-2.0 full-speed/high-speed PHY
- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI PHY

2.8 Dual PCI Express Interfaces

The PCI Express interfaces have the following features:

- PCI Express 1.0a compatible
- x1 link width
- Selectable operation as root complex or endpoint
- Both 32- and 64-bit addressing
- 128-byte maximum payload size
- Support for MSI and INTx interrupt messages
- Virtual channel 0 only
- Selectable Traffic Class
- Full 64-bit decode with 32-bit wide windows
- Dedicated descriptor based DMA engine per interface with separate read and write channels

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GVDD + 0.3)	V	2, 4
	DDR DRAM reference	MVREF	–0.3 to (GVDD + 0.3)	V	2, 4
	eTSEC signals	LV_{IN}	–0.3 to (LVDD + 0.3)	V	3, 4
	Local bus, DUART, SYS_CLK_IN, system control and power management, I^2C, and JTAG signals	NV_{IN}	–0.3 to (NVDD + 0.3)	V	3, 4
	PCI	NV_{IN}	–0.3 to (NVDD + 0.3)	V	5
	SATA_CLKIN	NV_{IN}	–0.3 to (NVDD + 0.3)	V	3, 4
Storage temperature range		T_{STG}	–55 to150	°C	—

Note:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** (N,L)V_{IN} must not exceed (N,L)VDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. (M,N,L)V_{IN} and MVREF may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
5. NV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 2.
6. The max value of supply voltage should be selected based on the RGMII mode.
7. NVDD means NVDD1_OFF, NVDD1_ON, NVDD2_OFF, NVDD2_ON, NVDD3_OFF, NVDD4_OFF
8. LVDD means LVDD1_OFF and LVDD2_ON

3.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for theMPC8315E. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

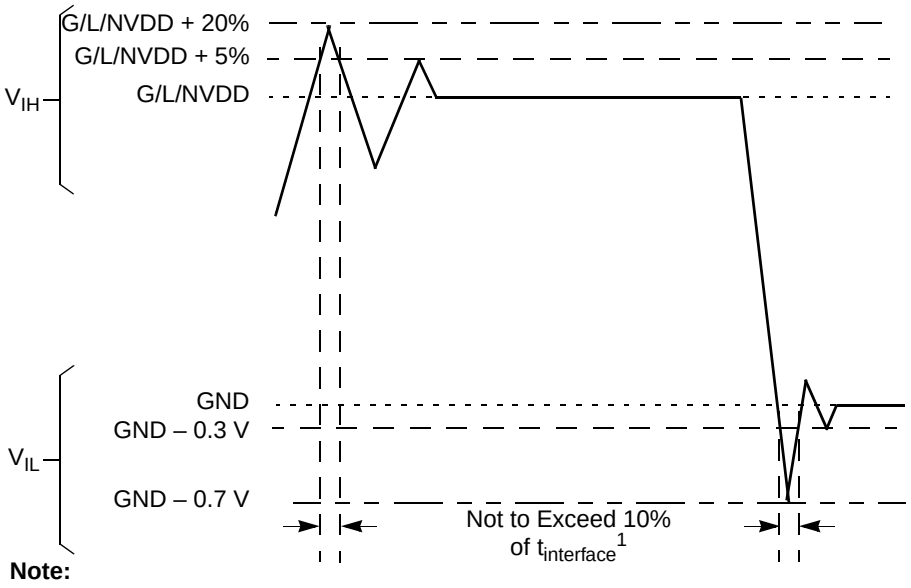
Characteristic	Symbol	Recommended Value[1]	Unit	Status in D3 Warm mode	Note
SerDes internal digital power	XCOREVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes internal digital power	XCOREVSS	0.0	V	—	—
SerDes I/O digital power	XPADVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes I/O digital power	XPADVSS	0.0	V	—	—
SerDes analog power for PLL	SDAVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes analog power for PLL	SDAVSS	0.0	V	—	—
Dedicated 3.3 V analog power for USB PLL	USB_PLL_PWR3	3.3 ± 165mv	V	Switched Off	—
Dedicated 1.0 Vanalog power for USB PLL	USB_PLL_PWR1	1.0 ± 50 mv	V	Switched Off	—
Dedicated analog ground for USB PLL	USB_PLL_GND	0.0	V	—	—
Dedicated USB power for USB bias circuit	USB_VDDA_BIAS	3.3 ± 300 mv	V	Switched Off	—

Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value[1]	Unit	Status in D3 Warm mode	Note

Note:
1. The NVDDx_ON are static power supplies and can be connected together.
2. The NVDDx_OFF are switchable power supplies and can be connected together.
3. Minimum Temperature is specified with T_A;maximum temperature is specified with T_J.
4. All Power rails must be connected and power applied to the MPC8315 even if the IP interfaces are not used.
5. All I/O pins should be interfaced with peripherals operating at same voltage level.
6. This voltage is the input to the filter discussed in Section 26.2, "PLL Power Supply Filtering" and not necessarily the voltage at the AVDD pin.
7. All 1V power supplies should be derived from the same source.

This figure shows the undershoot and overshoot voltages at the interfaces of the MPC8315E.



Note:
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for GVDD/NVDD/LVDD

3.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	NVDD = 3.3 V
PCI signals	25	
DDR signal[1]	18	GVDD = 2.5 V
DDR2 signal 1	18	GVDD = 1.8 V

7.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions

Parameter	Symbol [1]	Min	Max	Unit	Note
MCK[n] cycle time at MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	7.5	10	ns	2
ADDR/CMD output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHAS}	 2.9 3.5	 — —	ns	3
ADDR/CMD output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHAX}	 3.15 4.20	 — —	ns	3
$\overline{\text{MCS}}$[n] output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHCS}	 3.15 4.20	 — —	ns	3
$\overline{\text{MCS}}$[n] output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHCX}	 3.15 4.20	 — —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ//MDM output setup with respect to MDQS 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 900 1000	 — —	ps	5
MDQ//MDM output hold with respect to MDQS 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 1100 1200	 — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

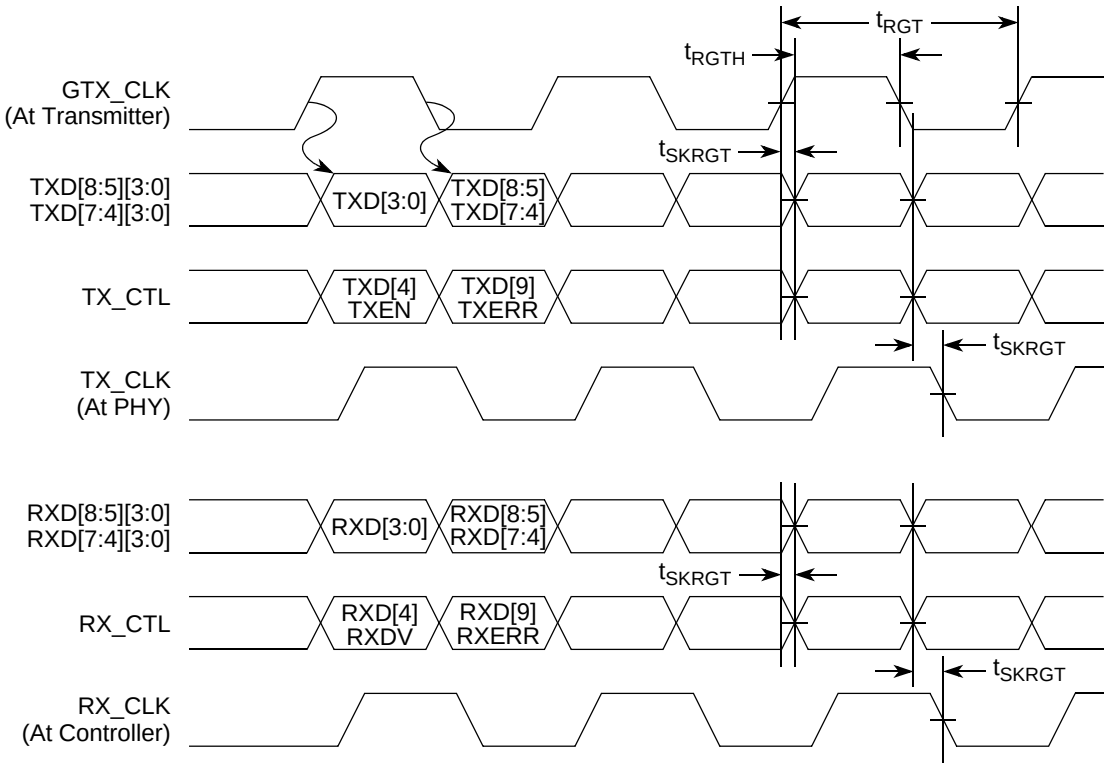


Figure 16. RGMII and RTBI AC Timing and Multiplexing Diagrams

9.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for MII, RMII, RGMII, and RTBI are specified in Section 9.1, "eTSEC (10/100/1000 Mbps)—MII/RMII/RGMII/RTBI Electrical Characteristics."

9.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Table 30. MII Management DC Electrical Characteristics Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	NVDD	—	—	3.0	3.6	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	NVDD = Min	2.10	NVDD + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	NVDD = Min	V_{SS}	0.50	V
Input high voltage	V_{IH}	—	—	2.00	—	V
Input low voltage	V_{IL}	—	—	—	0.80	V
Input high current	I_{IH}	NVDD = Max	V_{IN} [1] = 2.1 V	—	40	μA

Table 30. MII Management DC Electrical Characteristics Powered at 3.3 V (continued)

Parameter	Symbol	Conditions		Min	Max	Unit
Input low current	I_{IL}	NVDD = Max	V_{IN} = 0.5 V	–600	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

9.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 31. MII Management AC Timing Specifications

At recommended operating conditions with NVDD is 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	170	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 133 MHz, the maximum frequency is 4.16 MHz and the minimum frequency is 0.593 MHz).
3. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 133 MHz, the delay is 60 ns).

Table 35. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	XCOREVDD	0.95	1.0	1.05	V	—
Output high voltage	VOH	—	—	$XCOREVDD_{-Typ}/2 + \lvert V_{OD}\rvert_{-max}/2$	mV	1
Output low voltage	VOL	$XCOREVDD_{-Typ}/2 - \lvert V_{OD}\rvert_{-max}/2$	—	—	mV	1
Output ringing	V_{RING}	—	—	10	%	—
Output differential voltage[2, 3, 5]	$\lvert V_{OD}\rvert$	323	500	725	mV	Equalization setting: 1.0x
		296	459	665		Equalization setting: 1.09x
		269	417	604		Equalization setting: 1.2x
		243	376	545		Equalization setting: 1.33x
		215	333	483		Equalization setting: 1.5x
		189	292	424		Equalization setting: 1.71x
		162	250	362		Equalization setting: 2.0x
Output offset voltage	V_{OS}	425	500	575	mV	1, 4
Output impedance (single-ended)	R_O	40	—	60	Ω	—
Mismatch in a pair	ΔR_O	—	—	10	%	—
Change in V_{OD} between “0” and “1”	$\Delta \lvert V_{OD}\rvert$	—	—	25	mV	—
Change in V_{OS} between “0” and “1”	ΔV_{OS}	—	—	25	mV	—
Output current on short to GND	I_{SA}, I_{SB}	—	—	40	mA	—

Note:

1. This will not align to DC-coupled SGMII. $XCOREVDD_{-Typ}$=1.0V.
2. $\lvert V_{OD}\rvert = \lvert V_{TXn} - V_{\overline{TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX-DIFFp-p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the table assumes the following transmit equalization setting in the TXEQA (for SerDes lane A) or TXEQE (for SerDes lane E) bit field of MPC8315E’s SerDes Control Register 0:
   - The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. V_{OS} is also referred to as output common mode voltage.
5. The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $XCOREVDD_{-Typ}$=1.0V, no common mode offset variation (V_{OS} = 500 mV), SerDes transmitter is terminated with 100-Ω differential load between TX[n] and $\overline{TX}$[n].

Table 38. SGMII Receive AC Timing Specifications

At recommended operating conditions with XCOREVDD = 1.0V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal Jitter Tolerance	JSIN	0.1	—	—	UI p-p	1
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1
Bit Error Ratio	BER	—	—	10^{-12}		—
Unit Interval	UI	799.92	800	800.08	ps	2
AC Coupling Capacitor	C_{TX}	5	—	200	nF	3

Note:

1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It's recommended to be placed near the device transmitter outputs.
4. Refer to RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications.

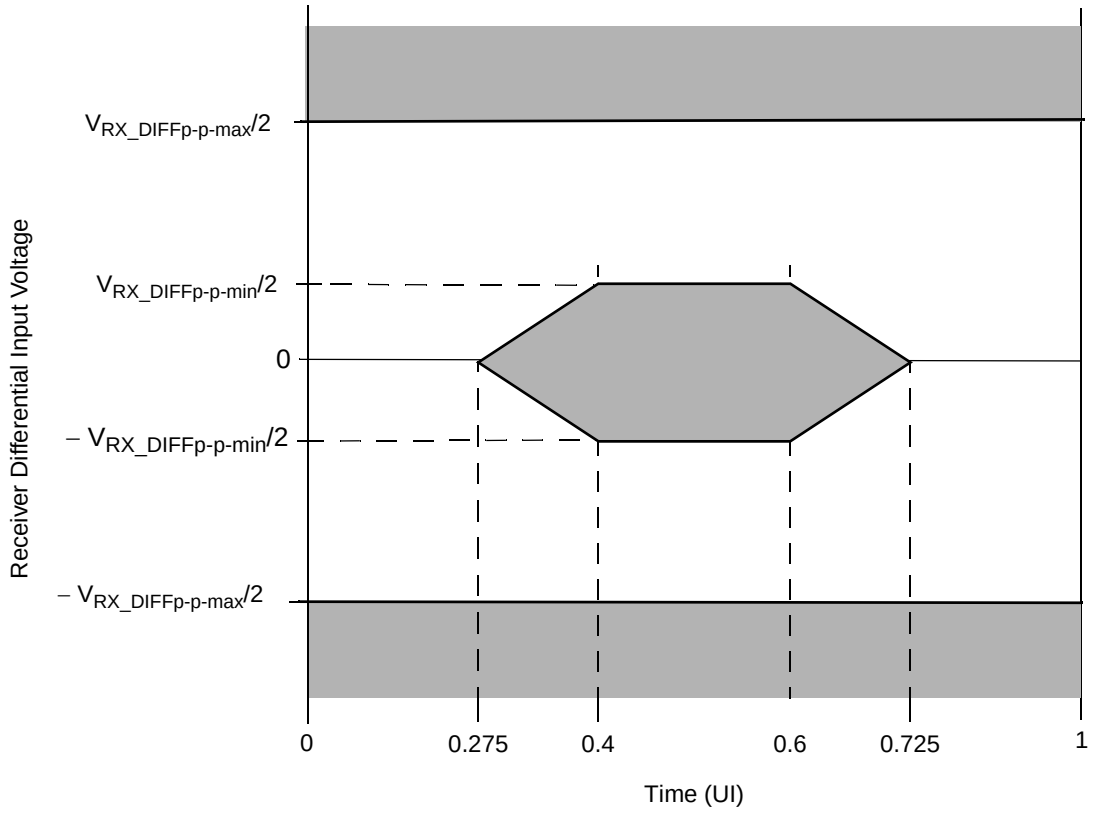


Figure 20. SGMII Receiver Input Compliance Mask

Figure 25 through Figure 27 show the local bus signals.

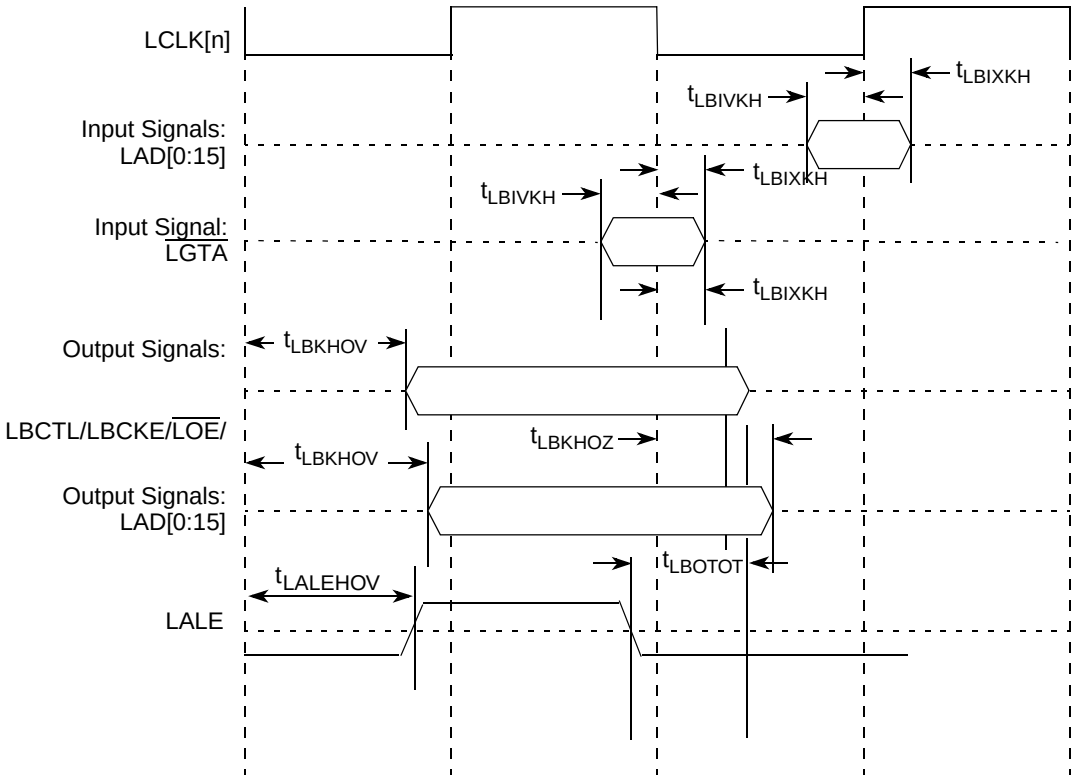


Figure 25. Local Bus Signals, Nonspecial Signals Only

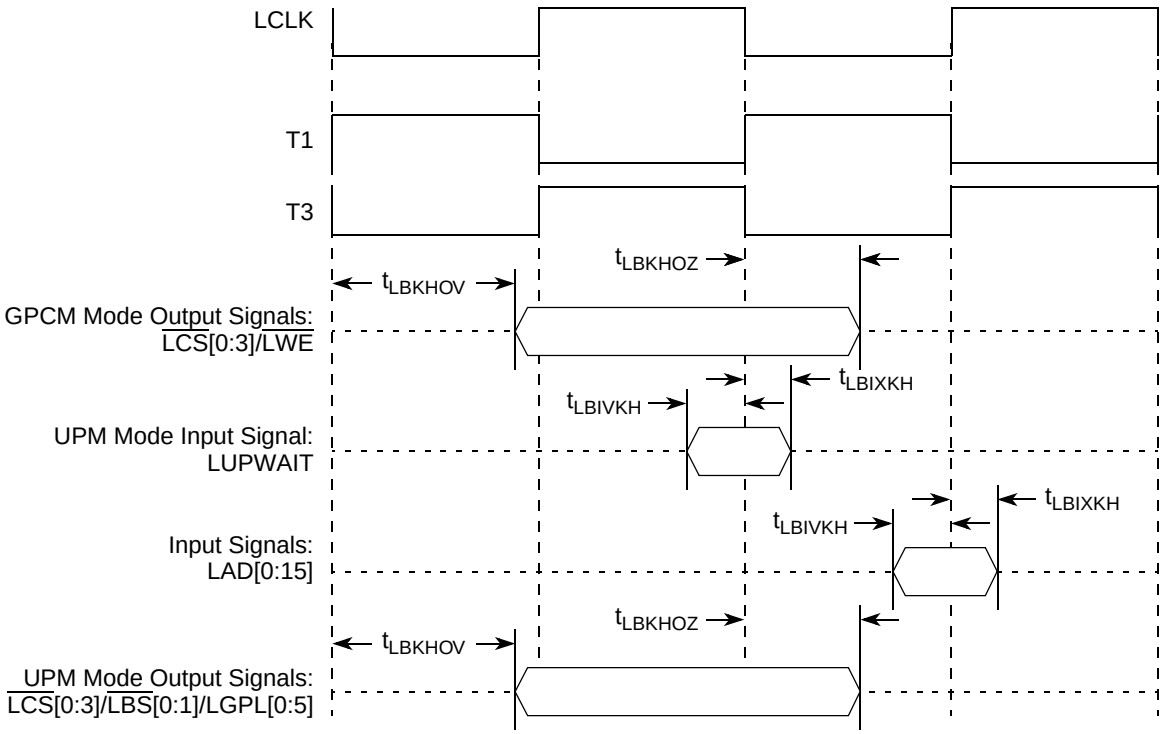


Figure 26. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2

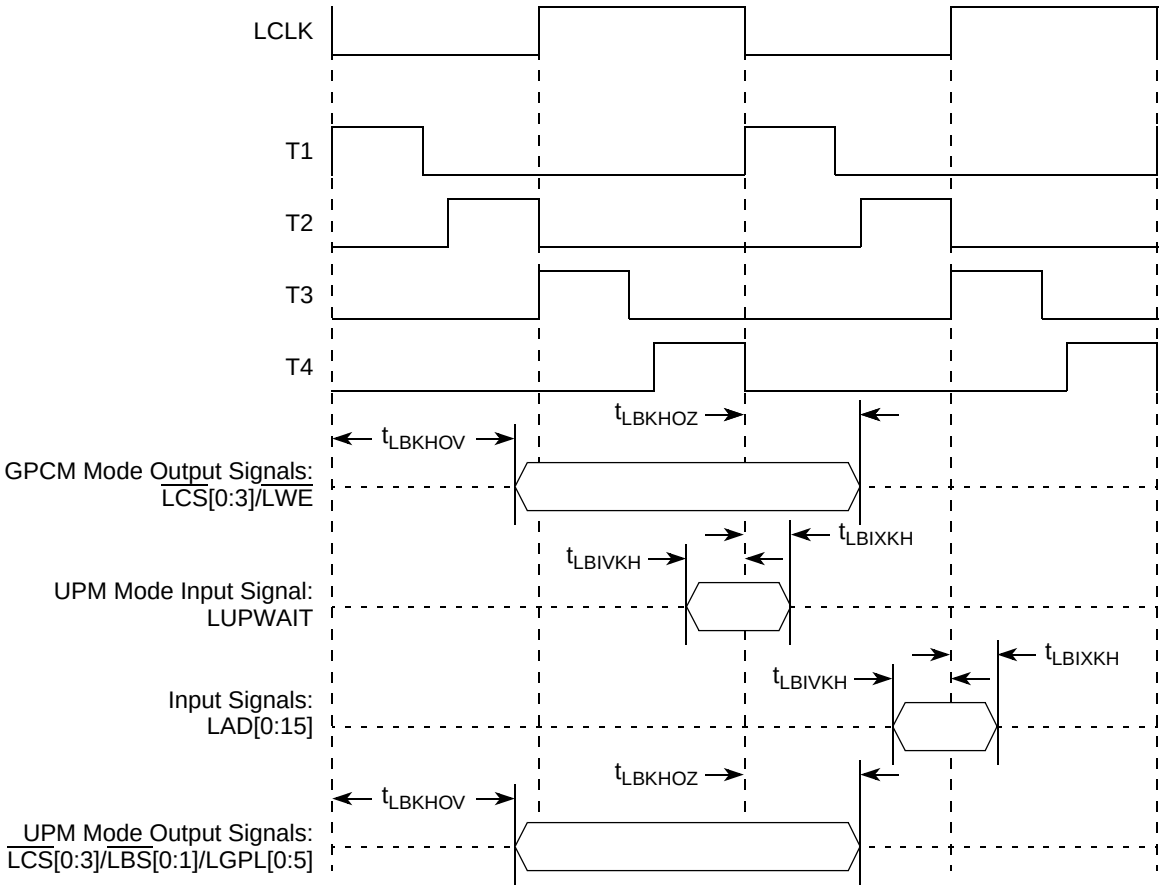


Figure 27. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

12 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface.

12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface.

Table 45. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

This figure shows the PCI input AC timing conditions.

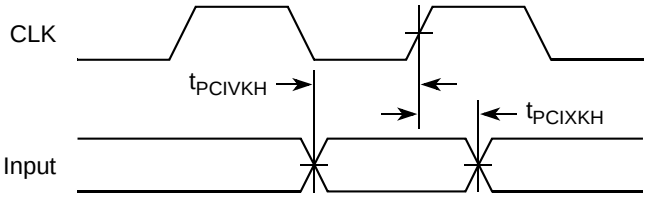


Figure 36. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

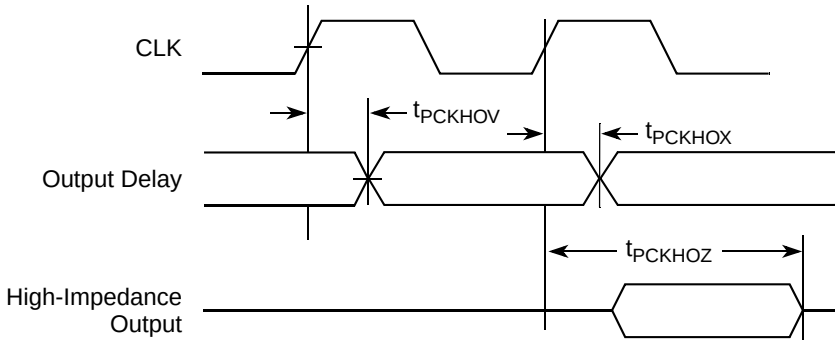


Figure 37. PCI Output AC Timing Measurement Condition

15 High-Speed Serial Interfaces (HSSI)

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

15.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 38 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (TXn and $\overline{\text{TXn}}$) or a receiver input (RXn and $\overline{\text{RXn}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals TXn, $\overline{\text{TXn}}$, RXn and $\overline{\text{RXn}}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's Single-Ended Swing.
2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

- The maximum average current requirement that also determines the common mode voltage range
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4V (0.4V/50 = 8mA) while the minimum common mode input level is 0.1V above XCOREVSS. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0-0.8V), such that each phase of the differential input has a single-ended swing from 0V to 800mV with the common mode voltage at 400mV.
  - If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 ohms to XCOREVSS DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  - This requirement is described in detail in the following sections.

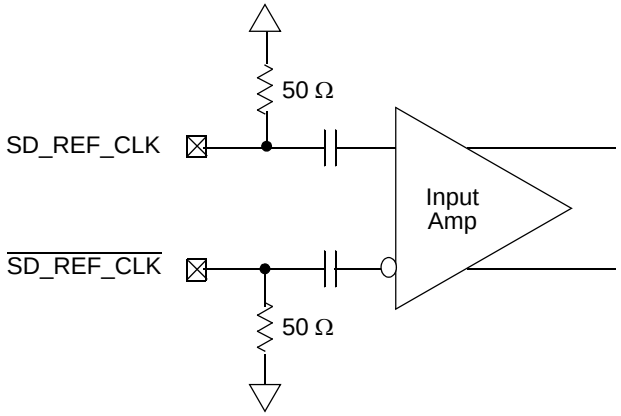


Figure 39. Receiver of SerDes Reference Clocks

15.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8315E SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400mV and 1600mV differential peak-peak (or between 200mV and 800mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800mV and greater than 200mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For **external DC-coupled** connection, as described in section 15.2.1, the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be

This figure shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8315E SerDes reference clock input's DC requirement.

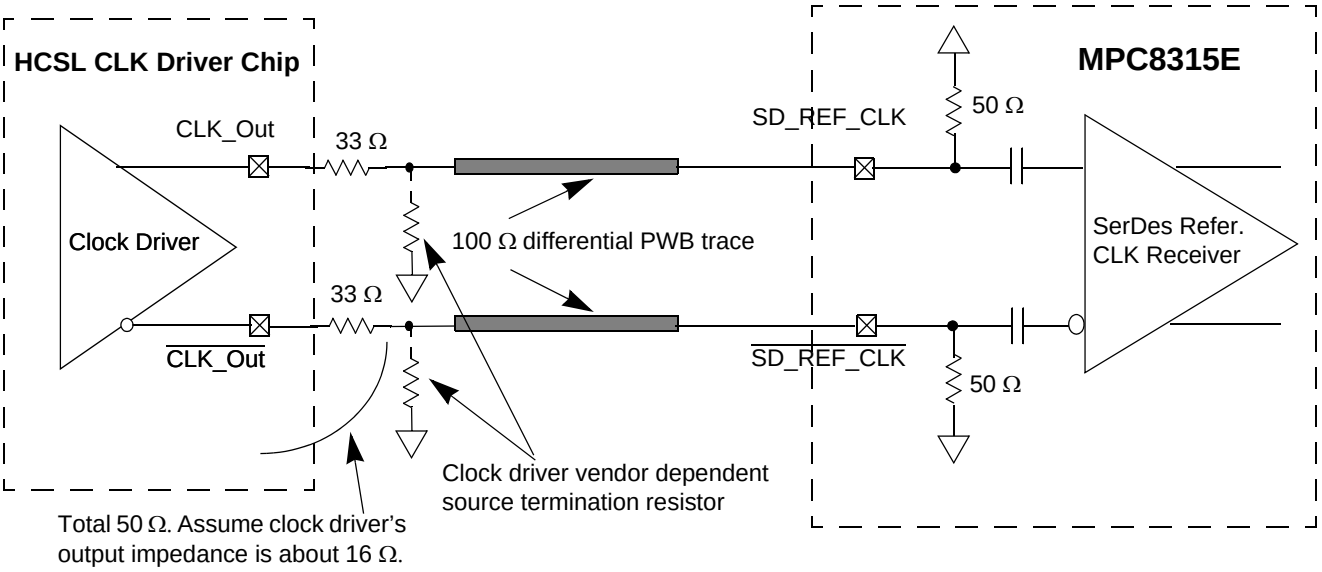


Figure 43. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8315E SerDes reference clock input's allowed range (100 to 400mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

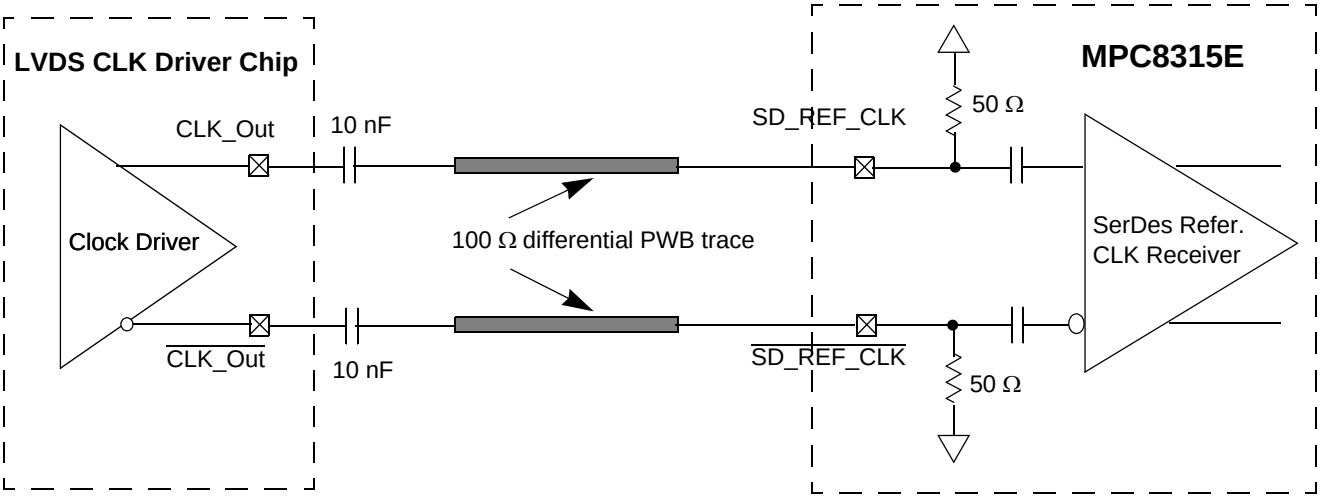


Figure 44. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 45 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8315E SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 45

Table 55. Differential Receiver (RX) Input Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Unit	Note
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power.	200 k	—	—	Ω	6
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	V_{PEEIDT} = 2*|V_{RX-D+} -V_{RX-D-}| Measured at the package pins of the Receiver	65	—	175	mV	—
Unexpected Electrical Idle Enter Detect Threshold Integration Time	$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	An unexpected Electrical Idle (Vrx-diffp-p < Vrx-idle-det-diffp-p) must be recognized no longer than Trx-idle-det-diff-entertime to signal an unexpected idle condition.	—	—	10	ms	—
Total Skew	$L_{RX-SKEW}$	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (e.g. COM and one to five SKP Symbols) at the RX as well as any delay differences arising from the interconnect itself.	—	—	20	ns	—

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 52 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 51). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 52). Note that the series capacitors, C_{TX}, is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
6. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

17.3 Out-of-Band (OOB) Electrical Characteristics

This table provides the out-of-band (OOB) electrical characteristics for the SATA interface of the MPC8315.

Table 59. Out-of-Band (OOB) Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Note
OOB Signal Detection Threshold 1.5G 3.0G	$V_{SATA\_OOBDETE}$	 50 75	 100 125	 200 200	mVp-p	—
UI During OOB Signaling	T_{SATA_UIOOB}	—	666.67	—	ps	—
COMINIT/ COMRESET and COMWAKE Transmit Burst Length	$T_{SATA\_UIOOBTXB}$	—	160	—	UI	—
COMINIT/ COMRESET Transmit Gap Length	$T_{SATA\_UIOOBTXGap}$	—	480	—	UI	—
COMWAKE Transmit Gap Length	$T_{SATA\_UIOOBTX WakeGap}$	—	160	—	UI	—

18 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8315E.

18.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 60. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le$ NVDD	—	± 5	μA

18.2 Timers AC Timing Specifications

This table provides the timers input and output AC timing specifications.

Table 61. Timers Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Table 61. Timers Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit

Note:
1. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers input are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure provides the AC test load for the Timers.

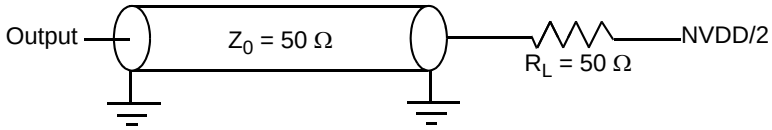


Figure 54. Timers AC Test Load

19 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8315E.

19.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO.

Table 62. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le$ NVDD	—	± 5	μA

19.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 63. GPIO Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Note:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
JTAG				
TCK	E5	I	$NVDD1_{ON}$	—
TDI	B4	I	$NVDD1_{ON}$	4
TDO	C4	O	$NVDD1_{ON}$	3
TMS	C3	I	$NVDD1_{ON}$	4
$\overline{\text{TRST}}$	C2	I	$NVDD1_{ON}$	4
TDM				
GPIO_18/TDM_RCK	AB1	I/O	$NVDD1_{OFF}$	—
GPIO_20/TDM_RD	AC1	I/O	$NVDD1_{OFF}$	—
GPIO_19/TDM_RFS	AB3	I/O	$NVDD1_{OFF}$	—
GPIO_21/TDM_TCK	AB5	I/O	$NVDD1_{OFF}$	—
GPIO_23/TDM_TD	AC3	I/O	$NVDD1_{OFF}$	—
GPIO_22/TDM_TFS	AC2	I/O	$NVDD1_{OFF}$	—
SATA				
PINRXMINUSA	N28	I	VDD1IO	—
PINRXMINUSB	U28	I	VDD1IO	—
PINRXPLUSA	M28	I	VDD1IO	—
PINRXPLUSB	T28	I	VDD1IO	—
PINTXMINUSA	M25	O	VDD1IO	—
PINTXMINUSB	P26	O	VDD1IO	—
PINTXPLUSA	N25	O	VDD1IO	—
PINTXPLUSB	R26	O	VDD1IO	—
SATA_ANAVIZ	U26	O	—	—
SATA_CLK_IN	V27	I	NVDD3_OFF	—
SATA_VDD	N27	I	—	—
SATA_VDD	U23	I	—	—
SATA_VSS	M27	I	—	—
SATA_VSS	V28	I	—	—
VSSRESREF	T26	I	—	—
RESREF	T25	I	—	10
VDD33ANA	U27	I	—	—
VDD33PLL	T27	I	—	—
TEST				
TEST_MODE	D6	I	$NVDD1_{ON}$	6
DEBUG				

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
VSS1IO	M24, N24, P19, P20, P25, P27, R25, R27, T24	I	—	—
XCOREVDD	P2, P10, R2, T1	I	—	—
XCOREVSS	R3, R10, U2, V2	I	—	—
XPADVDD	P3, R9, U3	I	—	—
XPADVSS	P5, P9, V3	I	—	—

Note:

1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to NVDD.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to NVDD.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. This pin must always be tied to VSS.
7. Thermal sensitive resistor.
8. This pin should be connected to USB_VSSA_BIAS through 10K precision resistor.
9. The LB_POR_CFG_BOOT_ECC functionality for this pin is only available in MPC8315E revision 1.1 and later. The LB_POR_CFG_BOOT_ECC is sampled only during the $\overline{\text{PORESET}}$ negation. This pin with an internal pull down resistor enables the ECC by default. To disable the ECC an external strong pull up resistor or a tristate buffer is needed.
10. This pin should be connected to an external 2.7 K ±1% resistor connected to VSS. The resistor should be placed as close as possible to the input.
11. This pin has a weak internal pull-down.
12. This pin has a weak internal pull-up.

Table 71. Configurable Clock Units

Unit	Default Frequency	Options
eTSEC1	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*
eTSEC2	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*
Security Core, I2C, SAP, TPR	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*
USB DR	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*
PCI and DMA complex	*csb_clk*	Off, *csb_clk*
PCI Express	*csb_clk*	Off, *csb_clk*
Serial ATA	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*

This table provides the operating frequencies for the TEPBGA II under recommended operating conditions (see Table 2).

Table 72. Operating Frequencies for TEPBGA II

Characteristic[1]	Max Operating Frequency	Unit
e300 core frequency (*core_clk*)	400	MHz
Coherent system bus frequency (*csb_clk*)	133	MHz
DDR1/2 memory bus frequency (MCK)[2]	133	MHz
Local bus frequency (LCLK*n*)[3]	66	MHz
PCI input frequency (SYS_CLK_IN or PCI_CLK)	24-66	MHz

Note:
1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK[0:1], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The DDR data rate is 2x the DDR memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the *lbiu_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

24.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 73 shows the multiplication factor encodings for the system PLL.

NOTE

If RCWL[DDRCM] and RCWL[LBCM] are both cleared, the system PLL VCO frequency = (CSB frequency) × (System PLL VCO Divider).

If either RCWL[DDRCM] or RCWL[LBCM] are set, the system PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO Divider).

The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.

also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 81. Part Numbering Nomenclature

MPC	8315	E	C	VR	AG	D	A
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range [3]**	**Package [1]**	**e300 Core Frequency [2]**	**DDR Frequency**	**Revision Level**
MPC	8315	Blank = Not included E = included	Blank = 0 to 105°C C = –40 to 105°C	VR= Pb Free TEPBGA II	AD = 266 MHz AF = 333 MHz AG = 400 MHz	D = 266 MHz	Contact local Freescale sales office

Note:
1. See Section 23, “Package and Pin Listings,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by electric may support other maximum core frequencies.
3. Contact your local Freescale field applications engineer (FAE).

This table shows the SVR settings by device and package type.

Table 82. SVR Settings

Device	Package	SVR (Rev 1.0)	SVR (Rev 1.1)	SVR (Rev 1.2)
MPC8315E	TEPBGA II	0x80B4_0010	0x80B4_0011	0x80B4_0012
MPC8315	TEPBGA II	0x80B5_0010	0x80B5_0011	0x80B5_0012

Note:
1. PVR = 8085_0020 for all devices and revisions in this table.