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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Security; SEC 3.3
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8315evrafda

1 Overview

The MPC8315E incorporates the e300c3 (MPC603e-based) core, which includes 16 Kbytes of L1 instruction and data caches, on-chip memory management units (MMUs), and floating-point support. In addition to the e300 core, the SoC platform includes features such as dual enhanced three-speed 10, 100, 1000 Mbps Ethernet controllers (eTSECs) with SGMII support, a 32- or 16-bit DDR1/DDR2 SDRAM memory controller, dual SATA 3 Gbps controllers (MPC8315E-specific), a security engine to accelerate control and data plane security protocols, and a high degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration. The MPC8315E also offers peripheral interfaces such as a 32-bit PCI interface with up to 66 MHz operation, 16-bit enhanced local bus interface with up to 66 MHz operation, TDM interface, and USB 2.0 with an on-chip USB 2.0 PHY.

The MPC8315E offers additional high-speed interconnect support with dual integrated SATA 3 Gbps interfaces and dual single-lane PCI Express interfaces. When not used for PCI Express, the SerDes interface may be configured to support SGMII. The MPC8315E security engine (SEC 3.3) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. This figure shows a block diagram of the MPC8315E.

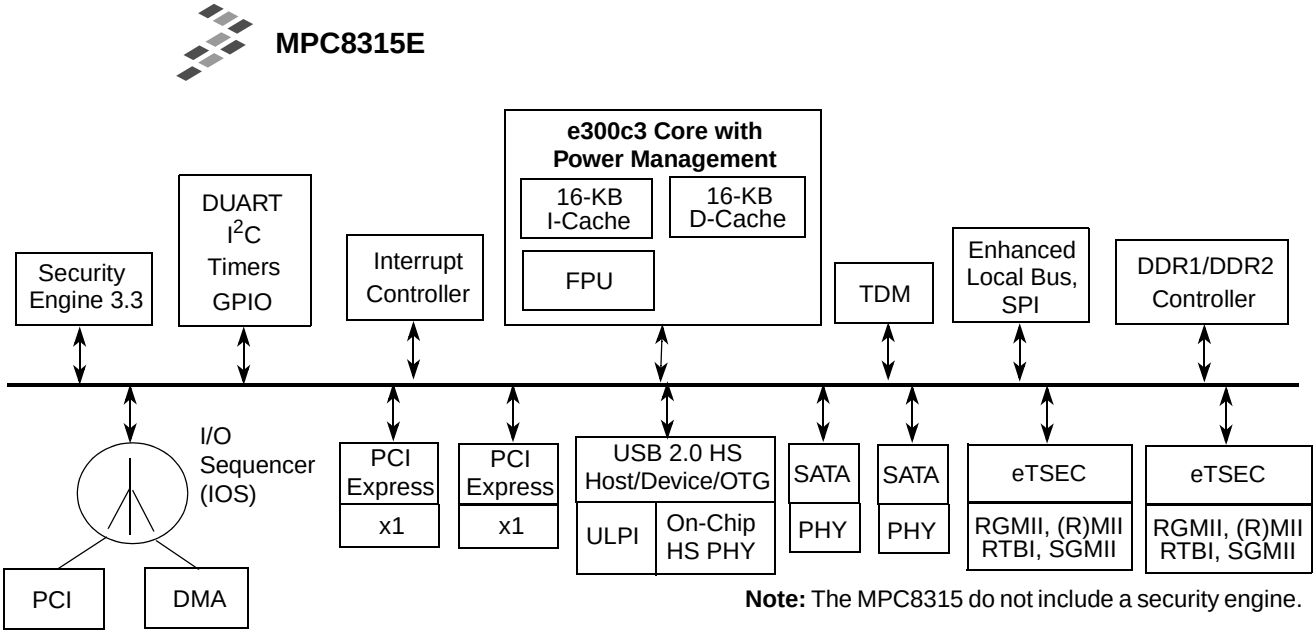


Figure 1. MPC8315E Block Diagram

2 MPC8315E Features

The following features are supported in the MPC8315E.

2.1 e300 Core

The e300 core has the following features:

- Operates at up to 400 MHz

2.9 Dual Serial ATA (SATA) Controllers

The SATA controllers have the following features:

- Designed to comply with *Serial ATA Rev 2.5 Specification*
- ATAPI 6+
- Spread spectrum clocking on receive
- Asynchronous notification
- Hot plug including asynchronous signal recovery
- Link power management
- Native command queuing
- Staggered spin-up and port multiplier support
- SATA 1.5 and 3.0 Gbps operation
- Interrupt driven
- Power management support
- Error handling and diagnostic features
  - Far end/near end loopback
  - Failed CRC error reporting
  - Increased ALIGN insertion rates
  - Scrambling and CONT override

2.10 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The eTSECs include the following features:

- Two SGMII/RGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Std 802.3™, IEEE 802.3u™, IEEE 802.3x™, IEEE 802.3z™, IEEE 802.3au™, IEEE 802.3ab™, and IEEE Std 1588™
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status.

2.11 Integrated Programmable Interrupt Controller (IPIC)

The integrated programmable interrupt controller (IPIC) provides a flexible solution for general-purpose interrupt control. The IPIC programming model is compatible with the MPC8260 interrupt controller and supports external and internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

5.1 DC Electrical Characteristics

This table provides the clock input (SYS_CLK_IN/PCI_SYNC_IN) DC timing specifications for the MPC8315E.

Table 6. SYS_CLK_IN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	NVDD + 0.3	V
Input low voltage	—	V_{IL}	-0.3	0.4	V
SYS_CLK_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
SYS_XTAL_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±40	μA
PCI_SYNC_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
RTC_CLK input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
USB_CLK_IN input current	0 V ≤ V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
USB_XTAL_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±40	μA
SATA_CLK_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA

5.2 AC Electrical Characteristics

The primary clock source for the MPC8315E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (SYS_CLK_IN/PCI_CLK) AC timing specifications for the MPC8315E.

Table 7. SYS_CLK_IN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
SYS_CLK_IN/PCI_CLK frequency	$f_{SYS\_CLK\_IN}$	24	—	66.67	MHz	1, 6, 7
SYS_CLK_IN/PCI_CLK cycle time	$t_{SYS\_CLK\_IN}$	15	—	41.6	ns	6
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	0.6	—	4	ns	2, 6
PCI_CLK rise and fall time	t_{PCH}, t_{PCL}	0.6	0.8	1.2	ns	2
SYS_CLK_IN/PCI_CLK duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3, 6
SYS_CLK_IN/PCI_CLK jitter	—	—	—	±150	ps	4, 5, 6

Note:

1. **Caution:** The system, core, and security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN/PCI_CLK are specified at 20% to 80% of signal swing.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
6. The parameter names PCI_CLK and PCI_SYNC_IN are used interchangeably in this document.
7. Spread spectrum is allowed up to 1% down-spread at 33kHz.(max. rate).

This figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

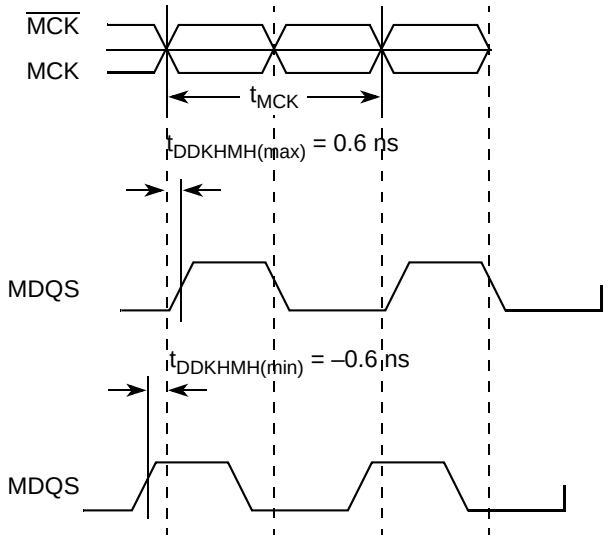


Figure 7. Timing Diagram for t_{DDKHMH}

This figure shows the DDR and DDR2 SDRAM output timing diagram.

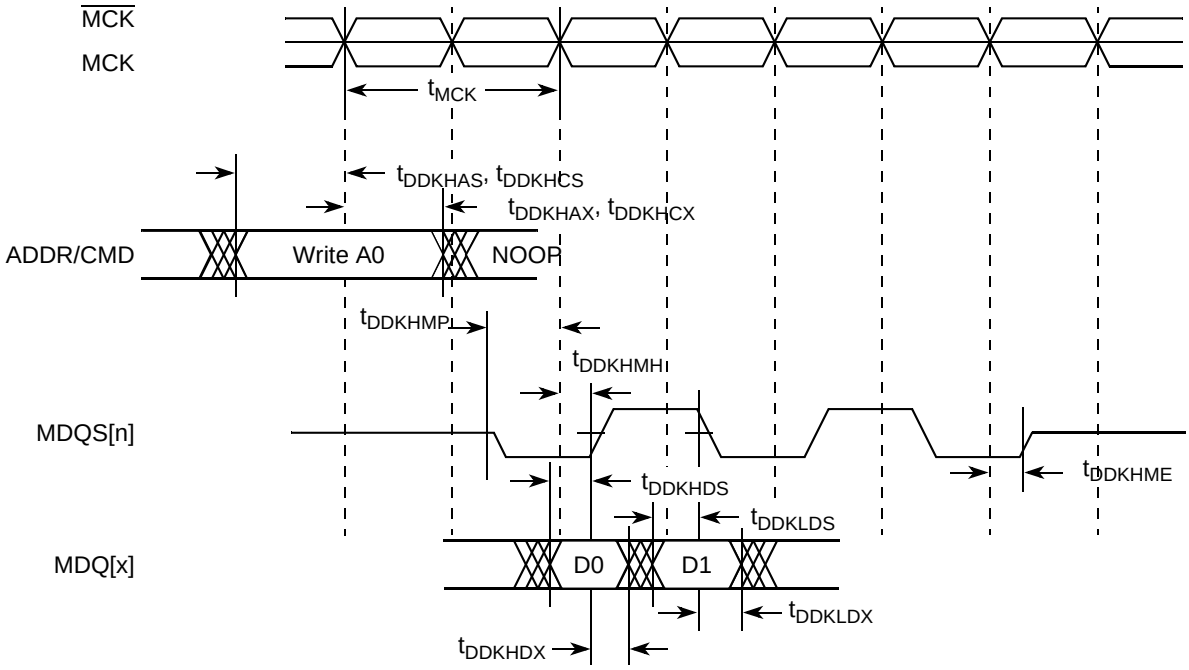


Figure 8. DDR and DDR2 SDRAM Output Timing Diagram

9.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

9.2.2.1 RMII Transmit AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications. This table provides the RMII transmit AC timing specifications.

Table 27. RMII Transmit AC Timing Specifications

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	10	ns
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

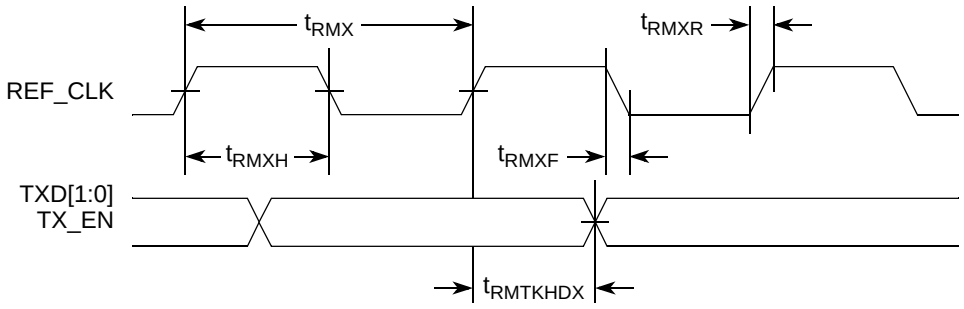


Figure 13. RMII Transmit AC Timing Diagram

9.2.2.2 RMII Receive AC Timing Specifications

This table provides the RMII receive AC timing specifications.

Table 28. RMII Receive AC Timing Specifications

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%

Table 29. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions (see Table 2)

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Clock cycle duration [3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12} [6]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Note:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the RTBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is LVDD/2.
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention. GTX_CLK supply voltage is fixed at 3.3V inside the chip. If PHY supplies a 2.5 V Clock signal on this input, set TSCOMOBI bit of System I/O configuration register (SICRH) as 1. See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
7. The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm

This figure shows the MII management AC timing diagram.

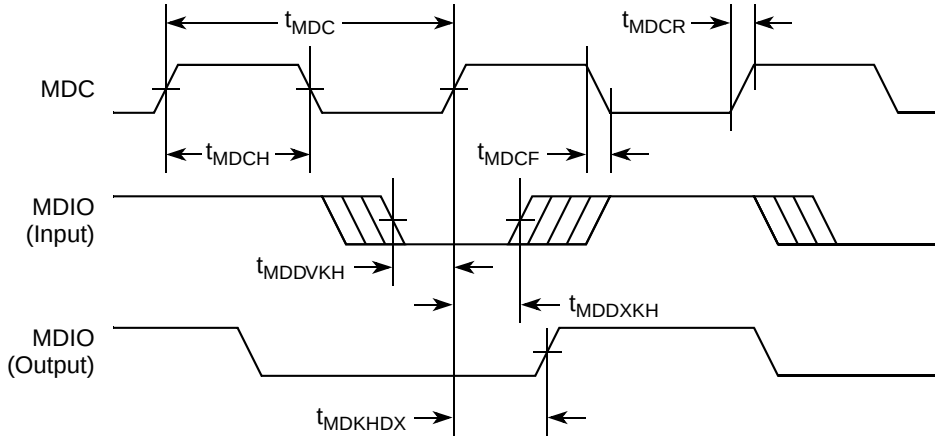


Figure 17. MII Management Interface Timing Diagram

9.4 1588 Timer Specifications

This section describes the DC and AC electrical specifications for the 1588 timer.

9.4.1 1588 Timer DC Specifications

This table provides the 1588 timer DC specifications.

Table 32. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NVDD	—	± 5	μA

9.4.2 1588 Timer AC Specifications

This table provides the 1588 timer AC specifications.

Table 33. 1588 Timer AC Specifications

Parameter	Symbol	Min	Max	Unit	Note
Timer clock cycle time	t_{TMRCK}	0	70	MHz	1
Input setup to timer clock	t_{TMRCKS}	—	—	—	2, 3
Input hold from timer clock	t_{TMRCKH}	—	—	—	2, 3
Output clock to output valid	t_{GCLKNV}	0	6	ns	
Timer alarm to output valid	t_{TMRAL}	—	—	—	2

Table 38. SGMII Receive AC Timing Specifications

At recommended operating conditions with XCOREVDD = 1.0V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal Jitter Tolerance	JSIN	0.1	—	—	UI p-p	1
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1
Bit Error Ratio	BER	—	—	10^{-12}		—
Unit Interval	UI	799.92	800	800.08	ps	2
AC Coupling Capacitor	C_{TX}	5	—	200	nF	3

Note:

1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It's recommended to be placed near the device transmitter outputs.
4. Refer to RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications.

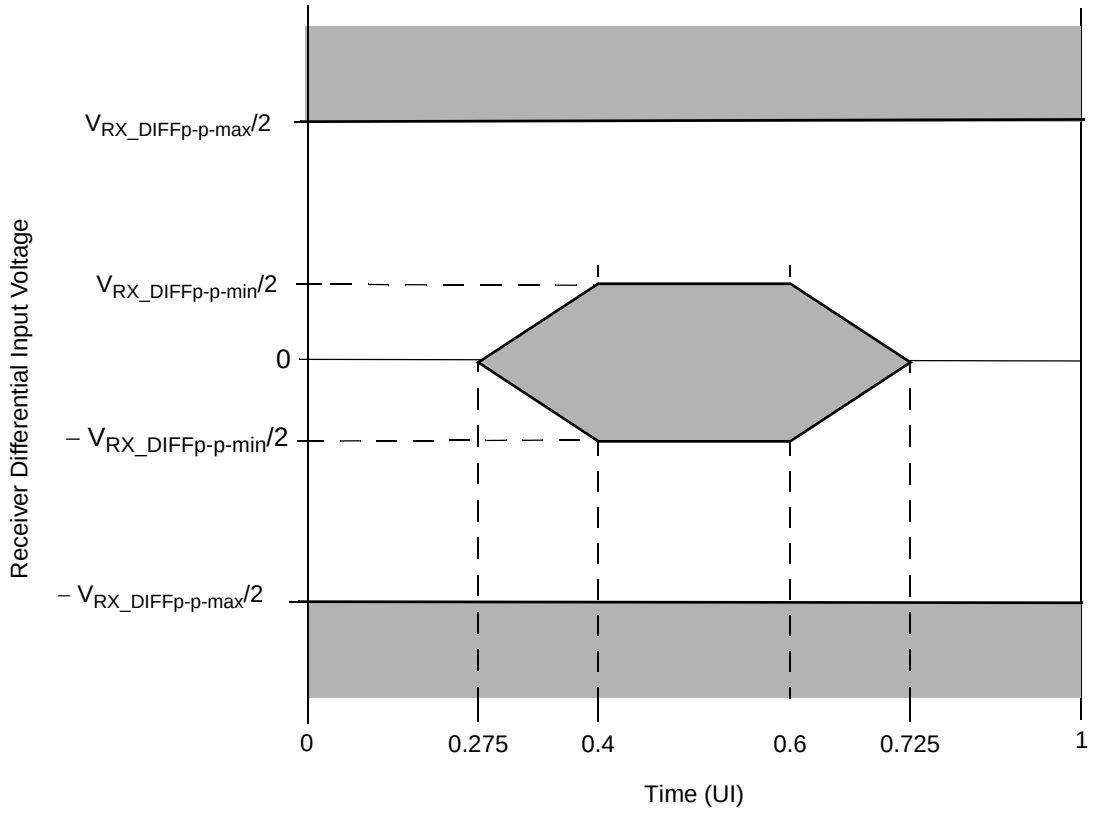


Figure 20. SGMII Receiver Input Compliance Mask

Table 44. Local Bus General Timing Parameters (continued)

Parameter	Symbol [1]	Min	Max	Unit	Note
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD	t_{LBKHOZ}	—	4	ns	8
LALE output rise to LCLK negative edge	$t_{LALEHOV}$	—	3.0	ns	

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from NVDD/2 of the rising/falling edge of LCLK0 to 0.4 × NVDD of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.
8. For active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This figure provides the AC test load for the local bus.

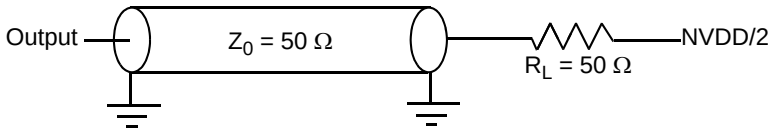


Figure 24. Local Bus AC Test Load

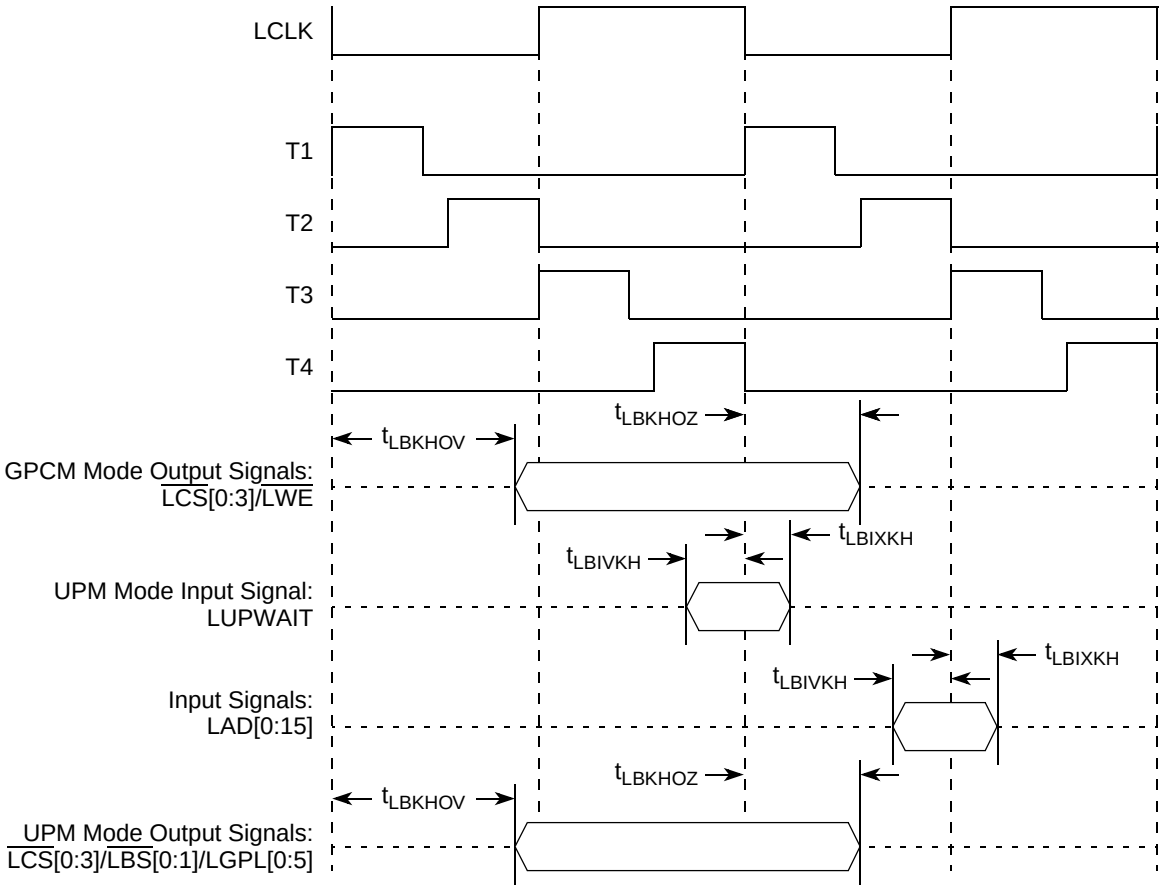


Figure 27. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

12 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface.

12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface.

Table 45. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

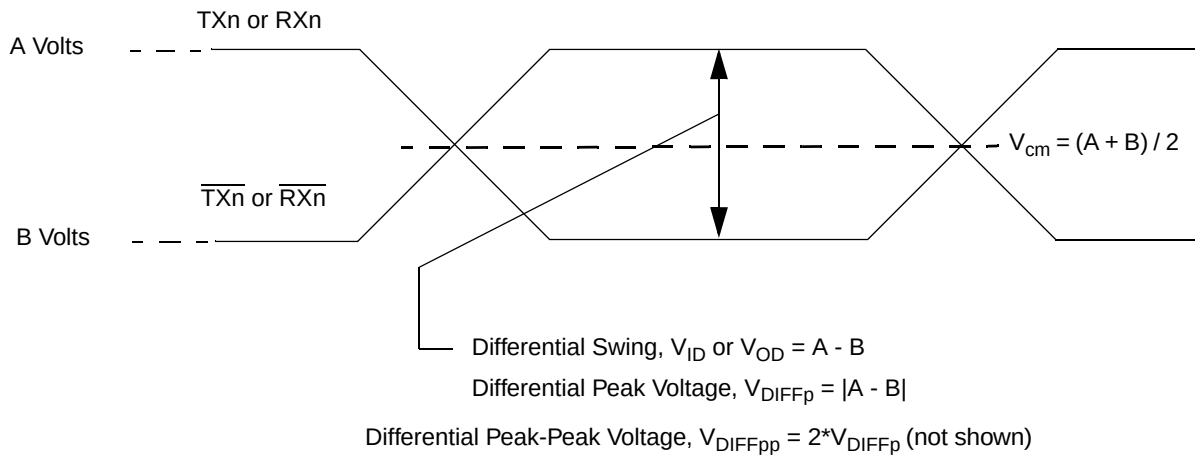


Figure 38. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5V and 2.0V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

15.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks input is SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ for PCI Express and SGMII interface.

The following sections describe the SerDes reference clock requirements and some application information.

15.2.1 SerDes Reference Clock Receiver Characteristics

Figure 39 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XCOREVDD are specified in Table 1 and Table 2.
- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 39. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to XCOREVSS followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.

Table 54. Differential Transmitter (TX) Output Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Unit	Note
Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	$T_{TX-IDLE-SET-TO-IDLE}$	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.	—	—	20	UI	—
Maximum time to transition to valid TX specifications after leaving an electrical idle condition	$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle	—	—	20	UI	—
Differential return loss	$RL_{TX-DIFF}$	Measured over 50 MHz to 1.25 GHz.	12	—	—	dB	4
Common mode return loss	RL_{TX-CM}	Measured over 50 MHz to 1.25 GHz.	6	—	—	dB	4
DC differential TX impedance	$Z_{TX-DIFF-DC}$	TX DC Differential mode Low Impedance	80	100	120	Ω	—
Transmitter DC impedance	Z_{TX-DC}	Required TX D+ as well as D- DC Impedance during all states	40	—	—	Ω	—
Lane-to-Lane output skew	$L_{TX-SKEW}$	Static skew between any two Transmitter Lanes within a single Link	—	—	500 + 2 UI	ps	—
AC coupling capacitor	C_{TX}	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.	75	—	200	nF	8
Crosslink random timeout	$T_{crosslink}$	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port.	0	—	1	ms	7

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 52 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 50.)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 52). Note that the series capacitors, C_{TX}, is optional for the return loss measurement.
5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 52 for both V_{TX-D+} and V_{TX-D-}.
6. See Section 4.3.1.8 of the *PCI Express Base Specifications*, Rev 1.0a.
7. See Section 4.2.6.3 of the *PCI Express Base Specifications*, Rev 1.0a.
8. MPC8315E SerDes transmitter does not have C_{TX} built-in. An external AC Coupling capacitor is required

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{QUIESCE}}$	B5	O	$NVDD1_{ON}$	—
System Control				
$\overline{\text{HRESET}}$	B6	I/O	$NVDD1_{ON}$	1
$\overline{\text{PORESET}}$	A6	I	$NVDD1_{ON}$	—
Clocks				
SYS_XTAL_IN	L27	I	$NVDD2_{ON}$	—
SYS_XTAL_OUT	J28	O	$NVDD2_{ON}$	—
SYS_CLK_IN	K28	I	$NVDD2_{ON}$	—
USB_XTAL_IN	A15	I	$NVDD2_{OFF}$	—
USB_XTAL_OUT	B14	O	$NVDD2_{OFF}$	—
USB_CLK_IN	B15	I	$NVDD2_{OFF}$	—
PCI_SYNC_OUT	J27	O	$NVDD2_{ON}$	3
RTC_CLK	K26	I	$NVDD2_{ON}$	—
PCI_SYNC_IN	K27	I	$NVDD2_{ON}$	—
MISC				
AVDD1	AC15	I	—	—
AVDD2	M23	I	—	—
THERM0	L25	I	$NVDD2_{ON}$	7
$\overline{\text{DMA\_DACK0}}$/GPIO_13	AC4	I/O	$NVDD1_{OFF}$	—
$\overline{\text{DMA\_DREQ0}}$/GPIO_12	AD1	I/O	$NVDD1_{OFF}$	—
DMA_DONE0/GPIO_14	AD2	I/O	$NVDD1_{OFF}$	—
NC, No Connect	A2	—	—	—
NC, No Connect	U25	—	—	—
PCI				
$\overline{\text{PCI\_INTA}}$	B18	O	$NVDD2_{OFF}$	—
$\overline{\text{PCI\_RESET\_OUT}}$	A20	O	$NVDD2_{OFF}$	—
PCI_AD[0]	J25	I/O	$NVDD2_{OFF}$	—
PCI_AD[1]	J24	I/O	$NVDD2_{OFF}$	—
PCI_AD[2]	K24	I/O	$NVDD2_{OFF}$	—
PCI_AD[3]	H27	I/O	$NVDD2_{OFF}$	—
PCI_AD[4]	H28	I/O	$NVDD2_{OFF}$	—
PCI_AD[5]	H26	I/O	$NVDD2_{OFF}$	—
PCI_AD[6]	G27	I/O	$NVDD2_{OFF}$	—
PCI_AD[7]	G28	I/O	$NVDD2_{OFF}$	—
PCI_AD[8]	F26	I/O	$NVDD2_{OFF}$	—

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

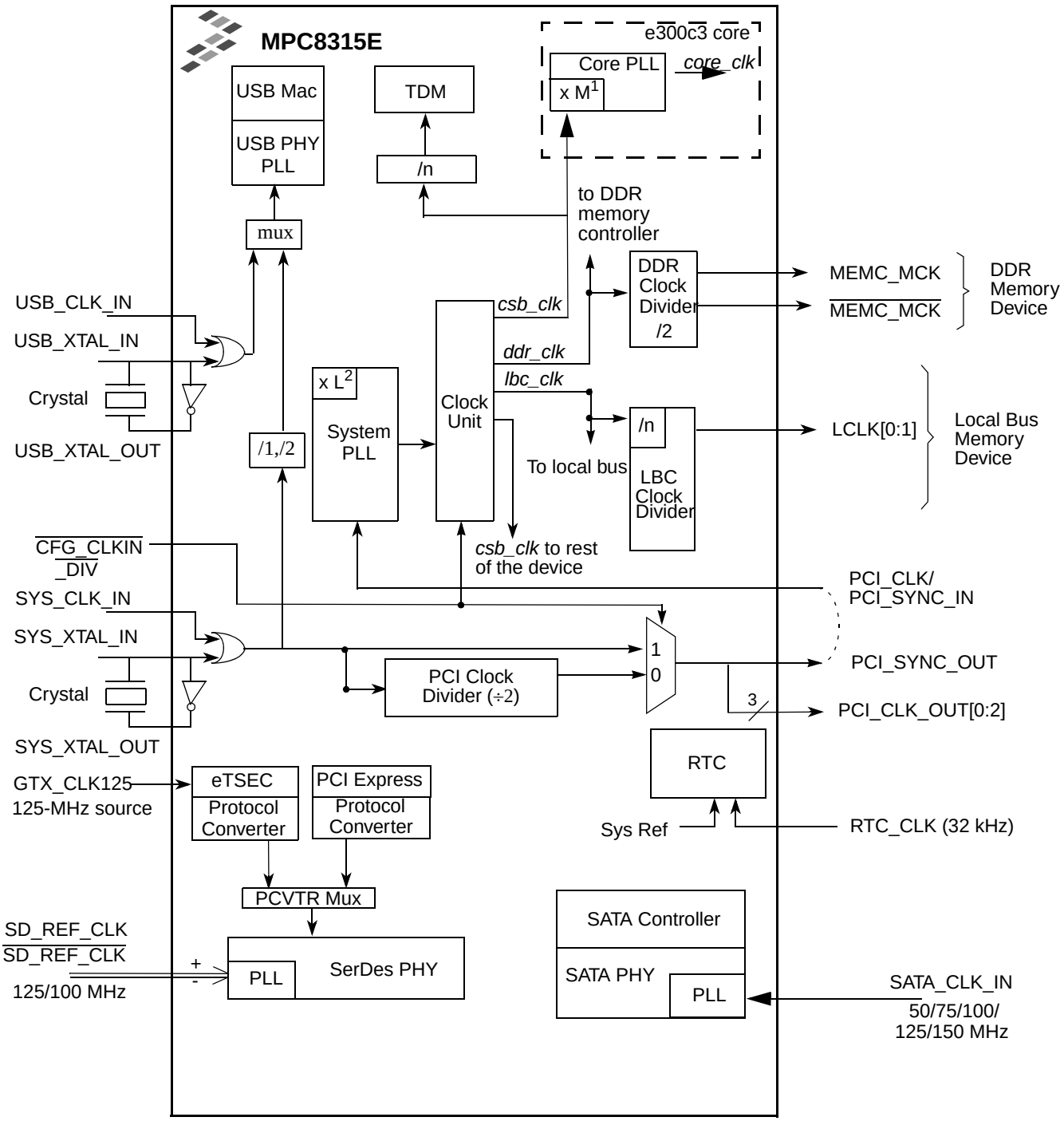
Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_AD[9]	F28	I/O	$NVDD2_{OFF}$	—
PCI_AD[10]	G25	I/O	$NVDD2_{OFF}$	—
PCI_AD[11]	F27	I/O	$NVDD2_{OFF}$	—
PCI_AD[12]	E27	I/O	$NVDD2_{OFF}$	—
PCI_AD[13]	E28	I/O	$NVDD2_{OFF}$	—
PCI_AD[14]	D28	I/O	$NVDD2_{OFF}$	—
PCI_AD[15]	D27	I/O	$NVDD2_{OFF}$	—
PCI_AD[16]	B25	I/O	$NVDD2_{OFF}$	—
PCI_AD[17]	D24	I/O	$NVDD2_{OFF}$	—
PCI_AD[18]	B26	I/O	$NVDD2_{OFF}$	—
PCI_AD[19]	C24	I/O	$NVDD2_{OFF}$	—
PCI_AD[20]	A26	I/O	$NVDD2_{OFF}$	—
PCI_AD[21]	E20	I/O	$NVDD2_{OFF}$	—
PCI_AD[22]	A23	I/O	$NVDD2_{OFF}$	—
PCI_AD[23]	C22	I/O	$NVDD2_{OFF}$	—
PCI_AD[24]	E19	I/O	$NVDD2_{OFF}$	—
PCI_AD[25]	A22	I/O	$NVDD2_{OFF}$	—
PCI_AD[26]	C20	I/O	$NVDD2_{OFF}$	—
PCI_AD[27]	B21	I/O	$NVDD2_{OFF}$	—
PCI_AD[28]	D19	I/O	$NVDD2_{OFF}$	—
PCI_AD[29]	A19	I/O	$NVDD2_{OFF}$	—
PCI_AD[30]	A21	I/O	$NVDD2_{OFF}$	—
PCI_AD[31]	B19	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[0]	H24	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[1]	C27	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[2]	A25	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[3]	E21	I/O	$NVDD2_{OFF}$	—
PCI_PAR	G24	I/O	$NVDD2_{OFF}$	—
$\overline{PCI\_FRAME}$	C28	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_TRDY}$	A24	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_IRDY}$	D25	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_STOP}$	D23	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_DEVSEL}$	E22	I/O	$NVDD2_{OFF}$	5
PCI_IDSEL	D26	I	$NVDD2_{OFF}$	—
$\overline{PCI\_SERR}$	C25	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_PERR}$	D21	I/O	$NVDD2_{OFF}$	5

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
USB_DP	A11	I/O	USB_VDDA	—
USB_DM	A12	I/O	USB_VDDA	—
USB_VBUS	C12	I	—	—
USB_TPA	A14	O	—	—
USB_RBIAS	D14	I	—	8
USB_PLL_PWR3	A13	I	—	—
USB_PLL_GND0 & USB_PLL_GND1	D13	I	—	—
USB_PLL_PWR1	B13	I	—	—
USB_VSSA_BIAS	E14	I	—	—
USB_VDDA_BIAS	C14	I	—	—
USB_VSSA	E13	I	—	—
USB_VDDA	E12	I	—	—
GPIO				
GPIO_0/$\overline{\text{DMA\_DREQ1}}$/$\overline{\text{GTM1\_TOUT1}}$	C5	I/O	$NVDD1_{ON}$	—
GPIO_1/$\overline{\text{DMA\_DACK1}}$/GTM1_TIN2/GTM2_TIN1	A4	I/O	$NVDD1_{ON}$	—
GPIO_2/$\overline{\text{DMA\_DONE1}}$/$\overline{\text{GTM1\_TGATE2}}$/$\overline{\text{GTM2\_TGATE1}}$	K3	I/O	$NVDD4_{OFF}$	—
GPIO_3/GTM1_TIN3/GTM2_TIN4	K1	I/O	$NVDD4_{OFF}$	—
GPIO_4/$\overline{\text{GTM1\_TGATE3}}$/$\overline{\text{GTM2\_TGATE4}}$	K2	I/O	$NVDD4_{OFF}$	—
GPIO_5/$\overline{\text{GTM1\_TOUT3}}$/$\overline{\text{GTM2\_TOUT1}}$	L5	I/O	$NVDD4_{OFF}$	—
GPIO_6/GTM1_TIN4/GTM2_TIN3	L3	I/O	$NVDD4_{OFF}$	—
GPIO_7/$\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$	L1	I/O	$NVDD4_{OFF}$	—
GPIO_8/USBDR_DRIVE_VBUS/GTM1_TIN1/GTM2_TIN2	M1	I/O	$NVDD4_{OFF}$	—
GPIO_9/USBDR_PWRFAULT/$\overline{\text{GTM1\_TGATE1}}$/$\overline{\text{GTM2\_TGATE2}}$	M2	I/O	$NVDD4_{OFF}$	—
GPIO_10/USBDR_PCTL0/$\overline{\text{GTM1\_TOUT2}}$/$\overline{\text{GTM2\_TOUT1}}$	M5	I/O	$NVDD4_{OFF}$	—
GPIO_11/USBDR_PCTL1/$\overline{\text{GTM1\_TOUT4}}$/$\overline{\text{GTM2\_TOUT3}}$	M4	I/O	$NVDD4_{OFF}$	—
SPI				
SPIMOSI/GPIO_15	W3	I/O	$NVDD1_{OFF}$	—
SPIMISO/GPIO_16	W4	I/O	$NVDD1_{OFF}$	—
SPICLK	Y1	I/O	$NVDD1_{OFF}$	—
SPISEL/GPIO_17	W2	I/O	$NVDD1_{OFF}$	—

24 Clocking

This figure shows the internal distribution of clocks within the MPC8315E.



1 Multiplication factor M = 1, 1.5, 2, 2.5, and 3. Value is decided by RCWLR[COREPLL].

2 Multiplication factor L = 2, 3, 4 and 5. Value is decided by RCWLR[SPMF].

Figure 62. MPC8315E Clock Subsystem

Table 73. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110–1111	Reserved

As described in Section 24, "Clocking," The LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ configuration input signal select the ratio between the primary clock input (SYS_CLK_IN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 74 and Table 75 shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN/PCI_SYNC_IN ratios.

Table 74. CSB Frequency Options for Host Mode

$\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ at Reset[1]	SPMF	csb_clk : Input Clock Ratio [2]	Input Clock Frequency (MHz)[2]		
			24	33.33	66.67
High/Low [3]	0010	2:1			133
High/Low	0011	3:1		100	—
High/Low	0100	4:1	96	133	—
High/Low	0101	5:1	120	—	—

1 $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ select the ratio between SYS_CLK_IN and PCI_SYNC_OUT.
2 SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.
3 In the Host mode it does not matter if the value is High or Low.

Table 75. CSB Frequency Options for Agent Mode

$\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio [2]	Input Clock frequency (MHz)[2]		
			25	33.33	66.67
High	0010	2: 1			133
High	0011	3: 1		100	—
High	0100	4: 1		133	—
High	0101	5: 1	120	—	—

1 $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ doubles csb_clk if set low.
2 SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

25.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

25.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum VDD, nominal NVDD, 105°C.

Table 80. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI Signals (not including PCI Output Clocks)	PCI Output Clocks (including PCI_SYNC_OUT)	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
R_P	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
Differential	NA	NA	NA	NA	Z_{DIFF}	Ω

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

26.6 Configuration Pin Multiplexing

The MPC8315E provides the user with power-on configuration options that can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{PORESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

26.7 Pull-Up Resistor Requirements

The MPC8315E requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C pins and EPIC interrupt pins.

For more information on required pull up resistors and the connections required for JTAG interface, see AN3438, MPC8315 Design Checklist

27 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 27.1, “Part Numbers Fully Addressed by this Document.”

27.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the MPC8315E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme

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