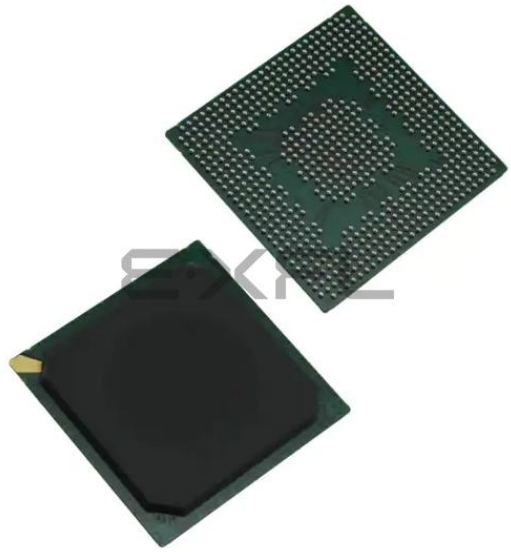

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Security; SEC 3.3
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8315evragda

2.12 Power Management Controller (PMC)

The MPC8315E supports a range of power management states that significantly lower power consumption under the control of the power management controller. The PMC includes the following features:

- Provides power management when the device is used in both PCI host and agent modes
- PCI Power Management 1.2 D0, D1, D2, D3hot, and D3cold states
- PME generation in PCI agent mode, PME detection in PCI host mode
- Wake-up from Ethernet (magic packet), USB, GPIO, and PCI (PME input as host) while in the D1, D2 and D3hot states
- A new low-power standby power management state called D3warm
  - The PMC, one Ethernet port, and the GTM block remain powered via a split power supply controlled through an external power switch
  - Wake-up events include Ethernet (magic packet), GTM, GPIO, or IRQ inputs and cause the device to transition back to normal operation
  - PCI agent mode is not be supported in D3warm state
- PCI Express-based PME events are not supported

2.13 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the MPC8315E to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

2.14 DMA Controller, I^2C, DUART, Enhanced Local Bus Controller (eLBC), and Timers

The integrated four-channel DMA controller includes the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters)
- Misaligned transfer capability for source/destination address
- Supports external DREQ, DACK and DONE signals

There is one I^2C controller. This synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The eLBC port allows connections with a wide variety of external DSPs and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices

This figure shows the SATA power supplies.

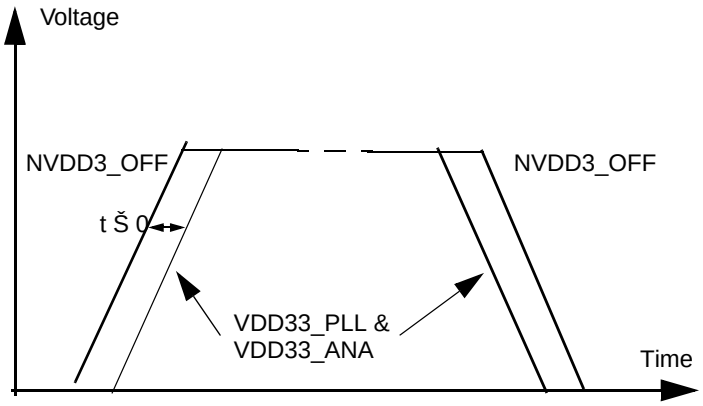

Figure 5. SATA Power Supplies

4 Power Characteristics

This table shows the estimated typical power dissipation for this family of devices.

Table 4. MPC8315E Power Dissipation

(Does not include I/O power dissipation)

Core Frequency (MHz)	CSB Frequency (MHz)	Typical [1,3]	Maximum [1,2]	Unit
266	133	1.116	1.646	W
333	133	1.142	1.665	W
400	133	1.167	1.690	W

Note:

1. The values do not include I/O supply power, but do include core, AVDD, USB PLL, digital SerDes power, and SATA PHY power.
2. Maximum power is based on a voltage of V_{dd} = 1.05V, a junction temperature of T_j = 105°C, and an artificial smoker test.
3. Typical power is based on a voltage of V_{dd} = 1.05V, and an artificial smoker test running at room temperature.

This table shows the estimated typical I/O power dissipation for this family of devices.

Table 5. MPC8315E Power Dissipation

Interface	Frequency	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	NV_{DD} (3.3 V)	LVDD1_OFF/ LVDD2_ON (3.3V)	LVDD2 _ON (3.3V)	VDD33PLL, VDD33ANA (3.3V)	SATA_VDD, VDD1IO, VDD1ANA (1.0V)	XCOREVDD, XPADVDD, SDAVDD (1.0V)	Unit
DDR 1 Rs = 22Ω Rt = 50Ω	266MHz, 32 bits	—	0.323	—	—	—	—	—	—	W
	200MHz, 32 bits	—	0.291	—	—	—	—	—	—	W

Table 11. DDR2 SDRAM DC Electrical Characteristics for GVDD(typ) = 1.8 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Note

Note:
1. GVDD is expected to be within 50 mV of the DRAM GVDD at all times.
2. MVREF is expected to be equal to 0.5 × GVDD, and to track GVDD DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GVDD.

This table provides the DDR2 capacitance when GVDD(typ) = 1.8 V.

Table 12. DDR2 SDRAM Capacitance for GVDD(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GVDD = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8315E when GVDD(typ) = 2.5 V.

Table 13. DDR SDRAM DC Electrical Characteristics for GVDD(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GVDD	2.3	2.7	V	1
I/O reference voltage	MVREF	0.49 × GVDD	0.51 × GVDD	V	2
I/O termination voltage	V_{TT}	MVREF – 0.04	MVREF + 0.04	V	3
Input high voltage	V_{IH}	MVREF + 0.15	GVDD + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF – 0.15	V	—
Output leakage current	I_{OZ}	–9.9	–9.9	μA	4
Output high current (V_{OUT} = 1.95 V, GVDD = 2.3V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Note:
1. GVDD is expected to be within 50 mV of the DRAM GVDD at all times.
2. MVREF is expected to be equal to 0.5 × GVDD, and to track GVDD DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GVDD.

This table provides the DDR capacitance when GVDD(typ) = 2.5 V.

Table 14. DDR SDRAM Capacitance for GVDD(typ) = 2.5 V Interface

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ,DQS	C_{IO}	6	8	pF	1

Table 28. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load.

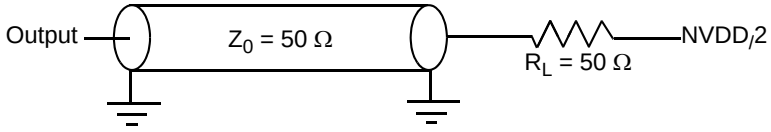

Figure 14. AC Test Load

This figure shows the RMII receive AC timing diagram.

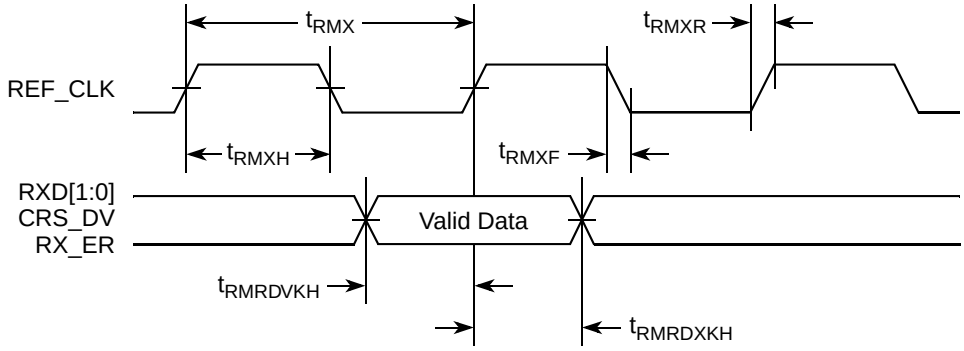

Figure 15. RMII Receive AC Timing Diagram

9.2.3 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 29. RGMII and RTBI AC Timing Specifications

At recommended operating conditions (see Table 2)

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	–0.6	—	0.6	ns
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.6	ns

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

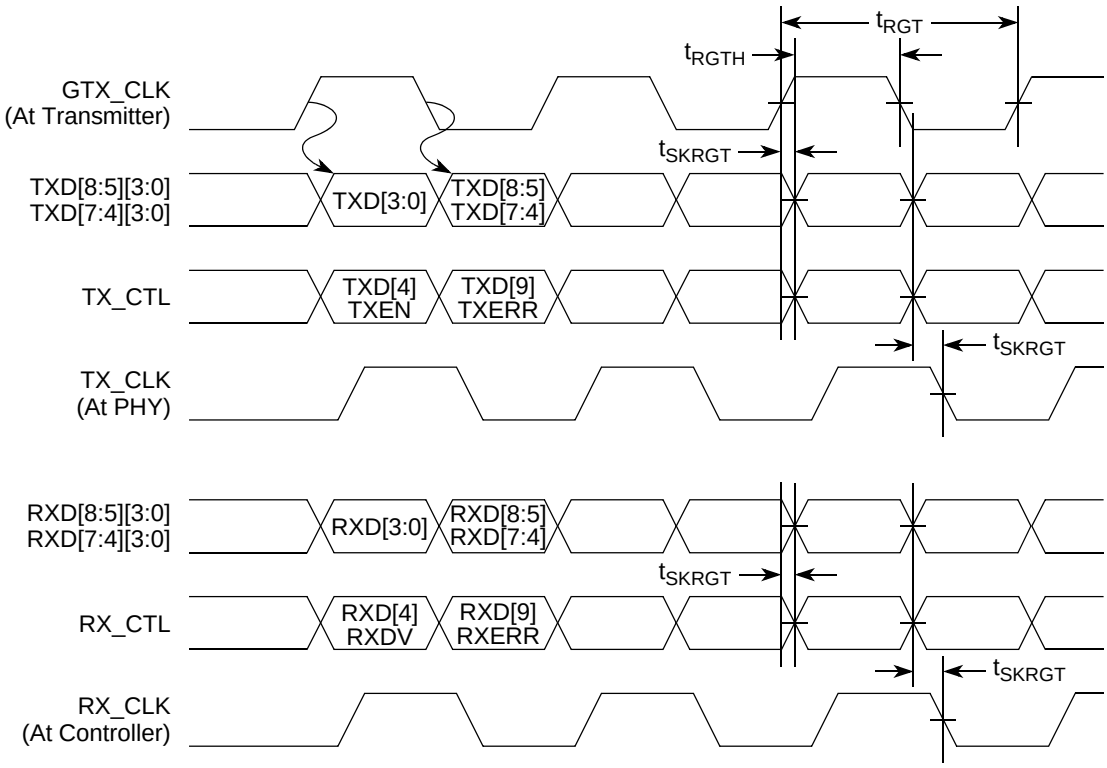

Figure 16. RGMII and RTBI AC Timing and Multiplexing Diagrams

9.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for MII, RMII, RGMII, and RTBI are specified in Section 9.1, "eTSEC (10/100/1000 Mbps)—MII/RMII/RGMII/RTBI Electrical Characteristics."

9.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Table 30. MII Management DC Electrical Characteristics Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	NVDD	—	—	3.0	3.6	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	NVDD = Min	2.10	NVDD + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	NVDD = Min	V_{SS}	0.50	V
Input high voltage	V_{IH}	—	—	2.00	—	V
Input low voltage	V_{IL}	—	—	—	0.80	V
Input high current	I_{IH}	NVDD = Max	V_{IN} [1] = 2.1 V	—	40	μA

Table 36. SGMII DC Receiver Electrical Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input AC common mode voltage	$V_{CM\_ACp\text{-}p}$	—	—	100	mV	5
Receiver differential input impedance	Z_{RX_DIFF}	80	100	120	Ω	—
Receiver common mode input impedance	Z_{RX_CM}	20	—	35	Ω	—
Common mode input voltage	V_{CM}	—	$V_{xcorevss}$	—	V	6

Note:
1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak to peak input differential voltage
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in PCI Express. Refer to PCI Express Differential Receiver (RX) Input Specifications section for further explanation.
4. The EQ shown in the table refers to the RXEQA or RXEQE bit field of MPC8315E's SerDes Control Register 0.
5. $V_{CM\_ACp\text{-}p}$ is also referred to as peak to peak AC common mode voltage.
6. On-chip termination to XCOREVSS.

9.5.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (TX[n] and $\overline{\text{TX}}$[n]) or at the receiver inputs (RX[n] and $\overline{\text{RX}}$[n]) as depicted in Figure 21 respectively.

9.5.4.1 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 37. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XCOREVDD = 1.0V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic Jitter	JD	—	—	0.17	UI p-p	—
Total Jitter	JT	—	—	0.35	UI p-p	—
Unit Interval	UI	799.92	800	800.08	ps	—
V_{OD} fall time (80%-20%)	tfall	50	—	120	ps	—
V_{OD} rise time (20%-80%)	t_{rise}	50	—	120	ps	—

Note:
1. Each UI is 800 ps ± 100 ppm.

9.5.4.2 SGMII Receive AC Timing Specifications

This table provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 20 shows the SGMII Receiver Input Compliance Mask eye diagram.

This figure provides the test access port timing diagram.

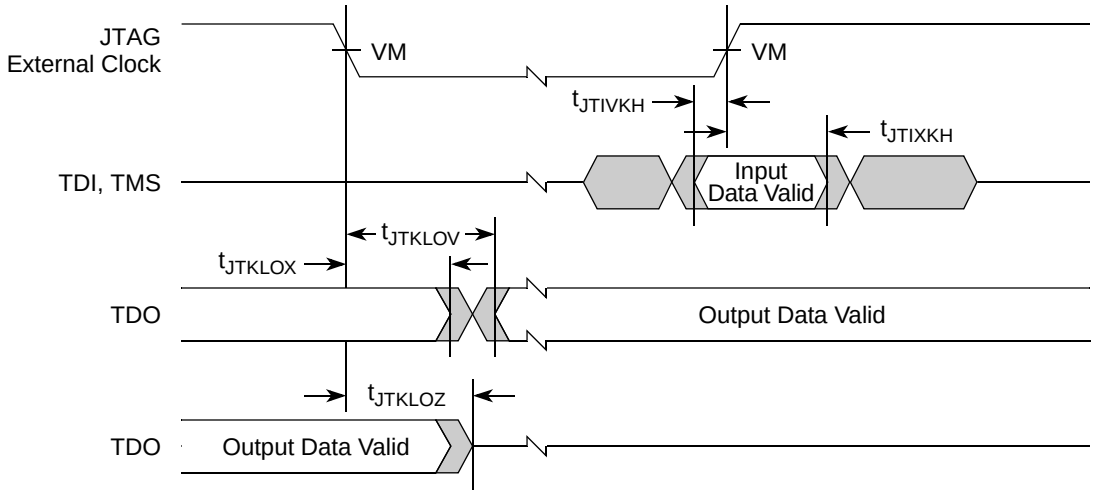

Figure 32. Test Access Port Timing Diagram

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8315E.

13.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interface.

Table 47. I²C DC Electrical Characteristics

At recommended operating conditions with NVDD of 3.3 V ± 300 mv

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage level	V_{IH}	0.7 × NVDD	NVDD + 0.3	V	—
Input low voltage level	V_{IL}	–0.3	0.3 × NVDD	V	—
Low level output voltage	V_{OL}	0	0.2 × NVDD	V	1
High level output voltage	V_{OH}	0.8 × NVDD	NVDD + 0.3	V	—
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	20 + 0.1 × C_B	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current (0 V ≤V_{IN} ≤ NVDD)	I_{IN}	—	± 5	μA	4

Note:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if NVDD is switched off.

This figure shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8315E SerDes reference clock input's DC requirement.

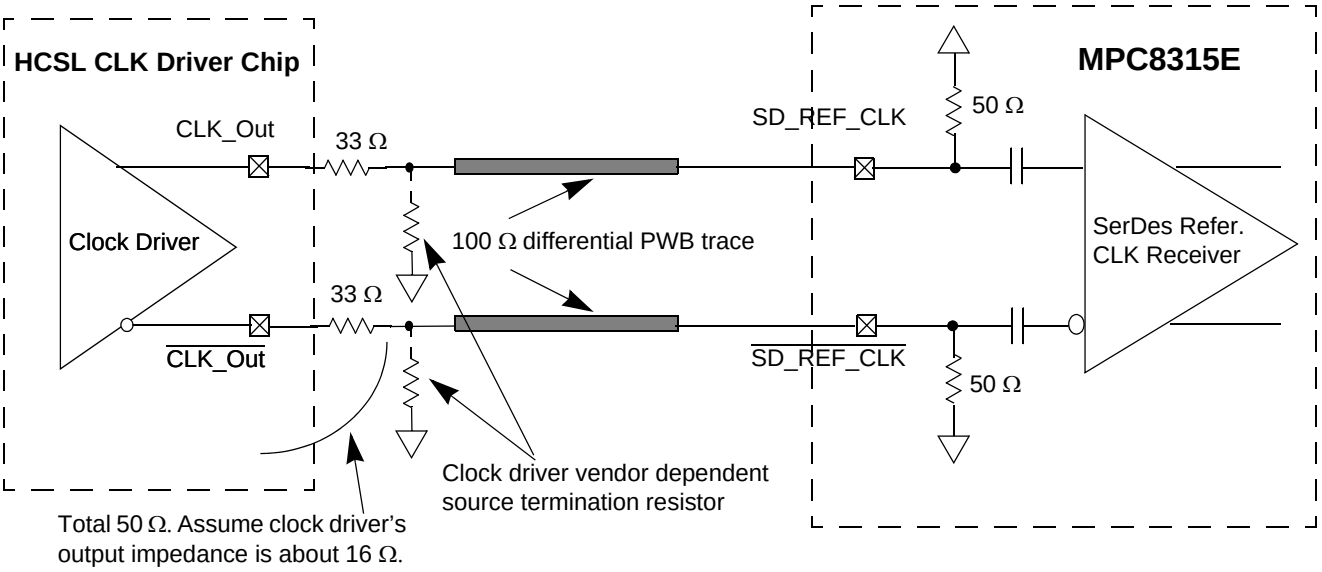

Figure 43. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8315E SerDes reference clock input's allowed range (100 to 400mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

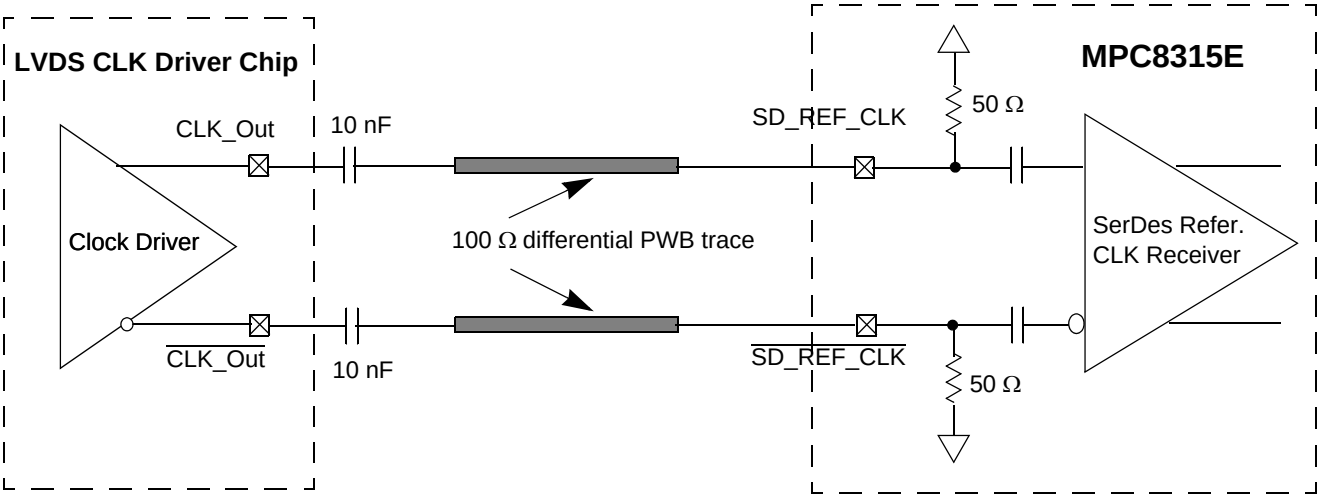

Figure 44. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 45 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8315E SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 45

16 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8315E.

16.1 DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK

For more information, see Section 15.2, "SerDes Reference Clocks."

16.2 AC Requirements for PCI Express SerDes Clocks

This table lists the PCI Express SerDes clock AC requirements.

Table 53. SD_REF_CLK and SD_REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Unit	Note
t_{REF}	REFCLK cycle time	—	10	—	ns	—
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	–50	—	50	ps	—

16.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

16.4 Physical Layer Specifications

Following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer please use the *PCI Express Base Specification*, Rev. 1.0a.

16.4.1 Differential Transmitter (TX) Output

This table defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 54. Differential Transmitter (TX) Output Specifications

Parameter	Symbol	Comments	Min	Typical	Max	Unit	Note
Unit interval	UI	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations.	399.88	400	400.12	ps	1
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	$V_{TX-DIFFp-p} = 2*\|V_{TX-D+} - V_{TX-D-}\|$	0.8	—	1.2	V	2

16.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 51 is specified using the passive compliance/test measurement load (see Figure 52) in place of any real PCI Express RX component. In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 52) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 51) expected at the input receiver based on an adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 Ω probes—see Figure 52). Note that the series capacitors, $C_{PEACCTX}$, are optional for the return loss measurement.

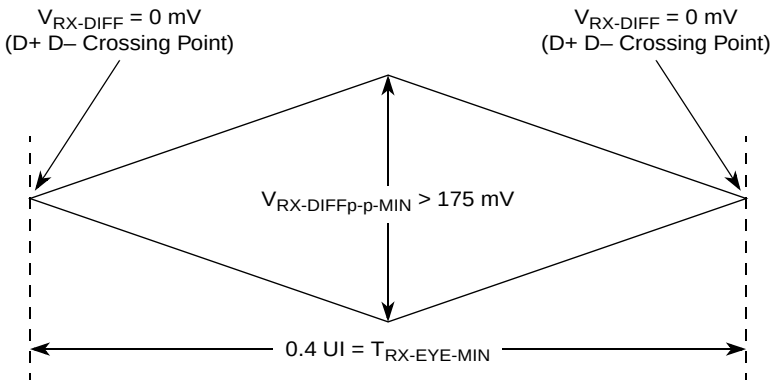

Figure 51. Minimum Receiver Eye Timing and Voltage Compliance Specification

16.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 52.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

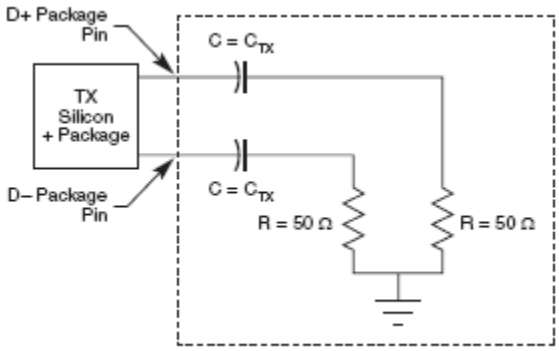

Figure 52. Compliance Test/Measurement Load

17 Serial ATA (SATA)

The serial ATA (SATA) of the MPC8315E is designed to comply with Serial ATA 2.5 Specification. Note that the external cabled applications or long backplane applications (Gen1x & Gen2x) are not supported.

17.1 Requirements for SATA REF_CLK

The reference clock for MPC8315E is a single ended input clock required for the SATA Interface operation. The AC requirements for the SATA reference clock are listed in the this table.

Table 56. Reference Clock Input Requirements

Parameter	Symbol	Conditions	Min	Typical	Max	Unit	Note
Frequency range	t_{CLK_REF}	—	50	75	150	MHz	1
Clock frequency tolerance	t_{CLK_TOL}	—	-350	0	+350	ppm	—
Input High Voltage	V_{CLK_INHI}	—	2.0	—	—	V	—
Input Low Voltage	V_{CLK_INLo}	—	—	—	0.7	V	—
Reference clock rise and fall time	t_{CLK_RISE}/ t_{CLK_FALL}	20% to 80% of nominal amplitude	—	—	2	ns	—
Reference clock duty cycle	t_{CLK_DUTY}	Measured at 1.6V	40	50	60	%	—

Table 61. Timers Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit

Note:
1. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers input are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure provides the AC test load for the Timers.

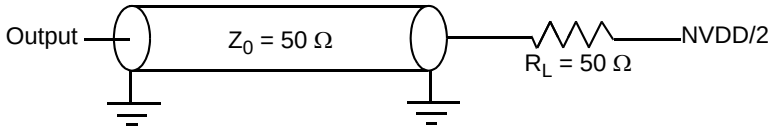

Figure 54. Timers AC Test Load

19 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8315E.

19.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO.

Table 62. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le$ NVDD	—	± 5	μA

19.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 63. GPIO Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Note:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
JTAG				
TCK	E5	I	$NVDD1_{ON}$	—
TDI	B4	I	$NVDD1_{ON}$	4
TDO	C4	O	$NVDD1_{ON}$	3
TMS	C3	I	$NVDD1_{ON}$	4
$\overline{\text{TRST}}$	C2	I	$NVDD1_{ON}$	4
TDM				
GPIO_18/TDM_RCK	AB1	I/O	$NVDD1_{OFF}$	—
GPIO_20/TDM_RD	AC1	I/O	$NVDD1_{OFF}$	—
GPIO_19/TDM_RFS	AB3	I/O	$NVDD1_{OFF}$	—
GPIO_21/TDM_TCK	AB5	I/O	$NVDD1_{OFF}$	—
GPIO_23/TDM_TD	AC3	I/O	$NVDD1_{OFF}$	—
GPIO_22/TDM_TFS	AC2	I/O	$NVDD1_{OFF}$	—
SATA				
PINRXMINUSA	N28	I	VDD1IO	—
PINRXMINUSB	U28	I	VDD1IO	—
PINRXPLUSA	M28	I	VDD1IO	—
PINRXPLUSB	T28	I	VDD1IO	—
PINTXMINUSA	M25	O	VDD1IO	—
PINTXMINUSB	P26	O	VDD1IO	—
PINTXPLUSA	N25	O	VDD1IO	—
PINTXPLUSB	R26	O	VDD1IO	—
SATA_ANAVIZ	U26	O	—	—
SATA_CLK_IN	V27	I	NVDD3_OFF	—
SATA_VDD	N27	I	—	—
SATA_VDD	U23	I	—	—
SATA_VSS	M27	I	—	—
SATA_VSS	V28	I	—	—
VSSRESREF	T26	I	—	—
RESREF	T25	I	—	10
VDD33ANA	U27	I	—	—
VDD33PLL	T27	I	—	—
TEST				
TEST_MODE	D6	I	$NVDD1_{ON}$	6
DEBUG				

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_AD[9]	F28	I/O	$NVDD2_{OFF}$	—
PCI_AD[10]	G25	I/O	$NVDD2_{OFF}$	—
PCI_AD[11]	F27	I/O	$NVDD2_{OFF}$	—
PCI_AD[12]	E27	I/O	$NVDD2_{OFF}$	—
PCI_AD[13]	E28	I/O	$NVDD2_{OFF}$	—
PCI_AD[14]	D28	I/O	$NVDD2_{OFF}$	—
PCI_AD[15]	D27	I/O	$NVDD2_{OFF}$	—
PCI_AD[16]	B25	I/O	$NVDD2_{OFF}$	—
PCI_AD[17]	D24	I/O	$NVDD2_{OFF}$	—
PCI_AD[18]	B26	I/O	$NVDD2_{OFF}$	—
PCI_AD[19]	C24	I/O	$NVDD2_{OFF}$	—
PCI_AD[20]	A26	I/O	$NVDD2_{OFF}$	—
PCI_AD[21]	E20	I/O	$NVDD2_{OFF}$	—
PCI_AD[22]	A23	I/O	$NVDD2_{OFF}$	—
PCI_AD[23]	C22	I/O	$NVDD2_{OFF}$	—
PCI_AD[24]	E19	I/O	$NVDD2_{OFF}$	—
PCI_AD[25]	A22	I/O	$NVDD2_{OFF}$	—
PCI_AD[26]	C20	I/O	$NVDD2_{OFF}$	—
PCI_AD[27]	B21	I/O	$NVDD2_{OFF}$	—
PCI_AD[28]	D19	I/O	$NVDD2_{OFF}$	—
PCI_AD[29]	A19	I/O	$NVDD2_{OFF}$	—
PCI_AD[30]	A21	I/O	$NVDD2_{OFF}$	—
PCI_AD[31]	B19	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[0]	H24	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[1]	C27	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[2]	A25	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[3]	E21	I/O	$NVDD2_{OFF}$	—
PCI_PAR	G24	I/O	$NVDD2_{OFF}$	—
$\overline{PCI\_FRAME}$	C28	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_TRDY}$	A24	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_IRDY}$	D25	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_STOP}$	D23	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_DEVSEL}$	E22	I/O	$NVDD2_{OFF}$	5
PCI_IDSEL	D26	I	$NVDD2_{OFF}$	—
$\overline{PCI\_SERR}$	C25	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_PERR}$	D21	I/O	$NVDD2_{OFF}$	5

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_REQ0	E18	I/O	$NVDD2_{OFF}$	—
PCI_REQ1/CPCI_HS_ES	C18	I	$NVDD2_{OFF}$	—
PCI_REQ2	E17	I	$NVDD2_{OFF}$	—
PCI_GNT0	B20	I/O	$NVDD2_{OFF}$	—
PCI_GNT1/CPCI_HS_LED	D17	O	$NVDD2_{OFF}$	—
PCI_GNT2/CPCI_HS_ENUM	E15	O	$NVDD2_{OFF}$	—
M66EN	L24	I	$NVDD2_{OFF}$	—
PCI_CLK0	E23	O	$NVDD2_{OFF}$	—
PCI_CLK1	F24	O	$NVDD2_{OFF}$	—
PCI_CLK2	E25	O	$NVDD2_{OFF}$	—
PCI_PME	B23	I/O	$NVDD2_{OFF}$	2
ETSEC1/_USBULPI				
GPIO_24/TSEC1_COL/USBDR_TXDRXD0	J1	I/O	$LVDD1_{OFF}$	—
GPIO_25/TSEC1_CRS/USBDR_TXDRXD1	H1	I/O	$LVDD1_{OFF}$	—
TSEC1_GTX_CLK/USBDR_TXDRXD2	K5	I/O	$LVDD1_{OFF}$	3
TSEC1_RX_CLK/USBDR_TXDRXD3	J4	I/O	$LVDD1_{OFF}$	—
TSCE1_RX_DV/USBDR_TXDRXD4	J2	I/O	$LVDD1_{OFF}$	—
TSEC1_RXD[3]/USBDR_TXDRXD5	G1	I/O	$LVDD1_{OFF}$	—
TSEC1_RXD[2]/USBDR_TXDRXD6	H3	I/O	$LVDD1_{OFF}$	—
TSEC1_RXD[1]/USBDR_TXDRXD7/TSEC_TMR_CLK	J5	I/O	$LVDD1_{OFF}$	—
TSEC1_RXD[0]/USBDR_NXT/TSEC_TMR_TRIG1	H2	I	$LVDD1_{OFF}$	—
TSEC1_RX_ER/USBDR_DIR/TSEC_TMR_TRIG2	H5	I	$LVDD1_{OFF}$	—
TSEC1_TX_CLK/USBDR_CLK	G2	I	$LVDD1_{OFF}$	—
GPIO_28/TSEC1_TXD[3]/TSEC_TMR_GCLK	F3	I/O	$LVDD1_{OFF}$	—
GPIO_29/TSEC1_TXD[2]/TSEC_TMR_PP1	F2	I/O	$LVDD1_{OFF}$	—
GPIO_30/TSEC1_TXD[1]/TSEC_TMR_PP2	F1	I/O	$LVDD1_{OFF}$	—
TSEC1_TXD[0]/USBDR_STP/ TSEC_TMR_PP3	G4	O	$LVDD1_{OFF}$	12
GPIO_31/TSEC1_TX_EN/TSEC_TMR_ALARM1	F4	I/O	$LVDD1_{OFF}$	—
TSEC1_TX_ER/TSEC_TMR_ALARM2	G5	O	$LVDD1_{OFF}$	—
TSEC_GTX_CLK125	D1	I	$NVDD1_{ON}$	—
TSEC_MDC/LB_POR_CFG_BOOT_ECC	E3	I/O	$NVDD1_{ON}$	9
TSEC_MDIO	E2	I/O	$NVDD1_{ON}$	

The primary clock source can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the device is configured as a PCI host device, SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the SYS_CLK_IN signal should be tied to GND.

As shown in Figure 62, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbiu_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{\text{PCI\_SYNC\_IN} \times (1 + \sim \overline{\text{CFG\_SYS\_CLKIN\_DIV}})\} \times \text{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + ~ $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$) is the SYS_CLK_IN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + \text{RCWL[DDRCM]})$$

Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbiu_clk* frequency is determined by the following equation:

$$lbiu\_clk = csb\_clk \times (1 + \text{RCWL[LBCM]})$$

Note that *lbiu_clk* is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LCLK[0:1]). The LBIU clock divider ratio is controlled by LCRR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 71 specifies which units have a configurable clock frequency.

Table 73. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110–1111	Reserved

As described in Section 24, "Clocking," The LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ configuration input signal select the ratio between the primary clock input (SYS_CLK_IN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 74 and Table 75 shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN/PCI_SYNC_IN ratios.

Table 74. CSB Frequency Options for Host Mode

$\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ at Reset[1]	SPMF	csb_clk : Input Clock Ratio [2]	Input Clock Frequency (MHz)[2]		
			24	33.33	66.67
High/Low [3]	0010	2:1			133
High/Low	0011	3:1		100	—
High/Low	0100	4:1	96	133	—
High/Low	0101	5:1	120	—	—

1 $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ select the ratio between SYS_CLK_IN and PCI_SYNC_OUT.
2 SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.
3 In the Host mode it does not matter if the value is High or Low.

Table 75. CSB Frequency Options for Agent Mode

$\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio [2]	Input Clock frequency (MHz)[2]		
			25	33.33	66.67
High	0010	2: 1			133
High	0011	3: 1		100	—
High	0100	4: 1		133	—
High	0101	5: 1	120	—	—

1 $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ doubles csb_clk if set low.
2 SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

Table 77. Suggested PLL Configurations

Conf. No.	SPMF	Core\PLL	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)
6	0010	0000101	66.67	133.33	333.33
7	0101	0000110	25	125	375
8	0100	0000110	33.33	133.33	400
9	0010	0000110	66.67	133.33	400

25 Thermal

This section describes the thermal specifications of the MPC8315E.

25.1 Thermal Characteristics

This table provides the package thermal characteristics for the 620 29 × 29 mm TEPBGA II.

Table 78. Package Thermal Characteristics for TEPBGA II

Characteristic	Board type	Symbol	Value	Unit	Note
Junction to ambient natural convection	Single layer board (1s)	$R_{\theta JA}$	23	°C/W	1, 2
Junction to ambient natural convection	Four layer board (2s2p)	$R_{\theta JA}$	16	°C/W	1, 2, 3
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	18	°C/W	1, 3
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	13	°C/W	1, 3
Junction to board	—	$R_{\theta JB}$	8	°C/W	4
Junction to case	—	$R_{\theta JC}$	6	°C/W	5
Junction to package top	Natural convection	Ψ_{JT}	6	°C/W	6

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum VDD, nominal NVDD, 105°C.

Table 80. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI Signals (not including PCI Output Clocks)	PCI Output Clocks (including PCI_SYNC_OUT)	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
R_P	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
Differential	NA	NA	NA	NA	Z_{DIFF}	Ω

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

26.6 Configuration Pin Multiplexing

The MPC8315E provides the user with power-on configuration options that can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{PORESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

26.7 Pull-Up Resistor Requirements

The MPC8315E requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C pins and EPIC interrupt pins.

For more information on required pull up resistors and the connections required for JTAG interface, see AN3438, MPC8315 Design Checklist

27 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 27.1, “Part Numbers Fully Addressed by this Document.”

27.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the MPC8315E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme

28 Revision History

This table summarizes a revision history for this document.

Table 83. Revision History

Revision	Date	Substantive Change(s)
2	11/2011	• In Table 70: – Corrected Note 11 to pull down. – Note 10 added to RESREF pin. Removed all other instances of Note 10. – Added pull up information.
1	11/2011	• Added Notes 4, 5, 6, and 7 in Table 2. • In Table 6: – Decoupled PCI_CLK and SYS_CLK_IN rise and fall times. – Relaxed maximum rise/fall time of SYS_CLK_IN from 1.2 ns to 4 ns. – Modified Note 2. – Updated SYS_CLK_IN/PCI_CLK frequency from 66 MHz to 66.67 MHz. • Added Note 4 to Table 9. • Added a note stating “eTSEC should be interfaced with peripheral operating at same voltage level.” in Section 9.1.1, “MII, RMII, RGMII, and RTBI DC Electrical Characteristics.” • Added a note in Table 26 stating “The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm." • Added a note in Table 29 stating “The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm • In Table 42, changed min/max values of t_{CLK_TOL} from 0.05 to 0.005. • Added $t_{LALEHOV}$ parameter to Table 44 • Replaced 50 with 50 Ω in Section 16.5, “Receiver Compliance Eye Diagrams.” • In Table 70: – Added Pull up and Pull down information. – Removed Note 2 from TSEC_MDIO. • Removed configuration 2 from Table 77. • Removed Preliminary from Section 25, “Thermal.” • Removed MDIO signal from Section 26.7, “Pull-Up Resistor Requirements” as this signal is not open drain. • Replaced LCCR with LCRR throughout. • Replaced SYS_CLKIN with SYS_CLK_IN throughout. • Replaced all LBIUCM with LBCM. • Replaced all SYS_CR_CLK_IN and SYS_CR_CLK_OUT with SYS_XTAL_IN and SYS_XTAL_OUT, respectively. Replaced all USB_CR_CLK_IN and USB_CR_CLK_OUT with USB_XTAL_IN and USB_XTAL_OUT, respectively. • Added rise/fall time spec for TDM CLK
0	05/2009	Initial public release