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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8315vradda

This figure shows the SATA power supplies.

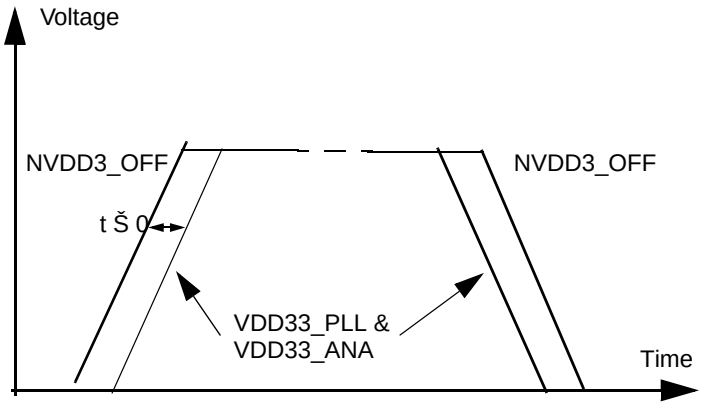


Figure 5. SATA Power Supplies

4 Power Characteristics

This table shows the estimated typical power dissipation for this family of devices.

Table 4. MPC8315E Power Dissipation

(Does not include I/O power dissipation)

Core Frequency (MHz)	CSB Frequency (MHz)	Typical [1,3]	Maximum [1,2]	Unit
266	133	1.116	1.646	W
333	133	1.142	1.665	W
400	133	1.167	1.690	W

Note:

1. The values do not include I/O supply power, but do include core, AVDD, USB PLL, digital SerDes power, and SATA PHY power.
2. Maximum power is based on a voltage of V_{dd} = 1.05V, a junction temperature of T_j = 105°C, and an artificial smoker test.
3. Typical power is based on a voltage of V_{dd} = 1.05V, and an artificial smoker test running at room temperature.

This table shows the estimated typical I/O power dissipation for this family of devices.

Table 5. MPC8315E Power Dissipation

Interface	Frequency	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	NV_{DD} (3.3 V)	LVDD1_OFF/ LVDD2_ON (3.3V)	LVDD2 _ON (3.3V)	VDD33PLL, VDD33ANA (3.3V)	SATA_VDD, VDD1IO, VDD1ANA (1.0V)	XCOREVDD, XPADVDD, SDAVDD (1.0V)	Unit
DDR 1 Rs = 22Ω Rt = 50Ω	266MHz, 32 bits	—	0.323	—	—	—	—	—	—	W
	200MHz, 32 bits	—	0.291	—	—	—	—	—	—	W

5.1 DC Electrical Characteristics

This table provides the clock input (SYS_CLK_IN/PCI_SYNC_IN) DC timing specifications for the MPC8315E.

Table 6. SYS_CLK_IN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	NVDD + 0.3	V
Input low voltage	—	V_{IL}	-0.3	0.4	V
SYS_CLK_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
SYS_XTAL_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±40	μA
PCI_SYNC_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
RTC_CLK input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
USB_CLK_IN input current	0 V ≤ V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
USB_XTAL_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±40	μA
SATA_CLK_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA

5.2 AC Electrical Characteristics

The primary clock source for the MPC8315E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (SYS_CLK_IN/PCI_CLK) AC timing specifications for the MPC8315E.

Table 7. SYS_CLK_IN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
SYS_CLK_IN/PCI_CLK frequency	$f_{SYS\_CLK\_IN}$	24	—	66.67	MHz	1, 6, 7
SYS_CLK_IN/PCI_CLK cycle time	$t_{SYS\_CLK\_IN}$	15	—	41.6	ns	6
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	0.6	—	4	ns	2, 6
PCI_CLK rise and fall time	t_{PCH}, t_{PCL}	0.6	0.8	1.2	ns	2
SYS_CLK_IN/PCI_CLK duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3, 6
SYS_CLK_IN/PCI_CLK jitter	—	—	—	±150	ps	4, 5, 6

Note:

1. **Caution:** The system, core, and security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN/PCI_CLK are specified at 20% to 80% of signal swing.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
6. The parameter names PCI_CLK and PCI_SYNC_IN are used interchangeably in this document.
7. Spread spectrum is allowed up to 1% down-spread at 33kHz.(max. rate).

Table 9. RESET Initialization Timing Specifications (continued)

Note:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the SYS_CLK_IN input, and PCI_SYNC_IN period depends on the value of CFG_SYS_CLKIN_DIV.
2. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN. It is only valid when the device is in PCI host mode.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:3] and CFG_SYS_CLKIN_DIV.
4. The parameter names CFG_SYS_CLKIN_DIV and CFG_CLKIN_DIV are used interchangeably in this document.

This table provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
System PLL lock times	—	100	μs	—
e300 core PLL lock times	—	100	μs	—
SerDes (SGMII/PCI Exp Phy) PLL lock times	—	100	μs	—
USB phy PLL lock times	—	100	μs	—
SATA phy PLL lock times	—	100	μs	—

7 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8315E. Note that DDR SDRAM is GVDD(typ) = 2.5 V and DDR2 SDRAM is GVDD(typ) = 1.8 V.

7.1 DDR and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8315E when GVDD(typ) = 1.8 V.

Table 11. DDR2 SDRAM DC Electrical Characteristics for GVDD(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GVDD	1.7	1.9	V	1
I/O reference voltage	MVREF	0.49 × GVDD	0.51 × GVDD	V	2
I/O termination voltage	V_{TT}	MVREF – 0.04	MVREF + 0.04	V	3
Input high voltage	V_{IH}	MVREF+ 0.125	GVDD + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.420 V, GVDD= 1.7V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	

7.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions

Parameter	Symbol [1]	Min	Max	Unit	Note
MCK[n] cycle time at MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	7.5	10	ns	2
ADDR/CMD output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHAS}	 2.9 3.5	 — —	ns	3
ADDR/CMD output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHAX}	 3.15 4.20	 — —	ns	3
$\overline{\text{MCS}}$[n] output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHCS}	 3.15 4.20	 — —	ns	3
$\overline{\text{MCS}}$[n] output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHCX}	 3.15 4.20	 — —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ//MDM output setup with respect to MDQS 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 900 1000	 — —	ps	5
MDQ//MDM output hold with respect to MDQS 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 1100 1200	 — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

This figure provides the AC test load for the DDR bus.

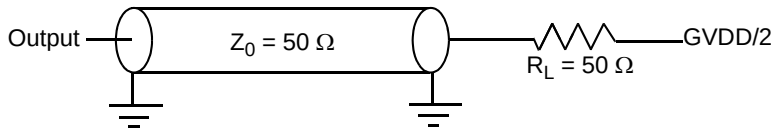


Figure 9. DDR AC Test Load

8 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

8.1 DUART DC Electrical Characteristics

This table lists the DC electrical characteristics for the DUART interface.

Table 21. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2.1	NVDD + 0.3	V
Low-level input voltage NVDD	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	NVDD – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V
Input current (0 V ≤V_{IN} ≤ NVDD)	I_{IN}	—	± 5	μA

8.2 DUART AC Electrical Specifications

This table lists the AC timing parameters for the DUART interface.

Table 22. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Note:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

9 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

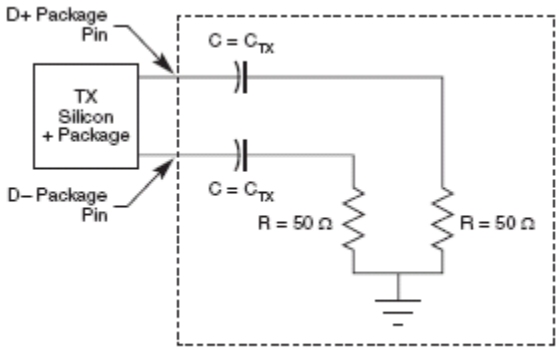


Figure 21. SGMII AC Test/Measurement Load

10 USB

10.1 USB Dual-Role Controllers

This section provides the AC and DC electrical specifications for the USB-ULPI interface.

10.1.1 USB DC Electrical Characteristics

This table lists the DC electrical characteristics for the USB interface.

Table 39. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	LVDD + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	LVDD – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

10.1.2 USB AC Electrical Specifications

This table lists the general timing parameters of the USB-ULPI interface.

Table 40. USB General Timing Parameters

Parameter	Symbol [1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	1, 2
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	1, 4
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	1, 4

Table 44. Local Bus General Timing Parameters (continued)

Parameter	Symbol [1]	Min	Max	Unit	Note
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD	t_{LBKHOZ}	—	4	ns	8
LALE output rise to LCLK negative edge	$t_{LALEHOV}$	—	3.0	ns	

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from NVDD/2 of the rising/falling edge of LCLK0 to 0.4 × NVDD of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.
8. For active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This figure provides the AC test load for the local bus.

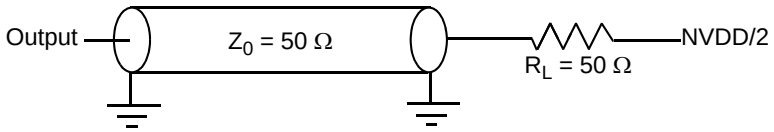


Figure 24. Local Bus AC Test Load

Figure 25 through Figure 27 show the local bus signals.

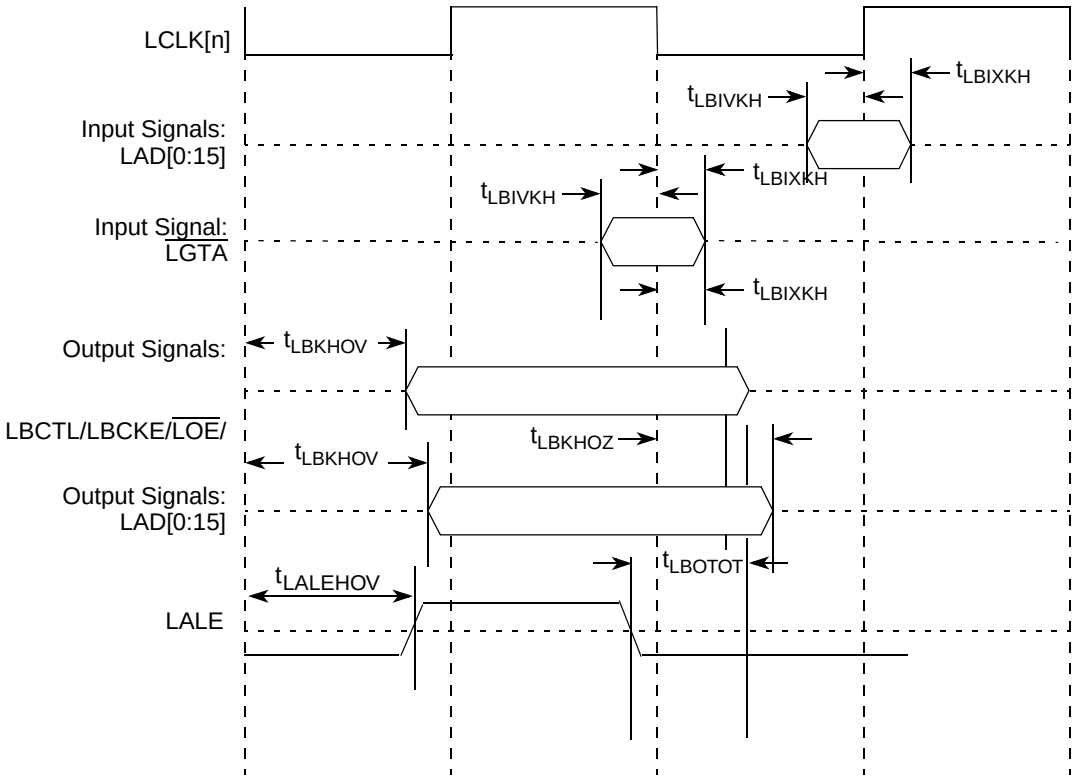


Figure 25. Local Bus Signals, Nonspecial Signals Only

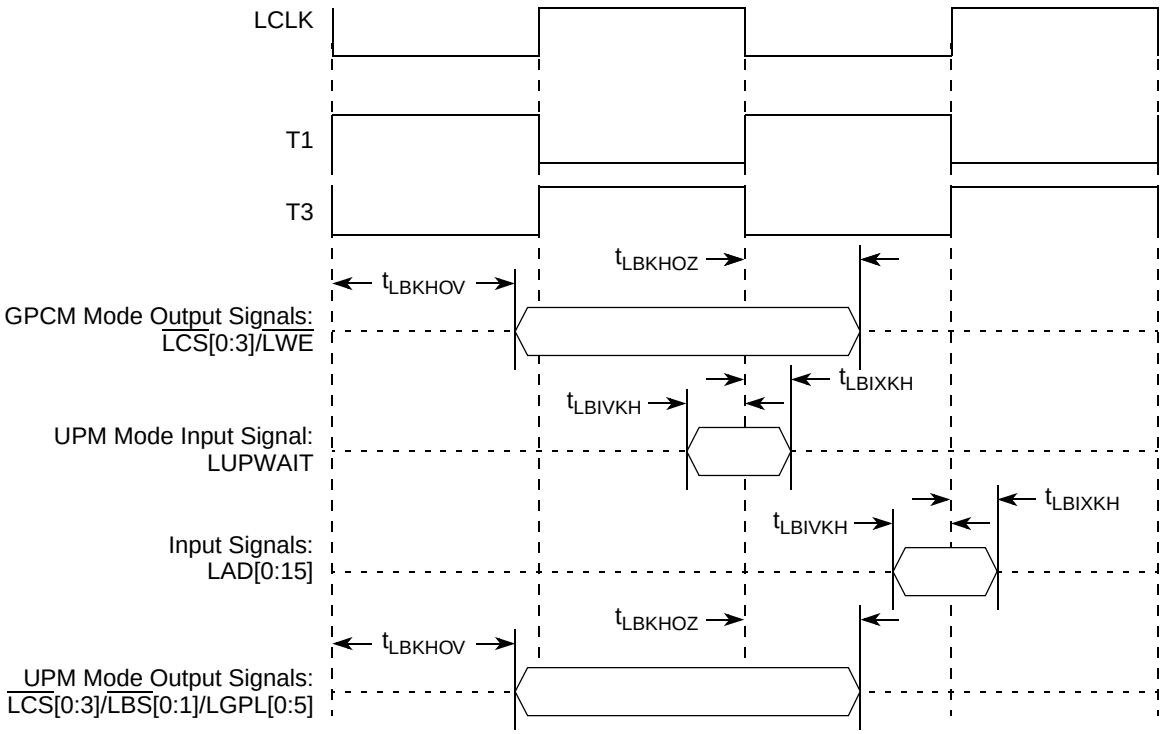


Figure 26. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2

The Differential Output Voltage (or Swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{TXn} - V_{\overline{TXn}}$. The V_{OD} value can be either positive or negative.

3. **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**):

   The Differential Input Voltage (or Swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{RXn} - V_{\overline{RXn}}$. The V_{ID} value can be either positive or negative.

4. **Differential Peak Voltage, V_{DIFFp}**

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. **Differential Peak-to-Peak, $V_{DIFFp-p}$**

   Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.

6. **Differential Waveform**

   The differential waveform is constructed by subtracting the inverting signal ($\overline{TXn}$, for example) from the non-inverting signal (TXn, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 47 as an example for differential waveform.

7. **Common Mode Voltage, V_{cm}**

   The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{TXn} + V_{\overline{TXn}})/2 = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It's also referred as the DC offset in some occasion.

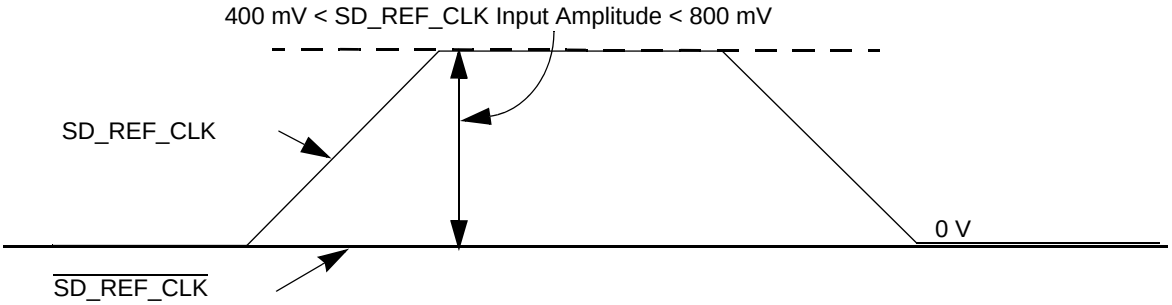


Figure 42. Single-Ended Reference Clock Input DC Requirements

15.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to XCOREVSS, the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 43–Figure 46 are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it’s very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8315E SerDes reference clock receiver requirement provided in this document.

assumes that the LVPECL clock driver's output impedance is 50Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140Ω to 240Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8315E SerDes reference clock's differential input amplitude requirement (between 200mV and 800mV differential peak). For example, if the LVPECL output's differential peak is 900mV and the desired SerDes reference clock input amplitude is selected as 600mV, the attenuation factor is 0.67, which requires R2 = 25Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

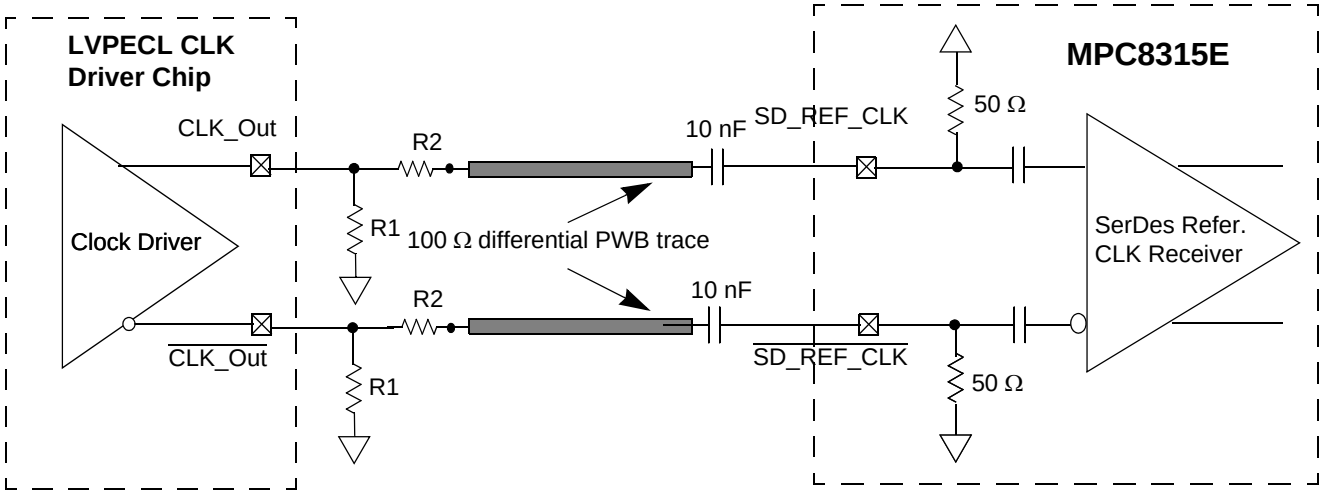


Figure 45. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8315E SerDes reference clock input's DC requirement.

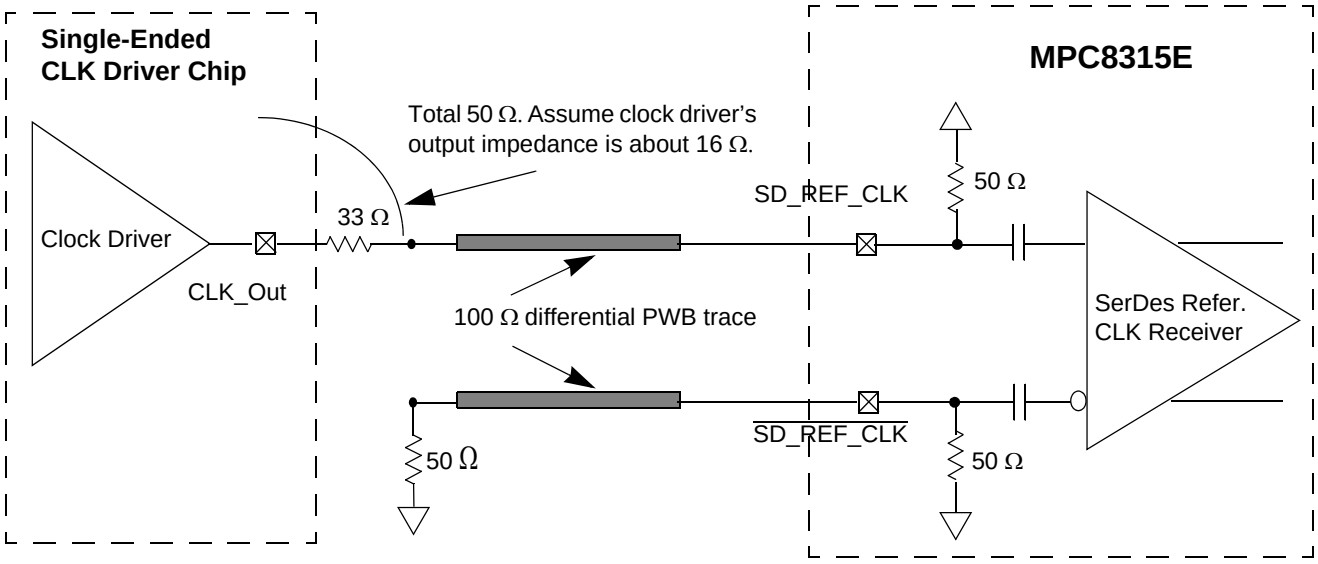


Figure 46. Single-Ended Connection (Reference Only)

16.4.3 Differential Receiver (RX) Input Specifications

This table defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 55. Differential Receiver (RX) Input Specifications

Parameter	Symbol	Comments	Min	Typical	Max	Unit	Note
Unit interval	UI	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations.	399.88	400	400.12	ps	1
Differential peak-to-peak output voltage	$V_{RX-DIFFp-p}$	$V_{RX-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$	0.175	—	1.200	V	2
Minimum receiver eye width	T_{RX-EYE}	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - U_{RX-EYE}$= 0.6 UI.	0.4	—	—	UI	2, 3
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.	—	—	0.3	UI	2, 3, 7
AC peak common mode input voltage	$V_{RX-CM-ACp}$	$V_{RX-CM-ACp} = \|V_{RXD+} + V_{RXD-}\|/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\|V_{RX-D+} + V_{RX-D-}\|/2$	—	—	150	mV	2
Differential return loss	$RL_{RX-DIFF}$	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively.	15	—	—	dB	4
Common mode return loss	RL_{RX-CM}	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V.	6	—	—	dB	4
DC differential input impedance	$Z_{RX-DIFF-DC}$	RX DC differential mode impedance.	80	100	120	Ω	5
DC Input Impedance	Z_{RX-DC}	Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance).	40	50	60	Ω	2, 5

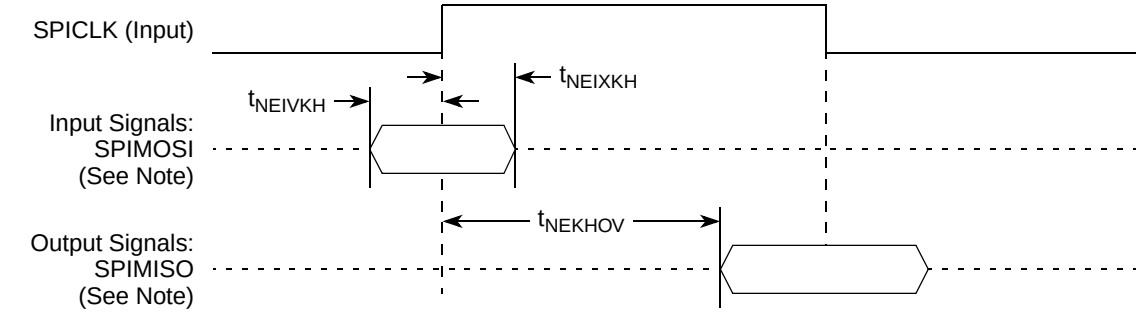
Table 55. Differential Receiver (RX) Input Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Unit	Note
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power.	200 k	—	—	Ω	6
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	V_{PEEIDT} = 2*|V_{RX-D+} -V_{RX-D-}| Measured at the package pins of the Receiver	65	—	175	mV	—
Unexpected Electrical Idle Enter Detect Threshold Integration Time	$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	An unexpected Electrical Idle (Vrx-diffp-p < Vrx-idle-det-diffp-p) must be recognized no longer than Trx-idle-det-diff-entertime to signal an unexpected idle condition.	—	—	10	ms	—
Total Skew	$L_{RX-SKEW}$	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (e.g. COM and one to five SKP Symbols) at the RX as well as any delay differences arising from the interconnect itself.	—	—	20	ns	—

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 52 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 51). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 52). Note that the series capacitors, C_{TX}, is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
6. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

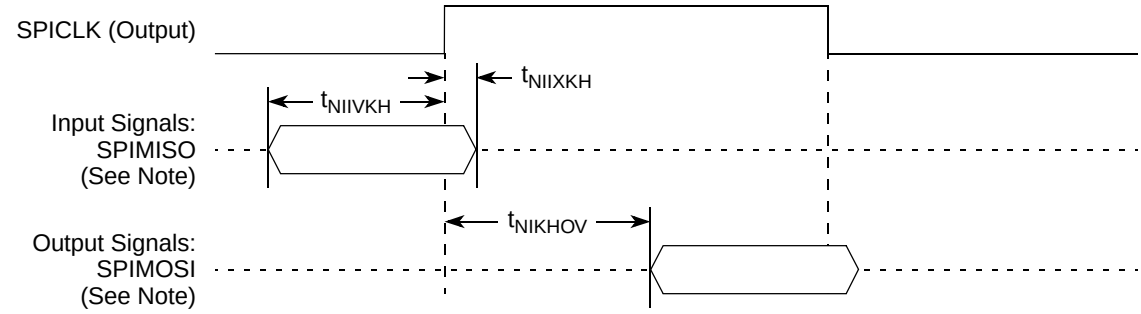
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 57. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 58. SPI AC Timing in Master Mode (Internal Clock) Diagram

22 TDM

This section describes the DC and AC electrical specifications for the TDM of the MPC8315E.

22.1 TDM DC Electrical Characteristics

This table provides the DC electrical characteristics TDM.

Table 68. TDM DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NVDD	—	± 5	μA

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
JTAG				
TCK	E5	I	$NVDD1_{ON}$	—
TDI	B4	I	$NVDD1_{ON}$	4
TDO	C4	O	$NVDD1_{ON}$	3
TMS	C3	I	$NVDD1_{ON}$	4
$\overline{\text{TRST}}$	C2	I	$NVDD1_{ON}$	4
TDM				
GPIO_18/TDM_RCK	AB1	I/O	$NVDD1_{OFF}$	—
GPIO_20/TDM_RD	AC1	I/O	$NVDD1_{OFF}$	—
GPIO_19/TDM_RFS	AB3	I/O	$NVDD1_{OFF}$	—
GPIO_21/TDM_TCK	AB5	I/O	$NVDD1_{OFF}$	—
GPIO_23/TDM_TD	AC3	I/O	$NVDD1_{OFF}$	—
GPIO_22/TDM_TFS	AC2	I/O	$NVDD1_{OFF}$	—
SATA				
PINRXMINUSA	N28	I	VDD1IO	—
PINRXMINUSB	U28	I	VDD1IO	—
PINRXPLUSA	M28	I	VDD1IO	—
PINRXPLUSB	T28	I	VDD1IO	—
PINTXMINUSA	M25	O	VDD1IO	—
PINTXMINUSB	P26	O	VDD1IO	—
PINTXPLUSA	N25	O	VDD1IO	—
PINTXPLUSB	R26	O	VDD1IO	—
SATA_ANAVIZ	U26	O	—	—
SATA_CLK_IN	V27	I	NVDD3_OFF	—
SATA_VDD	N27	I	—	—
SATA_VDD	U23	I	—	—
SATA_VSS	M27	I	—	—
SATA_VSS	V28	I	—	—
VSSRESREF	T26	I	—	—
RESREF	T25	I	—	10
VDD33ANA	U27	I	—	—
VDD33PLL	T27	I	—	—
TEST				
TEST_MODE	D6	I	$NVDD1_{ON}$	6
DEBUG				

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_REQ0	E18	I/O	$NVDD2_{OFF}$	—
PCI_REQ1/CPCI_HS_ES	C18	I	$NVDD2_{OFF}$	—
PCI_REQ2	E17	I	$NVDD2_{OFF}$	—
PCI_GNT0	B20	I/O	$NVDD2_{OFF}$	—
PCI_GNT1/CPCI_HS_LED	D17	O	$NVDD2_{OFF}$	—
PCI_GNT2/CPCI_HS_ENUM	E15	O	$NVDD2_{OFF}$	—
M66EN	L24	I	$NVDD2_{OFF}$	—
PCI_CLK0	E23	O	$NVDD2_{OFF}$	—
PCI_CLK1	F24	O	$NVDD2_{OFF}$	—
PCI_CLK2	E25	O	$NVDD2_{OFF}$	—
PCI_PME	B23	I/O	$NVDD2_{OFF}$	2
ETSEC1/_USBULPI				
GPIO_24/TSEC1_COL/USBDR_TXDRXD0	J1	I/O	$LVDD1_{OFF}$	—
GPIO_25/TSEC1_CRS/USBDR_TXDRXD1	H1	I/O	$LVDD1_{OFF}$	—
TSEC1_GTX_CLK/USBDR_TXDRXD2	K5	I/O	$LVDD1_{OFF}$	3
TSEC1_RX_CLK/USBDR_TXDRXD3	J4	I/O	$LVDD1_{OFF}$	—
TSCE1_RX_DV/USBDR_TXDRXD4	J2	I/O	$LVDD1_{OFF}$	—
TSEC1_RXD[3]/USBDR_TXDRXD5	G1	I/O	$LVDD1_{OFF}$	—
TSEC1_RXD[2]/USBDR_TXDRXD6	H3	I/O	$LVDD1_{OFF}$	—
TSEC1_RXD[1]/USBDR_TXDRXD7/TSEC_TMR_CLK	J5	I/O	$LVDD1_{OFF}$	—
TSEC1_RXD[0]/USBDR_NXT/TSEC_TMR_TRIG1	H2	I	$LVDD1_{OFF}$	—
TSEC1_RX_ER/USBDR_DIR/TSEC_TMR_TRIG2	H5	I	$LVDD1_{OFF}$	—
TSEC1_TX_CLK/USBDR_CLK	G2	I	$LVDD1_{OFF}$	—
GPIO_28/TSEC1_TXD[3]/TSEC_TMR_GCLK	F3	I/O	$LVDD1_{OFF}$	—
GPIO_29/TSEC1_TXD[2]/TSEC_TMR_PP1	F2	I/O	$LVDD1_{OFF}$	—
GPIO_30/TSEC1_TXD[1]/TSEC_TMR_PP2	F1	I/O	$LVDD1_{OFF}$	—
TSEC1_TXD[0]/USBDR_STP/ TSEC_TMR_PP3	G4	O	$LVDD1_{OFF}$	12
GPIO_31/TSEC1_TX_EN/TSEC_TMR_ALARM1	F4	I/O	$LVDD1_{OFF}$	—
TSEC1_TX_ER/TSEC_TMR_ALARM2	G5	O	$LVDD1_{OFF}$	—
TSEC_GTX_CLK125	D1	I	$NVDD1_{ON}$	—
TSEC_MDC/LB_POR_CFG_BOOT_ECC	E3	I/O	$NVDD1_{ON}$	9
TSEC_MDIO	E2	I/O	$NVDD1_{ON}$	

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
Power and Ground Supplies				
GVDD	Y11, Y12, Y14, Y15, Y17, AC8, AC11, AC14, AC17, AD6, AD9, AD17, AE8, AE13, AE19, AF10, AF15, AF21, AG2, AG3, AG8, AG13, AG19, AH2	I	—	—
LVDD1_OFF	H6, J3, L6, L9, M9	I	—	—
LVDD2_ON	C11, D9, E10, F11, J12	I	—	—
NVDD1_OFF	U9, V9, W10, Y4, Y6, AA3, AB4	I	—	—
NVDD1_ON	B1, B2, C1, D5, E7, F5, F9, J11, K10	I	—	—
NVDD2_OFF	B22, B27, C19, E16, F15, F18, F21, F25, H25, J17, J18, J23, L20, M20	I	—	—
NVDD2_ON	L26, N19	I	—	—
NVDD3_OFF	U20, V20, V23, V26, W19, Y18, Y26, AA23, AA25, AC20, AC25, AD23, AE25, AG25, AG27	I	—	—
NVDD4_OFF	K4, L2, M6, N10	I	—	—
VDD	J15, K15, K16, K17, K18, K19, L10, L19, M10, T10, U10, U19, V10, V19, W11, W12, W13, W14, W15, W16, W17, W18	I	—	—
VDD1ANA	P23, R23, T19	I	—	—
VDD1IO	M26, N26, P28, R28	I	—	—
VDDC	J14, K11, K12, K13, K14, M19	I	—	—
VSS	A3, A27, B3, B12, B24, B28, C6, C8, C13, C17, C21, C23, C26, D2, D7, D15, D18, D20, D22, E4, E6, E11, E24, E26, F8, F12, F14, F17, F20, G3, G26, H4, H23, J6, J26, K25, L4, L11, L12, L13, L14, L15, L16, L17, L18, L23, L28, M3, M11, M12, M13, M14, M15, M16, M17, M18, N5, N11, N12, N13, N14, N15, N16, N17, N18, P6, P11, P12, P13, P14, P15, P16, P17, P18, R6, R11, R12, R13, R14, R15, R16, R17, R18, T11, T12, T13, T14, T15, T16, T17, T18, U5, U6, U11, U12, U13, U14, U15, U16, U17, U18, V6, V11, V12, V13, V14, V15, V16, V17, V18, W5, W25, W27, Y2, Y23, AA6, AA27, AB2, AB26, AC5, AC9, AC12, AC18, AC21, AD3, AD14, AD16, AD20, AD26, AE2, AE7, AE11, AE16, AE22, AE24, AF2, AF9, AF12, AF18, AF20, AF23, AF27, AG1, AG5, AG11, AG16, AG22, AG28, AH27	I	—	—
VSS1ANA	P24, R19, R20, R24	I	—	—

Table 73. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110–1111	Reserved

As described in Section 24, "Clocking," The LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ configuration input signal select the ratio between the primary clock input (SYS_CLK_IN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 74 and Table 75 shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN/PCI_SYNC_IN ratios.

Table 74. CSB Frequency Options for Host Mode

$\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ at Reset[1]	SPMF	csb_clk : Input Clock Ratio [2]	Input Clock Frequency (MHz)[2]		
			24	33.33	66.67
High/Low [3]	0010	2:1			133
High/Low	0011	3:1		100	—
High/Low	0100	4:1	96	133	—
High/Low	0101	5:1	120	—	—

1 $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ select the ratio between SYS_CLK_IN and PCI_SYNC_OUT.
2 SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.
3 In the Host mode it does not matter if the value is High or Low.

Table 75. CSB Frequency Options for Agent Mode

$\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio [2]	Input Clock frequency (MHz)[2]		
			25	33.33	66.67
High	0010	2: 1			133
High	0011	3: 1		100	—
High	0100	4: 1		133	—
High	0101	5: 1	120	—	—

1 $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ doubles csb_clk if set low.
2 SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

24.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 76 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 76 should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider
VCO divider has to be set properly so that the core VCO frequency is in the range of 400–800 MHz.

Table 76. e300 Core PLL Configuration

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider[1]
0–1	2–5	6		
nn	0000	0	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
11	nnnn	n	N/A	N/A
00	0001	0	1:1	2
01	0001	0	1:1	4
00	0001	1	1.5:1	2
01	0001	1	1.5:1	4
00	0010	0	2:1	2
01	0010	0	2:1	4
00	0010	1	2.5:1	2
01	0010	1	2.5:1	4
00	0011	0	3:1	2
01	0011	0	3:1	4

1 Core VCO frequency = core frequency × VCO divider.

24.3 Suggested PLL Configurations

To simplify the PLL configurations, the MPC8315E might be separated into two clock domains. The first domain contain the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. Table 77 shows suggested PLL configurations for 33, 25, and 66 MHz input clocks.

Table 77. Suggested PLL Configurations

Conf. No.	SPMF	Core\PLL	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)
1	0100	0000100	33.33	133.33	266.66
3	0010	0000100	66.67	133.33	266.66
4	0100	0000101	33.33	133.33	333.33
5	0101	0000101	25	125	312.5

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum VDD, nominal NVDD, 105°C.

Table 80. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI Signals (not including PCI Output Clocks)	PCI Output Clocks (including PCI_SYNC_OUT)	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
R_P	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
Differential	NA	NA	NA	NA	Z_{DIFF}	Ω

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

26.6 Configuration Pin Multiplexing

The MPC8315E provides the user with power-on configuration options that can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{PORESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

26.7 Pull-Up Resistor Requirements

The MPC8315E requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C pins and EPIC interrupt pins.

For more information on required pull up resistors and the connections required for JTAG interface, see AN3438, MPC8315 Design Checklist

27 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 27.1, “Part Numbers Fully Addressed by this Document.”

27.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the MPC8315E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme