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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8315vrafda

2.12 Power Management Controller (PMC)

The MPC8315E supports a range of power management states that significantly lower power consumption under the control of the power management controller. The PMC includes the following features:

- Provides power management when the device is used in both PCI host and agent modes
- PCI Power Management 1.2 D0, D1, D2, D3hot, and D3cold states
- PME generation in PCI agent mode, PME detection in PCI host mode
- Wake-up from Ethernet (magic packet), USB, GPIO, and PCI (PME input as host) while in the D1, D2 and D3hot states
- A new low-power standby power management state called D3warm
  - The PMC, one Ethernet port, and the GTM block remain powered via a split power supply controlled through an external power switch
  - Wake-up events include Ethernet (magic packet), GTM, GPIO, or IRQ inputs and cause the device to transition back to normal operation
  - PCI agent mode is not be supported in D3warm state
- PCI Express-based PME events are not supported

2.13 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the MPC8315E to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

2.14 DMA Controller, I^2C, DUART, Enhanced Local Bus Controller (eLBC), and Timers

The integrated four-channel DMA controller includes the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters)
- Misaligned transfer capability for source/destination address
- Supports external DREQ, DACK and DONE signals

There is one I^2C controller. This synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The eLBC port allows connections with a wide variety of external DSPs and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GVDD + 0.3)	V	2, 4
	DDR DRAM reference	MVREF	–0.3 to (GVDD + 0.3)	V	2, 4
	eTSEC signals	LV_{IN}	–0.3 to (LVDD + 0.3)	V	3, 4
	Local bus, DUART, SYS_CLK_IN, system control and power management, I^2C, and JTAG signals	NV_{IN}	–0.3 to (NVDD + 0.3)	V	3, 4
	PCI	NV_{IN}	–0.3 to (NVDD + 0.3)	V	5
	SATA_CLKIN	NV_{IN}	–0.3 to (NVDD + 0.3)	V	3, 4
Storage temperature range		T_{STG}	–55 to150	°C	—

Note:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** (N,L)V_{IN} must not exceed (N,L)VDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. (M,N,L)V_{IN} and MVREF may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
5. NV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 2.
6. The max value of supply voltage should be selected based on the RGMII mode.
7. NVDD means NVDD1_OFF, NVDD1_ON, NVDD2_OFF, NVDD2_ON, NVDD3_OFF, NVDD4_OFF
8. LVDD means LVDD1_OFF and LVDD2_ON

3.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for theMPC8315E. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value[1]	Unit	Status in D3 Warm mode	Note
SerDes internal digital power	XCOREVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes internal digital power	XCOREVSS	0.0	V	—	—
SerDes I/O digital power	XPADVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes I/O digital power	XPADVSS	0.0	V	—	—
SerDes analog power for PLL	SDAVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes analog power for PLL	SDAVSS	0.0	V	—	—
Dedicated 3.3 V analog power for USB PLL	USB_PLL_PWR3	3.3 ± 165mv	V	Switched Off	—
Dedicated 1.0 Vanalog power for USB PLL	USB_PLL_PWR1	1.0 ± 50 mv	V	Switched Off	—
Dedicated analog ground for USB PLL	USB_PLL_GND	0.0	V	—	—
Dedicated USB power for USB bias circuit	USB_VDDA_BIAS	3.3 ± 300 mv	V	Switched Off	—

Table 5. MPC8315E Power Dissipation (continued)

Interface	Frequency	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	NV_{DD} (3.3 V)	LVDD1_OFF/ LVDD2_ON (3.3V)	LVDD2 _ON (3.3V)	VDD33PLL, VDD33ANA (3.3V)	SATA_VDD, VDD1IO, VDD1ANA (1.0V)	XCOREVDD, XPADVDD, SDAVDD (1.0V)	Unit
DDR 2 Rs = 22Ω Rt = 75Ω	266MHz, 32 bits	0.246	—	—	—	—	—	—	—	W
	200MHz, 32bits	0.225	—	—	—	—	—	—	—	W
PCI I/O load = 50pF	33 MHz	—	—	0.120	—	—	—	—	—	W
	66 MHz	—	—	0.249	—	—	—	—	—	W
Local bus I/O load = 20pF	66 MHz	—	—	—	—	0.056	—	—	—	W
	50 MHz	—	—	—	—	0.040	—	—	—	W
eTSEC I/O load = 20pF Multiple by number of interface used	MII, 25MHz	—	—	—	0.008	—	—	—	—	W
	RGMII, 125MHz (3.3V)	—	—	—	0.078	—	—	—	—	W
	RGMII, 125MHz (2.5V)	—	—	—	0.044	—	—	—	—	W
USBDR Controller (ULPI mode) load =20pF	60 MHz	—	—	—	0.078	—	—	—	—	W
USBDR+ Internal PHY (UTMI mode)	480 MHz	—	—	—	0.274	—	—	—	—	W
PCI Express two x1lane	2.5 GHz	—	—	—	—	—	—	—	0.190	W
SATA two ports	3.0 GHz	—	—	—	—	—	0.021	0.206	—	W
Other I/O	—	—	—	0.015	—	—	—	—	—	W

5 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8315E.

6 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8315E.

6.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins of the MPC8315E.

Table 8. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le$ NVDD	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

6.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications of the MPC8315E.

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to SYS_CLK_IN when the device is in PCI host mode	32	—	$t_{SYS\_CLK\_IN}$	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the device is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3] and $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	$t_{SYS\_CLK\_IN}$	2, 4
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3] and $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to turn on POR config signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Table 11. DDR2 SDRAM DC Electrical Characteristics for GVDD(typ) = 1.8 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Note

Note:
1. GVDD is expected to be within 50 mV of the DRAM GVDD at all times.
2. MVREF is expected to be equal to 0.5 × GVDD, and to track GVDD DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GVDD.

This table provides the DDR2 capacitance when GVDD(typ) = 1.8 V.

Table 12. DDR2 SDRAM Capacitance for GVDD(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GVDD = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8315E when GVDD(typ) = 2.5 V.

Table 13. DDR SDRAM DC Electrical Characteristics for GVDD(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GVDD	2.3	2.7	V	1
I/O reference voltage	MVREF	0.49 × GVDD	0.51 × GVDD	V	2
I/O termination voltage	V_{TT}	MVREF – 0.04	MVREF + 0.04	V	3
Input high voltage	V_{IH}	MVREF + 0.15	GVDD + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF – 0.15	V	—
Output leakage current	I_{OZ}	–9.9	–9.9	μA	4
Output high current (V_{OUT} = 1.95 V, GVDD = 2.3V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Note:
1. GVDD is expected to be within 50 mV of the DRAM GVDD at all times.
2. MVREF is expected to be equal to 0.5 × GVDD, and to track GVDD DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GVDD.

This table provides the DDR capacitance when GVDD(typ) = 2.5 V.

Table 14. DDR SDRAM Capacitance for GVDD(typ) = 2.5 V Interface

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ,DQS	C_{IO}	6	8	pF	1

This figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

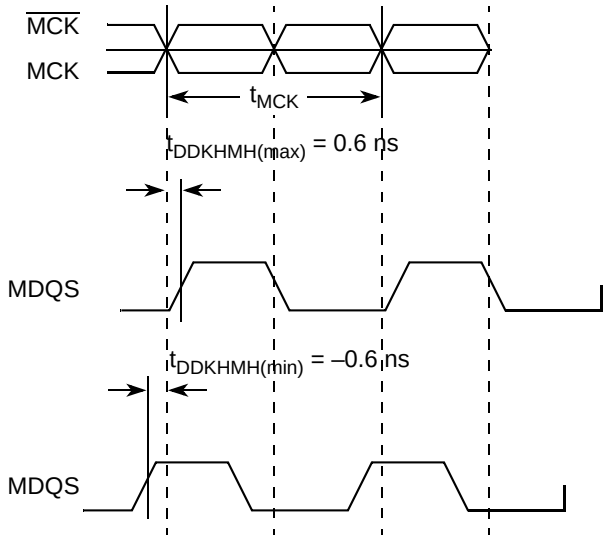


Figure 7. Timing Diagram for t_{DDKHMH}

This figure shows the DDR and DDR2 SDRAM output timing diagram.

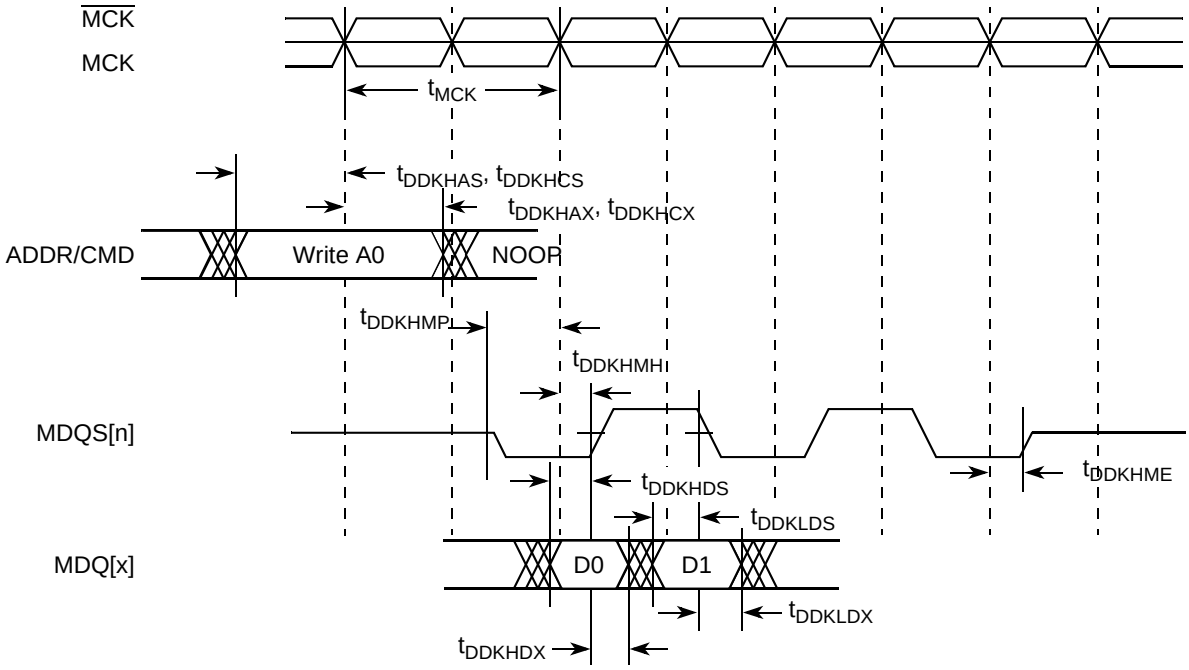


Figure 8. DDR and DDR2 SDRAM Output Timing Diagram

Table 24. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics (continued)

Parameters	Symbol	Conditions	Min	Max	Unit

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII, RMII, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for MII, RMII, RGMII, and RTBI are presented in this section.

9.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

9.2.1.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 25. MII Transmit AC Timing Specifications

At recommended operating conditions with LVDD of 3.3 V ± 300 mv.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{MTXF}	1.0	—	4.0	ns

Note:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII transmit AC timing diagram.

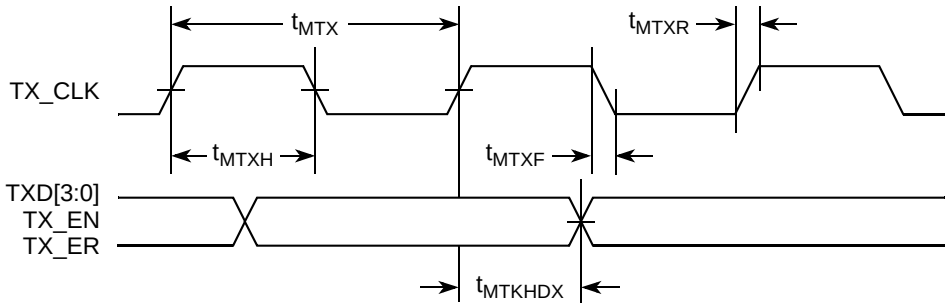


Figure 10. MII Transmit AC Timing Diagram

9.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

9.2.2.1 RMII Transmit AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications. This table provides the RMII transmit AC timing specifications.

Table 27. RMII Transmit AC Timing Specifications

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	10	ns
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

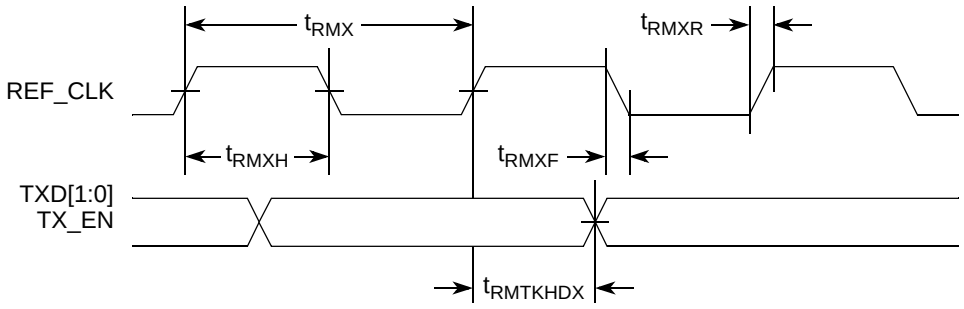


Figure 13. RMII Transmit AC Timing Diagram

9.2.2.2 RMII Receive AC Timing Specifications

This table provides the RMII receive AC timing specifications.

Table 28. RMII Receive AC Timing Specifications

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%

Table 35. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	XCOREVDD	0.95	1.0	1.05	V	—
Output high voltage	VOH	—	—	$XCOREVDD_{-Typ}/2 + \lvert V_{OD}\rvert_{-max}/2$	mV	1
Output low voltage	VOL	$XCOREVDD_{-Typ}/2 - \lvert V_{OD}\rvert_{-max}/2$	—	—	mV	1
Output ringing	V_{RING}	—	—	10	%	—
Output differential voltage[2, 3, 5]	$\lvert V_{OD}\rvert$	323	500	725	mV	Equalization setting: 1.0x
		296	459	665		Equalization setting: 1.09x
		269	417	604		Equalization setting: 1.2x
		243	376	545		Equalization setting: 1.33x
		215	333	483		Equalization setting: 1.5x
		189	292	424		Equalization setting: 1.71x
		162	250	362		Equalization setting: 2.0x
Output offset voltage	V_{OS}	425	500	575	mV	1, 4
Output impedance (single-ended)	R_O	40	—	60	Ω	—
Mismatch in a pair	ΔR_O	—	—	10	%	—
Change in V_{OD} between “0” and “1”	$\Delta \lvert V_{OD}\rvert$	—	—	25	mV	—
Change in V_{OS} between “0” and “1”	ΔV_{OS}	—	—	25	mV	—
Output current on short to GND	I_{SA}, I_{SB}	—	—	40	mA	—

Note:

1. This will not align to DC-coupled SGMII. $XCOREVDD_{-Typ}$=1.0V.
2. $\lvert V_{OD}\rvert = \lvert V_{TXn} - V_{\overline{TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX-DIFFp-p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the table assumes the following transmit equalization setting in the TXEQA (for SerDes lane A) or TXEQE (for SerDes lane E) bit field of MPC8315E’s SerDes Control Register 0:
   - The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. V_{OS} is also referred to as output common mode voltage.
5. The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $XCOREVDD_{-Typ}$=1.0V, no common mode offset variation (V_{OS} = 500 mV), SerDes transmitter is terminated with 100-Ω differential load between TX[n] and $\overline{TX}$[n].

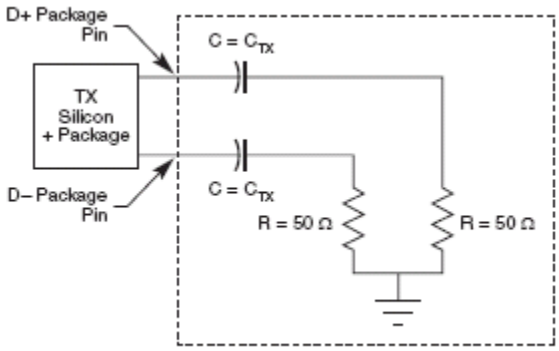


Figure 21. SGMII AC Test/Measurement Load

10 USB

10.1 USB Dual-Role Controllers

This section provides the AC and DC electrical specifications for the USB-ULPI interface.

10.1.1 USB DC Electrical Characteristics

This table lists the DC electrical characteristics for the USB interface.

Table 39. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	LVDD + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	LVDD – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

10.1.2 USB AC Electrical Specifications

This table lists the general timing parameters of the USB-ULPI interface.

Table 40. USB General Timing Parameters

Parameter	Symbol [1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	1, 2
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	1, 4
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	1, 4

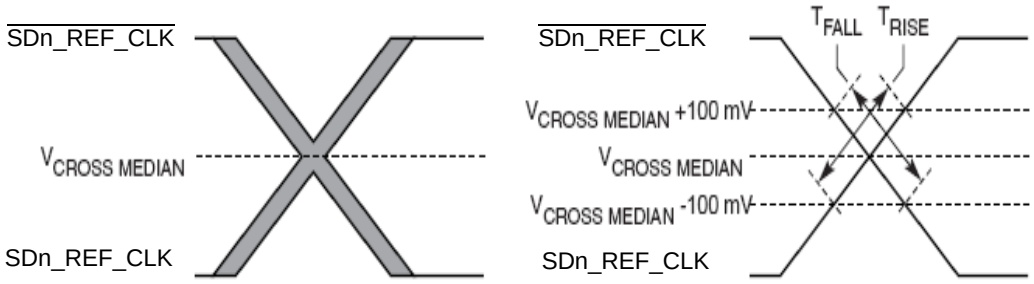


Figure 48. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- Section 9.5.2, “AC Requirements for SGMII SD_REF_CLK and SD_REF_CLK”
- Section 16.2, “AC Requirements for PCI Express SerDes Clocks”

15.2.4.1 Spread Spectrum Clock

SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

15.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane’s transmitter and receiver.

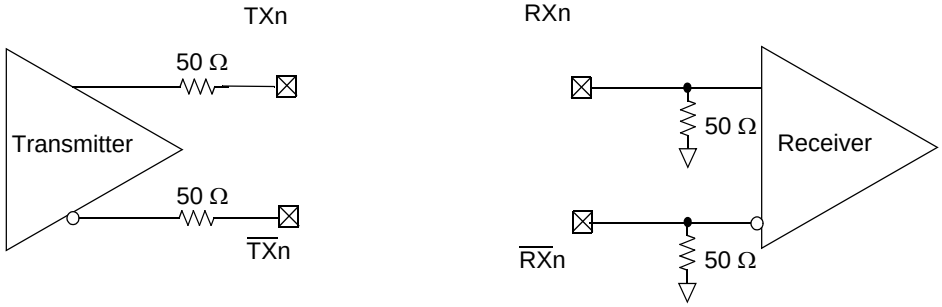


Figure 49. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express or SGMII) in this document based on the application usage:

- Section 9.5, “SGMII Interface Electrical Characteristics”
- Section 16, “PCI Express”

Note that external AC Coupling capacitor is required for the above two serial transmission protocols with the capacitor value defined in specification of each protocol section.

Table 55. Differential Receiver (RX) Input Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Unit	Note
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power.	200 k	—	—	Ω	6
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	V_{PEEIDT} = 2*|V_{RX-D+} -V_{RX-D-}| Measured at the package pins of the Receiver	65	—	175	mV	—
Unexpected Electrical Idle Enter Detect Threshold Integration Time	$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	An unexpected Electrical Idle (Vrx-diffp-p < Vrx-idle-det-diffp-p) must be recognized no longer than Trx-idle-det-diff-entertime to signal an unexpected idle condition.	—	—	10	ms	—
Total Skew	$L_{RX-SKEW}$	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (e.g. COM and one to five SKP Symbols) at the RX as well as any delay differences arising from the interconnect itself.	—	—	20	ns	—

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 52 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 51). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 52). Note that the series capacitors, C_{TX}, is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
6. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

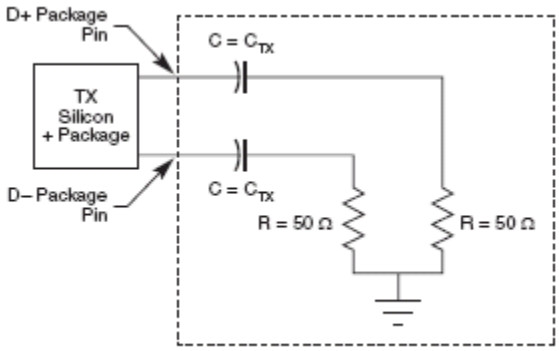


Figure 52. Compliance Test/Measurement Load

17 Serial ATA (SATA)

The serial ATA (SATA) of the MPC8315E is designed to comply with Serial ATA 2.5 Specification. Note that the external cabled applications or long backplane applications (Gen1x & Gen2x) are not supported.

17.1 Requirements for SATA REF_CLK

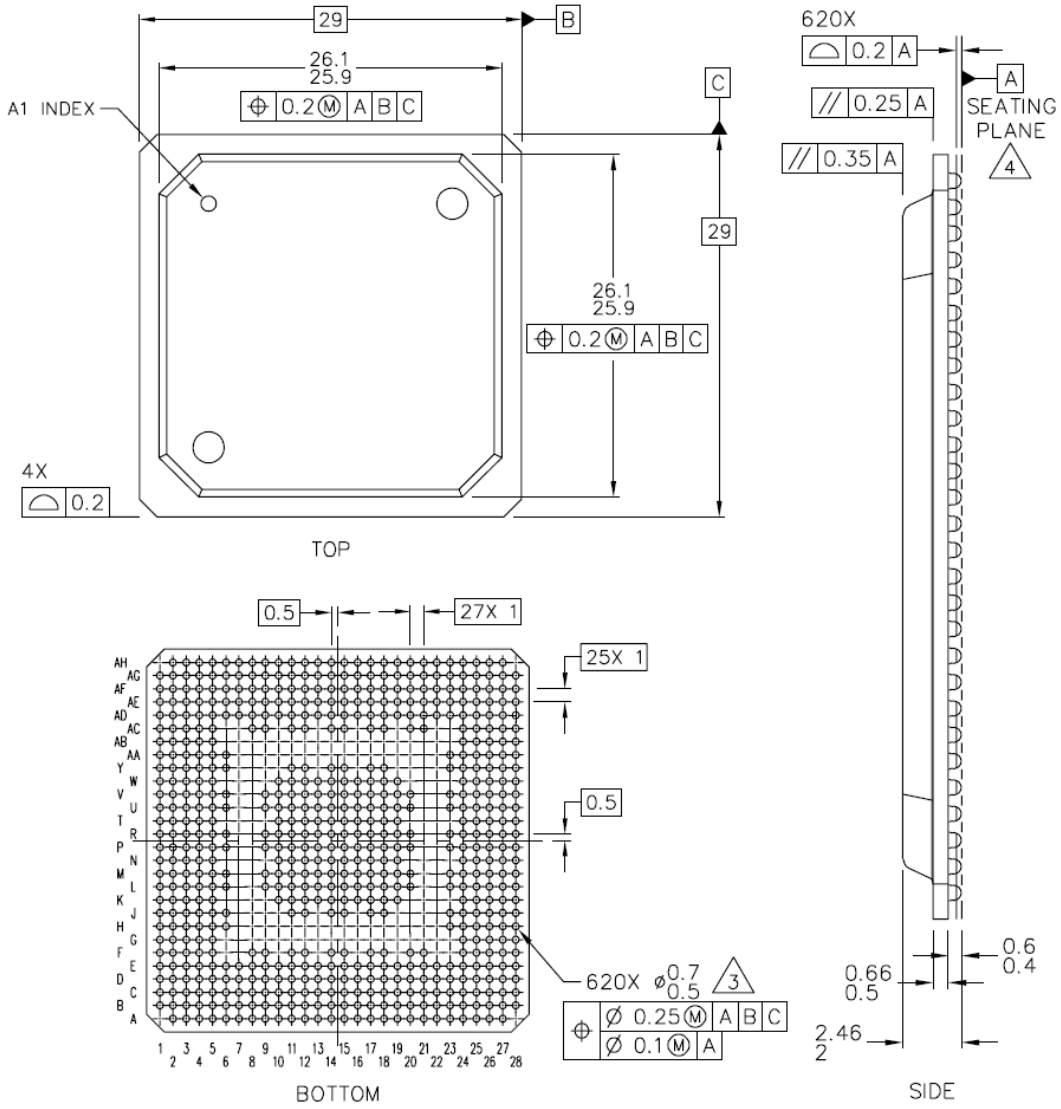
The reference clock for MPC8315E is a single ended input clock required for the SATA Interface operation. The AC requirements for the SATA reference clock are listed in the this table.

Table 56. Reference Clock Input Requirements

Parameter	Symbol	Conditions	Min	Typical	Max	Unit	Note
Frequency range	t_{CLK_REF}	—	50	75	150	MHz	1
Clock frequency tolerance	t_{CLK_TOL}	—	-350	0	+350	ppm	—
Input High Voltage	V_{CLK_INHI}	—	2.0	—	—	V	—
Input Low Voltage	V_{CLK_INLo}	—	—	—	0.7	V	—
Reference clock rise and fall time	t_{CLK_RISE}/ t_{CLK_FALL}	20% to 80% of nominal amplitude	—	—	2	ns	—
Reference clock duty cycle	t_{CLK_DUTY}	Measured at 1.6V	40	50	60	%	—

23.2 Mechanical Dimensions of the TEPBGA II

This figure shows the mechanical dimensions and bottom surface nomenclature of the 620-pin TEPBGA II package.



Notes:
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 61. Mechanical Dimensions and Bottom Surface Nomenclature of the TEPBGA II

23.3 Pinout Listings

This table provides the pin-out listing for the TEPBGA II package.

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
JTAG				
TCK	E5	I	$NVDD1_{ON}$	—
TDI	B4	I	$NVDD1_{ON}$	4
TDO	C4	O	$NVDD1_{ON}$	3
TMS	C3	I	$NVDD1_{ON}$	4
$\overline{\text{TRST}}$	C2	I	$NVDD1_{ON}$	4
TDM				
GPIO_18/TDM_RCK	AB1	I/O	$NVDD1_{OFF}$	—
GPIO_20/TDM_RD	AC1	I/O	$NVDD1_{OFF}$	—
GPIO_19/TDM_RFS	AB3	I/O	$NVDD1_{OFF}$	—
GPIO_21/TDM_TCK	AB5	I/O	$NVDD1_{OFF}$	—
GPIO_23/TDM_TD	AC3	I/O	$NVDD1_{OFF}$	—
GPIO_22/TDM_TFS	AC2	I/O	$NVDD1_{OFF}$	—
SATA				
PINRXMINUSA	N28	I	VDD1IO	—
PINRXMINUSB	U28	I	VDD1IO	—
PINRXPLUSA	M28	I	VDD1IO	—
PINRXPLUSB	T28	I	VDD1IO	—
PINTXMINUSA	M25	O	VDD1IO	—
PINTXMINUSB	P26	O	VDD1IO	—
PINTXPLUSA	N25	O	VDD1IO	—
PINTXPLUSB	R26	O	VDD1IO	—
SATA_ANAVIZ	U26	O	—	—
SATA_CLK_IN	V27	I	NVDD3_OFF	—
SATA_VDD	N27	I	—	—
SATA_VDD	U23	I	—	—
SATA_VSS	M27	I	—	—
SATA_VSS	V28	I	—	—
VSSRESREF	T26	I	—	—
RESREF	T25	I	—	10
VDD33ANA	U27	I	—	—
VDD33PLL	T27	I	—	—
TEST				
TEST_MODE	D6	I	$NVDD1_{ON}$	6
DEBUG				

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_AD[9]	F28	I/O	$NVDD2_{OFF}$	—
PCI_AD[10]	G25	I/O	$NVDD2_{OFF}$	—
PCI_AD[11]	F27	I/O	$NVDD2_{OFF}$	—
PCI_AD[12]	E27	I/O	$NVDD2_{OFF}$	—
PCI_AD[13]	E28	I/O	$NVDD2_{OFF}$	—
PCI_AD[14]	D28	I/O	$NVDD2_{OFF}$	—
PCI_AD[15]	D27	I/O	$NVDD2_{OFF}$	—
PCI_AD[16]	B25	I/O	$NVDD2_{OFF}$	—
PCI_AD[17]	D24	I/O	$NVDD2_{OFF}$	—
PCI_AD[18]	B26	I/O	$NVDD2_{OFF}$	—
PCI_AD[19]	C24	I/O	$NVDD2_{OFF}$	—
PCI_AD[20]	A26	I/O	$NVDD2_{OFF}$	—
PCI_AD[21]	E20	I/O	$NVDD2_{OFF}$	—
PCI_AD[22]	A23	I/O	$NVDD2_{OFF}$	—
PCI_AD[23]	C22	I/O	$NVDD2_{OFF}$	—
PCI_AD[24]	E19	I/O	$NVDD2_{OFF}$	—
PCI_AD[25]	A22	I/O	$NVDD2_{OFF}$	—
PCI_AD[26]	C20	I/O	$NVDD2_{OFF}$	—
PCI_AD[27]	B21	I/O	$NVDD2_{OFF}$	—
PCI_AD[28]	D19	I/O	$NVDD2_{OFF}$	—
PCI_AD[29]	A19	I/O	$NVDD2_{OFF}$	—
PCI_AD[30]	A21	I/O	$NVDD2_{OFF}$	—
PCI_AD[31]	B19	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[0]	H24	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[1]	C27	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[2]	A25	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[3]	E21	I/O	$NVDD2_{OFF}$	—
PCI_PAR	G24	I/O	$NVDD2_{OFF}$	—
$\overline{PCI\_FRAME}$	C28	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_TRDY}$	A24	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_IRDY}$	D25	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_STOP}$	D23	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_DEVSEL}$	E22	I/O	$NVDD2_{OFF}$	5
PCI_IDSEL	D26	I	$NVDD2_{OFF}$	—
$\overline{PCI\_SERR}$	C25	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_PERR}$	D21	I/O	$NVDD2_{OFF}$	5

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
ETSEC2				
GPIO_26/TSEC2_COL	A8	I/O	$LVDD2_{ON}$	—
GPIO_27/TSEC2_CRS	E9	I/O	$LVDD2_{ON}$	—
TSEC2_GTX_CLK	B10	O	$LVDD2_{ON}$	—
TSEC2_RX_CLK	B8	I	$LVDD2_{ON}$	—
TSCE2_RX_DV	C9	I	$LVDD2_{ON}$	—
TSEC2_RXD[3]	C10	I	$LVDD2_{ON}$	—
TSEC2_RXD[2]	D10	I	$LVDD2_{ON}$	—
TSEC2_RXD[1]	A9	I	$LVDD2_{ON}$	—
TSEC2_RXD[0]	B9	I	$LVDD2_{ON}$	—
TSEC2_RX_ER	A10	I	$LVDD2_{ON}$	—
TSEC2_TX_CLK	D8	I	$LVDD2_{ON}$	—
TSEC2_TXD[3]/CFG_RESET_SOURCE[0]	D11	I/O	$LVDD2_{ON}$	—
TSEC2_TXD[2]/CFG_RESET_SOURCE[1]	C7	I/O	$LVDD2_{ON}$	—
TSEC2_TXD[1]/CFG_RESET_SOURCE[2]	E8	I/O	$LVDD2_{ON}$	—
TSEC2_TXD[0]/CFG_RESET_SOURCE[3]	B7	I/O	$LVDD2_{ON}$	—
TSEC2_TX_EN	D12	O	$LVDD2_{ON}$	—
TSEC2_TX_ER	B11	O	$LVDD2_{ON}$	—
SGMII / PCI Express PHY				
TXA	P4	O	XPADVDD	—
$\overline{\text{TXA}}$	N4	O	XPADVDD	—
RXA	R1	I	XCOREVDD	—
$\overline{\text{RXA}}$	P1	I	XCOREVDD	—
TXB	U4	O	XPADVDD	—
$\overline{\text{TXB}}$	V4	O	XPADVDD	—
RXB	U1	I	XCOREVDD	—
$\overline{\text{RXB}}$	V1	I	XCOREVDD	—
SD_IMP_CAL_RX	N3	I	XCOREVDD	—
$\overline{\text{SD\_REF\_CLK}}$	R4	I	XCOREVDD	—
SD_REF_CLK	R5	I	XCOREVDD	—
SD_PLL_TPD	T2	O	—	—
SD_IMP_CAL_TX	V5	I	XPADVDD	—
SDAVDD	T3	I	—	—
SD_PLL_TPA_ANA	T4	O	—	—
SDAVSS	T5	I	—	—
USB Phy				

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
Power and Ground Supplies				
GVDD	Y11, Y12, Y14, Y15, Y17, AC8, AC11, AC14, AC17, AD6, AD9, AD17, AE8, AE13, AE19, AF10, AF15, AF21, AG2, AG3, AG8, AG13, AG19, AH2	I	—	—
LVDD1_OFF	H6, J3, L6, L9, M9	I	—	—
LVDD2_ON	C11, D9, E10, F11, J12	I	—	—
NVDD1_OFF	U9, V9, W10, Y4, Y6, AA3, AB4	I	—	—
NVDD1_ON	B1, B2, C1, D5, E7, F5, F9, J11, K10	I	—	—
NVDD2_OFF	B22, B27, C19, E16, F15, F18, F21, F25, H25, J17, J18, J23, L20, M20	I	—	—
NVDD2_ON	L26, N19	I	—	—
NVDD3_OFF	U20, V20, V23, V26, W19, Y18, Y26, AA23, AA25, AC20, AC25, AD23, AE25, AG25, AG27	I	—	—
NVDD4_OFF	K4, L2, M6, N10	I	—	—
VDD	J15, K15, K16, K17, K18, K19, L10, L19, M10, T10, U10, U19, V10, V19, W11, W12, W13, W14, W15, W16, W17, W18	I	—	—
VDD1ANA	P23, R23, T19	I	—	—
VDD1IO	M26, N26, P28, R28	I	—	—
VDDC	J14, K11, K12, K13, K14, M19	I	—	—
VSS	A3, A27, B3, B12, B24, B28, C6, C8, C13, C17, C21, C23, C26, D2, D7, D15, D18, D20, D22, E4, E6, E11, E24, E26, F8, F12, F14, F17, F20, G3, G26, H4, H23, J6, J26, K25, L4, L11, L12, L13, L14, L15, L16, L17, L18, L23, L28, M3, M11, M12, M13, M14, M15, M16, M17, M18, N5, N11, N12, N13, N14, N15, N16, N17, N18, P6, P11, P12, P13, P14, P15, P16, P17, P18, R6, R11, R12, R13, R14, R15, R16, R17, R18, T11, T12, T13, T14, T15, T16, T17, T18, U5, U6, U11, U12, U13, U14, U15, U16, U17, U18, V6, V11, V12, V13, V14, V15, V16, V17, V18, W5, W25, W27, Y2, Y23, AA6, AA27, AB2, AB26, AC5, AC9, AC12, AC18, AC21, AD3, AD14, AD16, AD20, AD26, AE2, AE7, AE11, AE16, AE22, AE24, AF2, AF9, AF12, AF18, AF20, AF23, AF27, AG1, AG5, AG11, AG16, AG22, AG28, AH27	I	—	—
VSS1ANA	P24, R19, R20, R24	I	—	—

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
VSS1IO	M24, N24, P19, P20, P25, P27, R25, R27, T24	I	—	—
XCOREVDD	P2, P10, R2, T1	I	—	—
XCOREVSS	R3, R10, U2, V2	I	—	—
XPADVDD	P3, R9, U3	I	—	—
XPADVSS	P5, P9, V3	I	—	—

Note:

1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to NVDD.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to NVDD.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. This pin must always be tied to VSS.
7. Thermal sensitive resistor.
8. This pin should be connected to USB_VSSA_BIAS through 10K precision resistor.
9. The LB_POR_CFG_BOOT_ECC functionality for this pin is only available in MPC8315E revision 1.1 and later. The LB_POR_CFG_BOOT_ECC is sampled only during the $\overline{\text{PORESET}}$ negation. This pin with an internal pull down resistor enables the ECC by default. To disable the ECC an external strong pull up resistor or a tristate buffer is needed.
10. This pin should be connected to an external 2.7 K ±1% resistor connected to VSS. The resistor should be placed as close as possible to the input.
11. This pin has a weak internal pull-down.
12. This pin has a weak internal pull-up.

Table 73. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110–1111	Reserved

As described in Section 24, "Clocking," The LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ configuration input signal select the ratio between the primary clock input (SYS_CLK_IN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 74 and Table 75 shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN/PCI_SYNC_IN ratios.

Table 74. CSB Frequency Options for Host Mode

$\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ at Reset[1]	SPMF	csb_clk : Input Clock Ratio [2]	Input Clock Frequency (MHz)[2]		
			24	33.33	66.67
High/Low [3]	0010	2:1			133
High/Low	0011	3:1		100	—
High/Low	0100	4:1	96	133	—
High/Low	0101	5:1	120	—	—

1 $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ select the ratio between SYS_CLK_IN and PCI_SYNC_OUT.
2 SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.
3 In the Host mode it does not matter if the value is High or Low.

Table 75. CSB Frequency Options for Agent Mode

$\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio [2]	Input Clock frequency (MHz)[2]		
			25	33.33	66.67
High	0010	2: 1			133
High	0011	3: 1		100	—
High	0100	4: 1		133	—
High	0101	5: 1	120	—	—

1 $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ doubles csb_clk if set low.
2 SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.