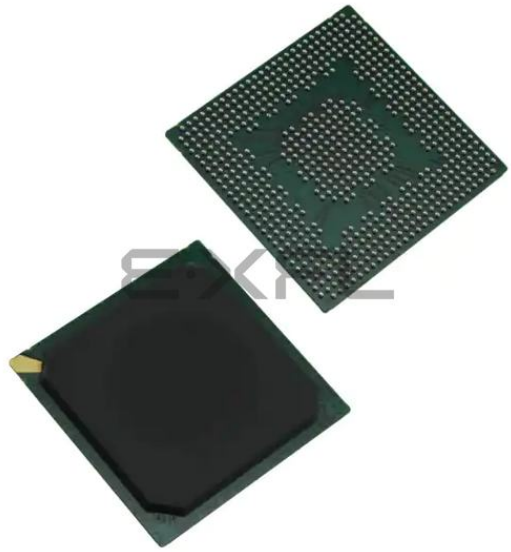

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8315vragda

  - Combines a True Random Number Generator (TRNG) and a NIST-approved Pseudo-Random Number Generator (PRNG) (as described in Annex C of FIPS140-2 and ANSI X9.62).
- Cyclical Redundancy Check Hardware Accelerator (CRCA)
  - Implements CRC32C as required for iSCSI header and payload checksums, CRC32 as required for IEEE 802 packets, as well as for programmable 32 bit CRC polynomials

2.4 DDR Memory Controller

The DDR1/DDR2 memory controller includes the following features:

- Single 16- or 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 266 MHz data rate
- Support for two physical banks (chip selects), each bank independently addressable
- 64-Mbit to 2-Gbit (for DDR1) and to 4-Gbit (for DDR2) devices with x8/x16 data ports (no direct x4 support)
- Support for one 16-bit device or two 8-bit devices on a 16-bit bus or two 16-bit devices on a 32-bit bus
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

2.5 PCI Controller

The PCI controller includes the following features:

- Designed to comply with *PCI Local Bus Specification Revision 2.3*
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

2.6 TDM Interface

The TDM interface includes the following features:

- Independent receive and transmit with dedicated data, clock and frame sync line
- Separate or shared RCK and TCK whose source can be either internal or external
- Glueless interface to E1/T1 frames and MVIP, SCAS, and H.110 buses
- Up to 128 time slots, where each slot can be programmed to be active or inactive
- 8- or 16-bit word widths
- The TDM Transmitter Sync Signal (TFS), Transmitter Clock Signal (TCK) and Receiver Clock

2.9 Dual Serial ATA (SATA) Controllers

The SATA controllers have the following features:

- Designed to comply with *Serial ATA Rev 2.5 Specification*
- ATAPI 6+
- Spread spectrum clocking on receive
- Asynchronous notification
- Hot plug including asynchronous signal recovery
- Link power management
- Native command queuing
- Staggered spin-up and port multiplier support
- SATA 1.5 and 3.0 Gbps operation
- Interrupt driven
- Power management support
- Error handling and diagnostic features
  - Far end/near end loopback
  - Failed CRC error reporting
  - Increased ALIGN insertion rates
  - Scrambling and CONT override

2.10 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The eTSECs include the following features:

- Two SGMII/RGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Std 802.3™, IEEE 802.3u™, IEEE 802.3x™, IEEE 802.3z™, IEEE 802.3au™, IEEE 802.3ab™, and IEEE Std 1588™
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status.

2.11 Integrated Programmable Interrupt Controller (IPIC)

The integrated programmable interrupt controller (IPIC) provides a flexible solution for general-purpose interrupt control. The IPIC programming model is compatible with the MPC8260 interrupt controller and supports external and internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GVDD + 0.3)	V	2, 4
	DDR DRAM reference	MVREF	–0.3 to (GVDD + 0.3)	V	2, 4
	eTSEC signals	LV_{IN}	–0.3 to (LVDD + 0.3)	V	3, 4
	Local bus, DUART, SYS_CLK_IN, system control and power management, I^2C, and JTAG signals	NV_{IN}	–0.3 to (NVDD + 0.3)	V	3, 4
	PCI	NV_{IN}	–0.3 to (NVDD + 0.3)	V	5
	SATA_CLKIN	NV_{IN}	–0.3 to (NVDD + 0.3)	V	3, 4
Storage temperature range		T_{STG}	–55 to150	°C	—

Note:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** (N,L)V_{IN} must not exceed (N,L)VDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. (M,N,L)V_{IN} and MVREF may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
5. NV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 2.
6. The max value of supply voltage should be selected based on the RGMII mode.
7. NVDD means NVDD1_OFF, NVDD1_ON, NVDD2_OFF, NVDD2_ON, NVDD3_OFF, NVDD4_OFF
8. LVDD means LVDD1_OFF and LVDD2_ON

3.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for theMPC8315E. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value[1]	Unit	Status in D3 Warm mode	Note
SerDes internal digital power	XCOREVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes internal digital power	XCOREVSS	0.0	V	—	—
SerDes I/O digital power	XPADVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes I/O digital power	XPADVSS	0.0	V	—	—
SerDes analog power for PLL	SDAVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes analog power for PLL	SDAVSS	0.0	V	—	—
Dedicated 3.3 V analog power for USB PLL	USB_PLL_PWR3	3.3 ± 165mv	V	Switched Off	—
Dedicated 1.0 Vanalog power for USB PLL	USB_PLL_PWR1	1.0 ± 50 mv	V	Switched Off	—
Dedicated analog ground for USB PLL	USB_PLL_GND	0.0	V	—	—
Dedicated USB power for USB bias circuit	USB_VDDA_BIAS	3.3 ± 300 mv	V	Switched Off	—

CAUTION

When the device is in D3 warm (standby) mode, all external voltage supplies applied to any I/O pins, with the exception of wake-up pins, must be turned off. Applying supplied external voltage to any I/O pins, except the wake up pins, while the device is in D3 warm standby mode may cause permanent damage to the device.

An example of the power-up sequence is shown in Figure 4 when implemented along with low power D3 warm mode.

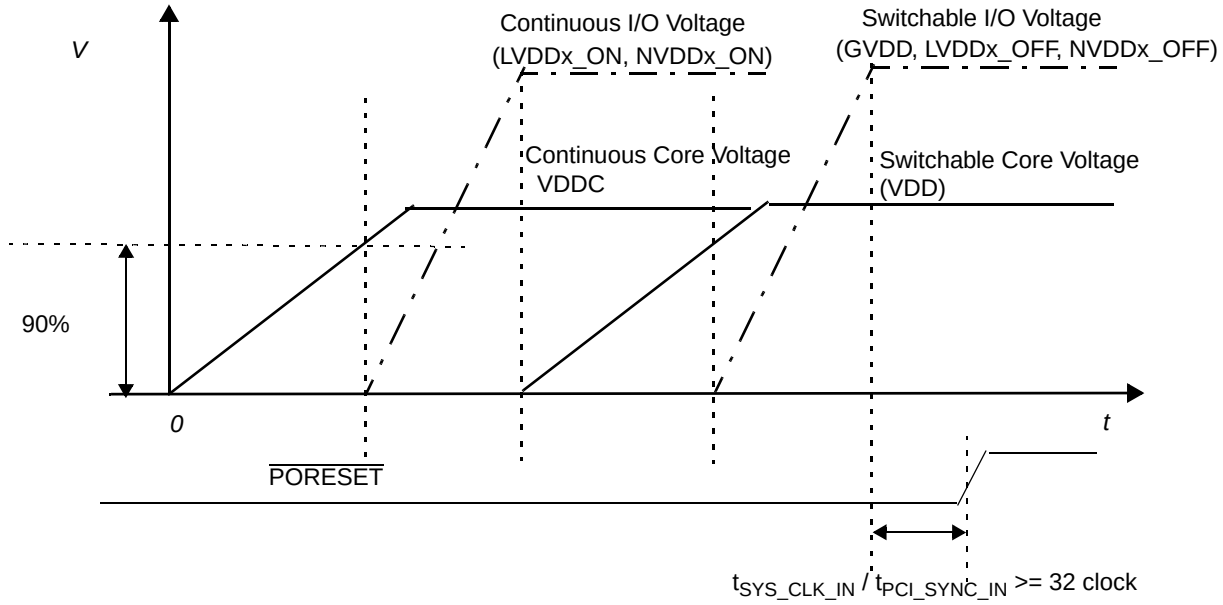

Figure 4. Power Up Sequencing Example with Low power D3 Warm Mode

The switchable and continuous supplies can be combined when the D3 warm mode is not used.

The SATA power supplies VDD33PLL and VDD33ANA should go high after NVDD3_OFF supply and go low before NVDD3_OFF supply. The NVDD3_OFF voltage levels should not drop below the VDD33PLL, VDD33ANA voltages at any time.

5.1 DC Electrical Characteristics

This table provides the clock input (SYS_CLK_IN/PCI_SYNC_IN) DC timing specifications for the MPC8315E.

Table 6. SYS_CLK_IN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	NVDD + 0.3	V
Input low voltage	—	V_{IL}	-0.3	0.4	V
SYS_CLK_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
SYS_XTAL_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±40	μA
PCI_SYNC_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
RTC_CLK input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
USB_CLK_IN input current	0 V ≤ V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
USB_XTAL_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±40	μA
SATA_CLK_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA

5.2 AC Electrical Characteristics

The primary clock source for the MPC8315E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (SYS_CLK_IN/PCI_CLK) AC timing specifications for the MPC8315E.

Table 7. SYS_CLK_IN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
SYS_CLK_IN/PCI_CLK frequency	$f_{SYS\_CLK\_IN}$	24	—	66.67	MHz	1, 6, 7
SYS_CLK_IN/PCI_CLK cycle time	$t_{SYS\_CLK\_IN}$	15	—	41.6	ns	6
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	0.6	—	4	ns	2, 6
PCI_CLK rise and fall time	t_{PCH}, t_{PCL}	0.6	0.8	1.2	ns	2
SYS_CLK_IN/PCI_CLK duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3, 6
SYS_CLK_IN/PCI_CLK jitter	—	—	—	±150	ps	4, 5, 6

Note:

1. **Caution:** The system, core, and security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN/PCI_CLK are specified at 20% to 80% of signal swing.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
6. The parameter names PCI_CLK and PCI_SYNC_IN are used interchangeably in this document.
7. Spread spectrum is allowed up to 1% down-spread at 33kHz.(max. rate).

Table 11. DDR2 SDRAM DC Electrical Characteristics for GVDD(typ) = 1.8 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Note

Note:
1. GVDD is expected to be within 50 mV of the DRAM GVDD at all times.
2. MVREF is expected to be equal to 0.5 × GVDD, and to track GVDD DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GVDD.

This table provides the DDR2 capacitance when GVDD(typ) = 1.8 V.

Table 12. DDR2 SDRAM Capacitance for GVDD(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GVDD = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8315E when GVDD(typ) = 2.5 V.

Table 13. DDR SDRAM DC Electrical Characteristics for GVDD(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GVDD	2.3	2.7	V	1
I/O reference voltage	MVREF	0.49 × GVDD	0.51 × GVDD	V	2
I/O termination voltage	V_{TT}	MVREF – 0.04	MVREF + 0.04	V	3
Input high voltage	V_{IH}	MVREF + 0.15	GVDD + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF – 0.15	V	—
Output leakage current	I_{OZ}	–9.9	–9.9	μA	4
Output high current (V_{OUT} = 1.95 V, GVDD = 2.3V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Note:
1. GVDD is expected to be within 50 mV of the DRAM GVDD at all times.
2. MVREF is expected to be equal to 0.5 × GVDD, and to track GVDD DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GVDD.

This table provides the DDR capacitance when GVDD(typ) = 2.5 V.

Table 14. DDR SDRAM Capacitance for GVDD(typ) = 2.5 V Interface

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ,DQS	C_{IO}	6	8	pF	1

7.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions

Parameter	Symbol [1]	Min	Max	Unit	Note
MCK[n] cycle time at MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	7.5	10	ns	2
ADDR/CMD output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHAS}	 2.9 3.5	 — —	ns	3
ADDR/CMD output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHAX}	 3.15 4.20	 — —	ns	3
$\overline{\text{MCS}}$[n] output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHCS}	 3.15 4.20	 — —	ns	3
$\overline{\text{MCS}}$[n] output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHCX}	 3.15 4.20	 — —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ//MDM output setup with respect to MDQS 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 900 1000	 — —	ps	5
MDQ//MDM output hold with respect to MDQS 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 1100 1200	 — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Table 28. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load.

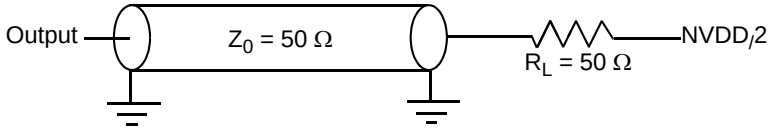

Figure 14. AC Test Load

This figure shows the RMII receive AC timing diagram.

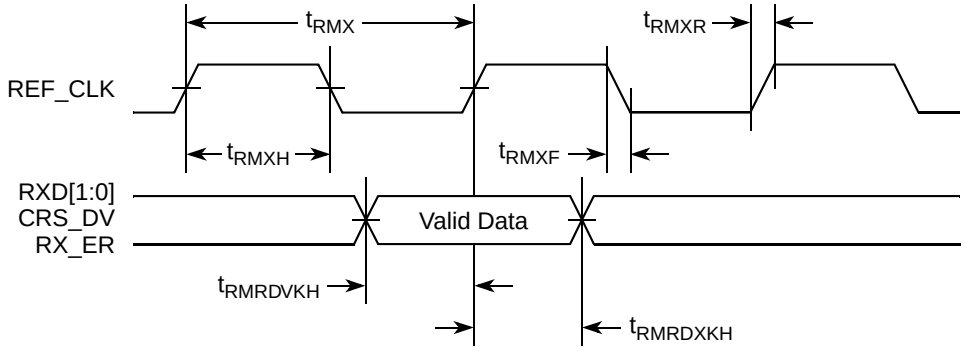

Figure 15. RMII Receive AC Timing Diagram

9.2.3 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 29. RGMII and RTBI AC Timing Specifications

At recommended operating conditions (see Table 2)

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	–0.6	—	0.6	ns
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.6	ns

Table 30. MII Management DC Electrical Characteristics Powered at 3.3 V (continued)

Parameter	Symbol	Conditions		Min	Max	Unit
Input low current	I_{IL}	NVDD = Max	V_{IN} = 0.5 V	–600	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

9.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 31. MII Management AC Timing Specifications

At recommended operating conditions with NVDD is 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	170	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 133 MHz, the maximum frequency is 4.16 MHz and the minimum frequency is 0.593 MHz).
3. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 133 MHz, the delay is 60 ns).

This figure shows the MII management AC timing diagram.

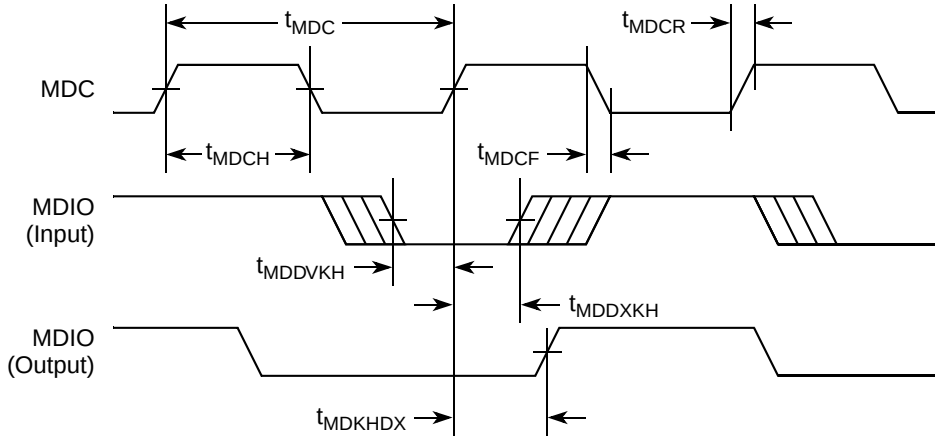

Figure 17. MII Management Interface Timing Diagram

9.4 1588 Timer Specifications

This section describes the DC and AC electrical specifications for the 1588 timer.

9.4.1 1588 Timer DC Specifications

This table provides the 1588 timer DC specifications.

Table 32. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NVDD	—	± 5	μA

9.4.2 1588 Timer AC Specifications

This table provides the 1588 timer AC specifications.

Table 33. 1588 Timer AC Specifications

Parameter	Symbol	Min	Max	Unit	Note
Timer clock cycle time	t_{TMRCK}	0	70	MHz	1
Input setup to timer clock	t_{TMRCKS}	—	—	—	2, 3
Input hold from timer clock	t_{TMRCKH}	—	—	—	2, 3
Output clock to output valid	t_{GCLKNV}	0	6	ns	
Timer alarm to output valid	t_{TMRAL}	—	—	—	2

Table 35. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	XCOREVDD	0.95	1.0	1.05	V	—
Output high voltage	VOH	—	—	$XCOREVDD_{-Typ}/2 + \lvert V_{OD}\rvert_{-max}/2$	mV	1
Output low voltage	VOL	$XCOREVDD_{-Typ}/2 - \lvert V_{OD}\rvert_{-max}/2$	—	—	mV	1
Output ringing	V_{RING}	—	—	10	%	—
Output differential voltage[2, 3, 5]	$\lvert V_{OD}\rvert$	323	500	725	mV	Equalization setting: 1.0x
		296	459	665		Equalization setting: 1.09x
		269	417	604		Equalization setting: 1.2x
		243	376	545		Equalization setting: 1.33x
		215	333	483		Equalization setting: 1.5x
		189	292	424		Equalization setting: 1.71x
		162	250	362		Equalization setting: 2.0x
Output offset voltage	V_{OS}	425	500	575	mV	1, 4
Output impedance (single-ended)	R_O	40	—	60	Ω	—
Mismatch in a pair	ΔR_O	—	—	10	%	—
Change in V_{OD} between “0” and “1”	$\Delta \lvert V_{OD}\rvert$	—	—	25	mV	—
Change in V_{OS} between “0” and “1”	ΔV_{OS}	—	—	25	mV	—
Output current on short to GND	I_{SA}, I_{SB}	—	—	40	mA	—

Note:

1. This will not align to DC-coupled SGMII. $XCOREVDD_{-Typ}$=1.0V.
2. $\lvert V_{OD}\rvert = \lvert V_{TXn} - V_{\overline{TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX-DIFFp-p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the table assumes the following transmit equalization setting in the TXEQA (for SerDes lane A) or TXEQE (for SerDes lane E) bit field of MPC8315E’s SerDes Control Register 0:
   - The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. V_{OS} is also referred to as output common mode voltage.
5. The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $XCOREVDD_{-Typ}$=1.0V, no common mode offset variation (V_{OS} = 500 mV), SerDes transmitter is terminated with 100-Ω differential load between TX[n] and $\overline{TX}$[n].

Table 38. SGMII Receive AC Timing Specifications

At recommended operating conditions with XCOREVDD = 1.0V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal Jitter Tolerance	JSIN	0.1	—	—	UI p-p	1
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1
Bit Error Ratio	BER	—	—	10^{-12}		—
Unit Interval	UI	799.92	800	800.08	ps	2
AC Coupling Capacitor	C_{TX}	5	—	200	nF	3

Note:

1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It's recommended to be placed near the device transmitter outputs.
4. Refer to RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications.

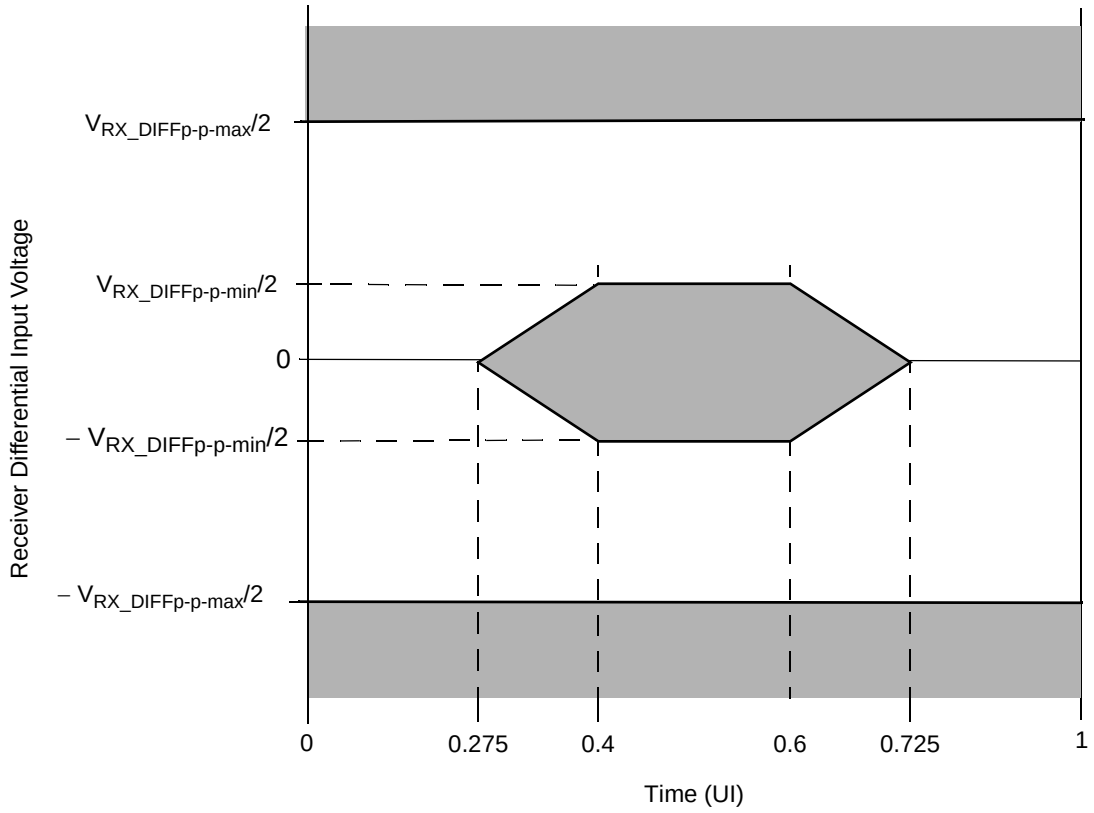

Figure 20. SGMII Receiver Input Compliance Mask

Table 50. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol [1]	Min	Max	Unit	Note
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Note:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

This table shows the PCI AC Timing Specifications at 33 MHz.

Table 51. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol [1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	4.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Note:

1. Note that the symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

This figure provides the AC test load for PCI.

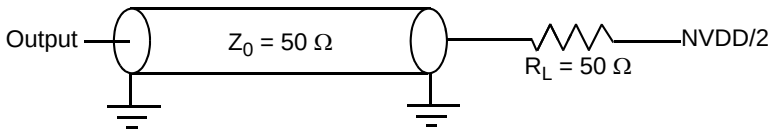

Figure 35. PCI AC Test Load

This figure shows the PCI input AC timing conditions.

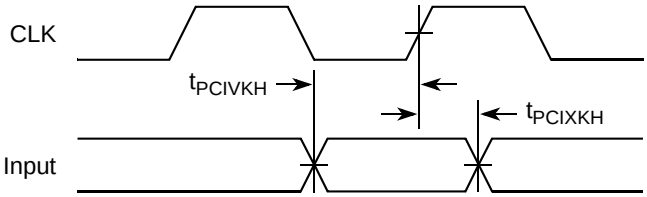

Figure 36. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

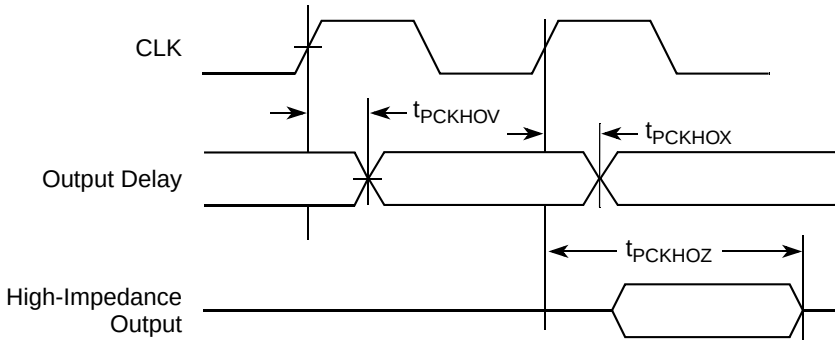

Figure 37. PCI Output AC Timing Measurement Condition

15 High-Speed Serial Interfaces (HSSI)

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

15.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 38 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (TXn and $\overline{\text{TXn}}$) or a receiver input (RXn and $\overline{\text{RXn}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals TXn, $\overline{\text{TXn}}$, RXn and $\overline{\text{RXn}}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's Single-Ended Swing.
2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

between 100 mV and 400 mV. Figure 40 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

— For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to XCOREVSS. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (XCOREVSS). Figure 41 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- **Single-ended Mode**
  — The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400mV and 800mV peak-peak (from Vmin to Vmax) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  — The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.
  — To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

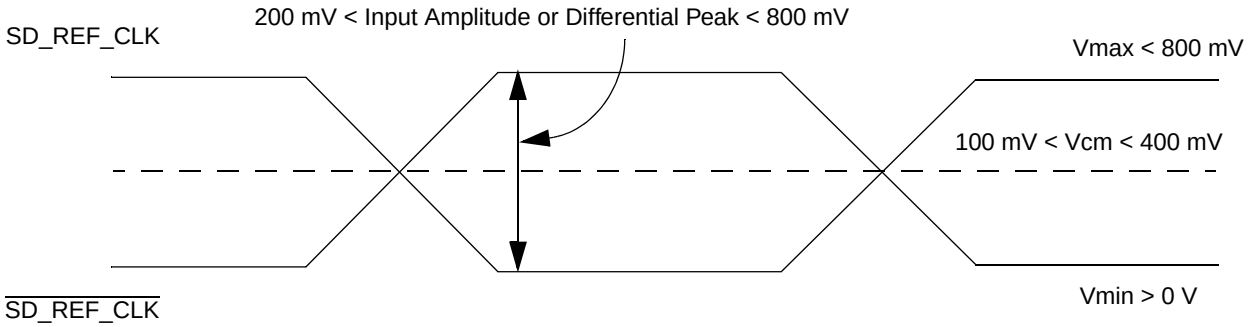

Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

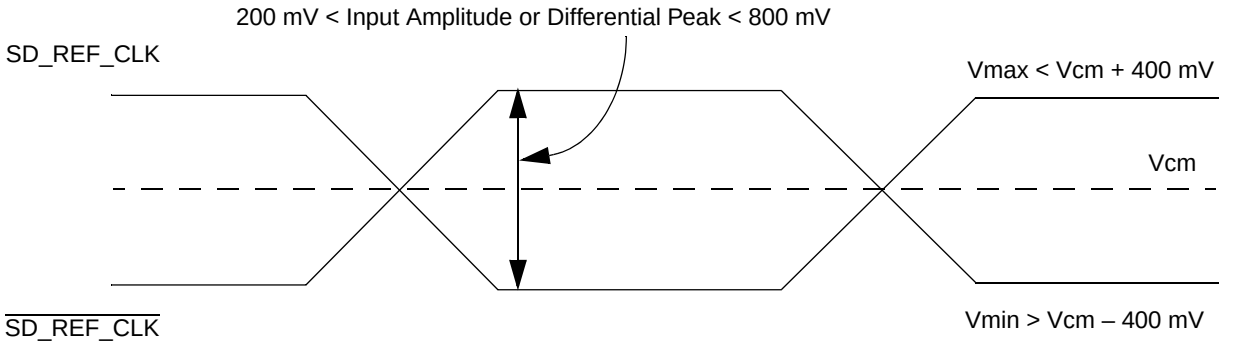

Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)

15.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15MHz is filtered by the PLL. The most problematic phase noise occurs in the 1-15MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters common to SGMII and PCI Express protocols.

Table 52. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XCOREVDD= 1.0V ± 5%

Parameter	Symbol	Min	Max	Unit	Note
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	+200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{\text{SDn\_REF\_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Note:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from -200 mV to +200 mV on the differential waveform (derived from SDn_REF_CLK minus $\overline{\text{SDn\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 47.
4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for $\overline{\text{SDn\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SDn\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SDn_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SDn\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 48.

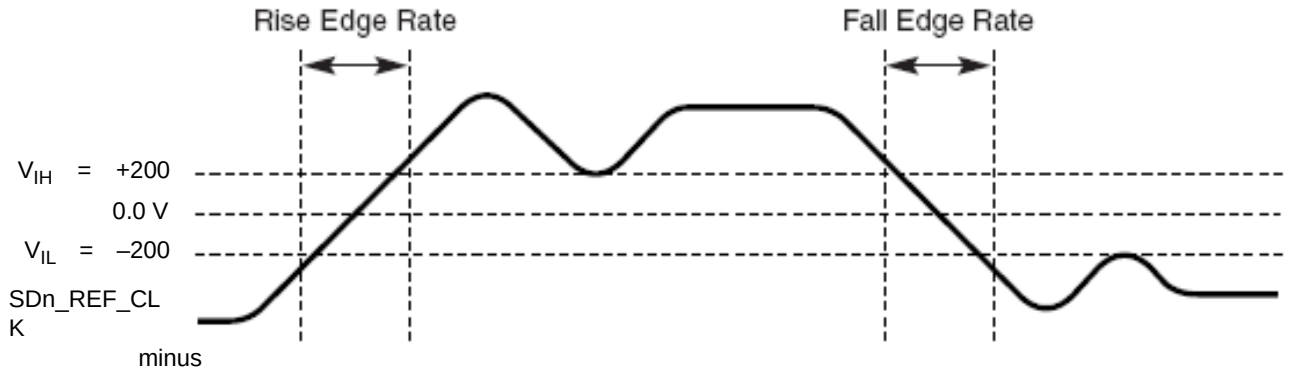

Figure 47. Differential Measurement Points for Rise and Fall Time

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

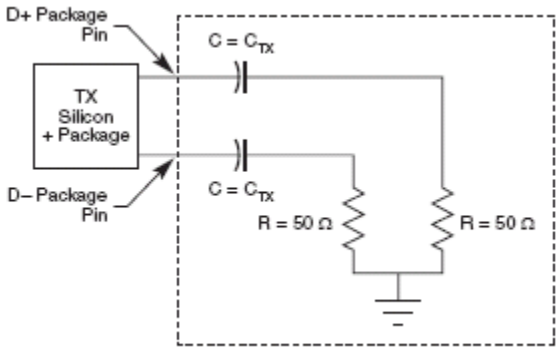

Figure 52. Compliance Test/Measurement Load

17 Serial ATA (SATA)

The serial ATA (SATA) of the MPC8315E is designed to comply with Serial ATA 2.5 Specification. Note that the external cabled applications or long backplane applications (Gen1x & Gen2x) are not supported.

17.1 Requirements for SATA REF_CLK

The reference clock for MPC8315E is a single ended input clock required for the SATA Interface operation. The AC requirements for the SATA reference clock are listed in the this table.

Table 56. Reference Clock Input Requirements

Parameter	Symbol	Conditions	Min	Typical	Max	Unit	Note
Frequency range	t_{CLK_REF}	—	50	75	150	MHz	1
Clock frequency tolerance	t_{CLK_TOL}	—	-350	0	+350	ppm	—
Input High Voltage	V_{CLK_INHI}	—	2.0	—	—	V	—
Input Low Voltage	V_{CLK_INLo}	—	—	—	0.7	V	—
Reference clock rise and fall time	t_{CLK_RISE}/ t_{CLK_FALL}	20% to 80% of nominal amplitude	—	—	2	ns	—
Reference clock duty cycle	t_{CLK_DUTY}	Measured at 1.6V	40	50	60	%	—

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
LGPL1/LFALE	AA28	O	$NVDD3_{OFF}$	—
LGPL2/$\overline{\text{LFRE}}$/$\overline{\text{LOE}}$	Y25	O	$NVDD3_{OFF}$	12
LGPL3/$\overline{\text{LFWP}}$	Y24	O	$NVDD3_{OFF}$	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/$\overline{\text{LFRB}}$	AA26	I/O	$NVDD3_{OFF}$	2
LGPL5	AF22	O	$NVDD3_{OFF}$	12
LCLK0	AH25	O	$NVDD3_{OFF}$	11
LCLK1	AD24	O	$NVDD3_{OFF}$	11
DUART				
UART_SOUT1/MSRCID0 (DDR ID)/LSRCID0	C15	O	$NVDD2_{OFF}$	—
UART_SIN1/MSRCID1 (DDR ID)/LSRCID1	B16	I/O	$NVDD2_{OFF}$	—
$\overline{\text{UART\_CTS}}$[1]/MSRCID2 (DDR ID)/LSRCID2	D16	I/O	$NVDD2_{OFF}$	—
$\overline{\text{UART\_RTS}}$[1]/MSRCID3 (DDR ID)/LSRCID3	B17	O	$NVDD2_{OFF}$	—
UART_SOUT2/MSRCID4 (DDR ID)/LSRCID4	A16	O	$NVDD2_{OFF}$	—
UART_SIN2/MDVAL (DDR ID)/LDVAL	C16	I/O	$NVDD2_{OFF}$	—
$\overline{\text{UART\_CTS}}$[2]	A17	I	$NVDD2_{OFF}$	—
$\overline{\text{UART\_RTS}}$[2]	A18	O	$NVDD2_{OFF}$	—
I^2C interface				
IIC_SDA/$\overline{\text{CKSTOP\_OUT}}$	N1	I/O	$NVDD4_{OFF}$	2
IIC_SCL/$\overline{\text{CKSTOP\_IN}}$	N2	I/O	$NVDD4_{OFF}$	2
Interrupts				
$\overline{\text{MCP\_OUT}}$	W1	O	$NVDD1_{OFF}$	2
$\overline{\text{IRQ}}$[0]/$\overline{\text{MCP\_IN}}$	Y3	I	$NVDD1_{OFF}$	—
$\overline{\text{IRQ}}$[1]	E1	I	$NVDD1_{ON}$	—
$\overline{\text{IRQ}}$[2]	A7	I	$NVDD1_{ON}$	—
$\overline{\text{IRQ}}$[3]	AA1	I	$NVDD1_{OFF}$	—
$\overline{\text{IRQ}}$[4]	Y5	I	$NVDD1_{OFF}$	—
$\overline{\text{IRQ}}$[5]/$\overline{\text{CORE\_SRESET\_IN}}$	AA2	I	$NVDD1_{OFF}$	—
$\overline{\text{IRQ}}$[6] /$\overline{\text{CKSTOP\_OUT}}$	AA4	I/O	$NVDD1_{OFF}$	—
$\overline{\text{IRQ}}$[7]/$\overline{\text{CKSTOP\_IN}}$	AA5	I	$NVDD1_{OFF}$	—
Configuration				
$\overline{\text{CFG\_CLKIN\_DIV}}$	A5	I	$NVDD1_{ON}$	12
EXT_PWR_CTRL	D3	O	$NVDD1_{ON}$	12
PMC_PWR_OK	D4	I	—	12

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
USB_DP	A11	I/O	USB_VDDA	—
USB_DM	A12	I/O	USB_VDDA	—
USB_VBUS	C12	I	—	—
USB_TPA	A14	O	—	—
USB_RBIAS	D14	I	—	8
USB_PLL_PWR3	A13	I	—	—
USB_PLL_GND0 & USB_PLL_GND1	D13	I	—	—
USB_PLL_PWR1	B13	I	—	—
USB_VSSA_BIAS	E14	I	—	—
USB_VDDA_BIAS	C14	I	—	—
USB_VSSA	E13	I	—	—
USB_VDDA	E12	I	—	—
GPIO				
GPIO_0/$\overline{\text{DMA\_DREQ1}}$/$\overline{\text{GTM1\_TOUT1}}$	C5	I/O	$NVDD1_{ON}$	—
GPIO_1/$\overline{\text{DMA\_DACK1}}$/GTM1_TIN2/GTM2_TIN1	A4	I/O	$NVDD1_{ON}$	—
GPIO_2/$\overline{\text{DMA\_DONE1}}$/$\overline{\text{GTM1\_TGATE2}}$/$\overline{\text{GTM2\_TGATE1}}$	K3	I/O	$NVDD4_{OFF}$	—
GPIO_3/GTM1_TIN3/GTM2_TIN4	K1	I/O	$NVDD4_{OFF}$	—
GPIO_4/$\overline{\text{GTM1\_TGATE3}}$/$\overline{\text{GTM2\_TGATE4}}$	K2	I/O	$NVDD4_{OFF}$	—
GPIO_5/$\overline{\text{GTM1\_TOUT3}}$/$\overline{\text{GTM2\_TOUT1}}$	L5	I/O	$NVDD4_{OFF}$	—
GPIO_6/GTM1_TIN4/GTM2_TIN3	L3	I/O	$NVDD4_{OFF}$	—
GPIO_7/$\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$	L1	I/O	$NVDD4_{OFF}$	—
GPIO_8/USBDR_DRIVE_VBUS/GTM1_TIN1/GTM2_TIN2	M1	I/O	$NVDD4_{OFF}$	—
GPIO_9/USBDR_PWRFAULT/$\overline{\text{GTM1\_TGATE1}}$/$\overline{\text{GTM2\_TGATE2}}$	M2	I/O	$NVDD4_{OFF}$	—
GPIO_10/USBDR_PCTL0/$\overline{\text{GTM1\_TOUT2}}$/$\overline{\text{GTM2\_TOUT1}}$	M5	I/O	$NVDD4_{OFF}$	—
GPIO_11/USBDR_PCTL1/$\overline{\text{GTM1\_TOUT4}}$/$\overline{\text{GTM2\_TOUT3}}$	M4	I/O	$NVDD4_{OFF}$	—
SPI				
SPIMOSI/GPIO_15	W3	I/O	$NVDD1_{OFF}$	—
SPIMISO/GPIO_16	W4	I/O	$NVDD1_{OFF}$	—
SPICLK	Y1	I/O	$NVDD1_{OFF}$	—
SPISEL/GPIO_17	W2	I/O	$NVDD1_{OFF}$	—

28 Revision History

This table summarizes a revision history for this document.

Table 83. Revision History

Revision	Date	Substantive Change(s)
2	11/2011	• In Table 70: – Corrected Note 11 to pull down. – Note 10 added to RESREF pin. Removed all other instances of Note 10. – Added pull up information.
1	11/2011	• Added Notes 4, 5, 6, and 7 in Table 2. • In Table 6: – Decoupled PCI_CLK and SYS_CLK_IN rise and fall times. – Relaxed maximum rise/fall time of SYS_CLK_IN from 1.2 ns to 4 ns. – Modified Note 2. – Updated SYS_CLK_IN/PCI_CLK frequency from 66 MHz to 66.67 MHz. • Added Note 4 to Table 9. • Added a note stating “eTSEC should be interfaced with peripheral operating at same voltage level.” in Section 9.1.1, “MII, RMII, RGMII, and RTBI DC Electrical Characteristics.” • Added a note in Table 26 stating “The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm." • Added a note in Table 29 stating “The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm • In Table 42, changed min/max values of t_{CLK_TOL} from 0.05 to 0.005. • Added $t_{LALEHOV}$ parameter to Table 44 • Replaced 50 with 50 Ω in Section 16.5, “Receiver Compliance Eye Diagrams.” • In Table 70: – Added Pull up and Pull down information. – Removed Note 2 from TSEC_MDIO. • Removed configuration 2 from Table 77. • Removed Preliminary from Section 25, “Thermal.” • Removed MDIO signal from Section 26.7, “Pull-Up Resistor Requirements” as this signal is not open drain. • Replaced LCCR with LCRR throughout. • Replaced SYS_CLKIN with SYS_CLK_IN throughout. • Replaced all LBIUCM with LBCM. • Replaced all SYS_CR_CLK_IN and SYS_CR_CLK_OUT with SYS_XTAL_IN and SYS_XTAL_OUT, respectively. Replaced all USB_CR_CLK_IN and USB_CR_CLK_OUT with USB_XTAL_IN and USB_XTAL_OUT, respectively. • Added rise/fall time spec for TDM CLK
0	05/2009	Initial public release