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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LCD, LVD, POR, PWM, WDT
Number of I/O	98
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 42x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk40dx256zvlq10

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5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength					
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -9\text{ mA}$	$V_{DD} - 0.5$	—	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -3\text{ mA}$	$V_{DD} - 0.5$	—	—	V	
	Output high voltage — low drive strength					
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -2\text{ mA}$	$V_{DD} - 0.5$	—	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -0.6\text{ mA}$	$V_{DD} - 0.5$	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage — high drive strength					2
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 9\text{ mA}$	—	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 3\text{ mA}$	—	—	0.5	V	
	Output low voltage — low drive strength					
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 2\text{ mA}$	—	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 0.6\text{ mA}$	—	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{INA}	Input leakage current, analog pins and digital pins configured as analog inputs					3, 4
	• $V_{SS} \leq V_{IN} \leq V_{DD}$					
	• All pins except EXTAL32, XTAL32, EXTAL, XTAL	—	0.002	0.5	μA	
	• EXTAL (PTA18) and XTAL (PTA19)	—	0.004	1.5	μA	
	• EXTAL32, XTAL32	—	0.075	10	μA	
I_{IND}	Input leakage current, digital pins					4, 5
	• $V_{SS} \leq V_{IN} \leq V_{IL}$					
	• All digital pins	—	0.002	0.5	μA	
	• $V_{IN} = V_{DD}$					
	• All digital pins except PTD7	—	0.002	0.5	μA	
	• PTD7	—	0.004	1	μA	
I_{IND}	Input leakage current, digital pins					4, 5, 6
	• $V_{IL} < V_{IN} < V_{DD}$					
	• $V_{DD} = 3.6\text{ V}$	—	18	26	μA	
	• $V_{DD} = 3.0\text{ V}$	—	12	49	μA	
	• $V_{DD} = 2.5\text{ V}$	—	8	13	μA	
	• $V_{DD} = 1.7\text{ V}$	—	3	6	μA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	N/A	—	mA	7
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	N/A	—	mA	8
I _{DD_STOP}	Stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.59	1.4	mA	
	• @ 70°C	—	2.26	7.9	mA	
	• @ 105°C	—	5.94	19.2	mA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25°C	—	93	435	μA	
	• @ 70°C	—	520	2000	μA	
	• @ 105°C	—	1350	4000	μA	
I _{DD_LLS}	Low leakage stop mode current at 3.0 V					9
	• @ –40 to 25°C	—	4.8	20	μA	
	• @ 70°C	—	28	68	μA	
	• @ 105°C	—	126	270	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					9
	• @ –40 to 25°C	—	3.1	8.9	μA	
	• @ 70°C	—	17	35	μA	
	• @ 105°C	—	82	148	μA	
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• @ –40 to 25°C	—	2.2	5.4	μA	
	• @ 70°C	—	7.1	12.5	μA	
	• @ 105°C	—	41	125	μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25°C	—	2.1	7.6	μA	
	• @ 70°C	—	6.2	13.5	μA	
	• @ 105°C	—	30	46	μA	
I _{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	• @ –40 to 25°C	—	0.33	0.39	μA	
	• @ 70°C	—	0.60	0.78	μA	
	• @ 105°C	—	1.97	2.9	μA	

Table continues on the next page...

5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CAN, CMT, and I²C signals.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	16	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Mode select (EZP_CS) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength) - Slew disabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$ - Slew enabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$	— — — —	12 6 36 24	ns ns ns ns	4
	Port rise and fall time (low drive strength) - Slew disabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$ - Slew enabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$	— — — —	12 6 36 24	ns ns ns ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load

5.4 Thermal specifications

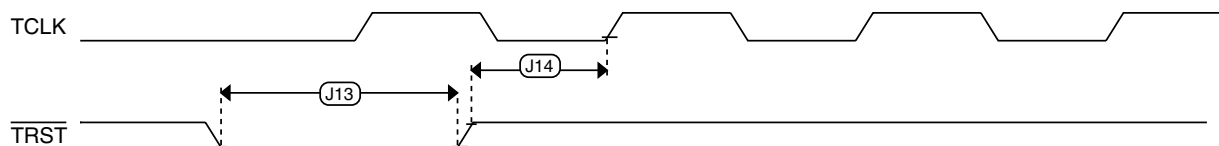


Figure 8. TRST timing

6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

6.3.1 MCG specifications

Table 15. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{\text{ints_ft}}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
$f_{\text{ints_t}}$	Internal reference frequency (slow clock) — user trimmed — over fixed voltage and temperature range of 0–70°C	31.25	—	38.2	kHz	
$\Delta f_{\text{dco_res_t}}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	% f_{dco}	1
$\Delta f_{\text{dco_t}}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 1.5	± 4.5	% f_{dco}	1
$f_{\text{intf_ft}}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
$f_{\text{intf_t}}$	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
$f_{\text{loc_low}}$	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{\text{ints_t}}$	—	—	kHz	
$f_{\text{loc_high}}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{\text{ints_t}}$	—	—	kHz	
FLL						
$f_{\text{fll_ref}}$	FLL reference frequency range	31.25	—	39.0625	kHz	

Table continues on the next page...

Table 15. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fil_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f _{fil_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f _{fil_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fil_ref}	80	83.89	100	MHz	
f _{dco_t_DMX32}	DCO output frequency	Low range (DRS=00) 732 × f _{fil_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f _{fil_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f _{fil_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f _{fil_ref}	—	95.98	—	MHz	
J _{cyc_fll}	FLL period jitter - f_{VCO} = 48 MHz - f_{VCO} = 98 MHz	—	180	—	ps		
		—	150	—			
t _{fil_acquire}	FLL target frequency acquisition time		—	—	1	ms	6
PLL							
f _{vco}	VCO operating frequency		48.0	—	100	MHz	
I _{pll}	PLL operating current PLL @ 96 MHz (f_{osc_hi_1} = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1060	—	μA	7
I _{pll}	PLL operating current PLL @ 48 MHz (f_{osc_hi_1} = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	600	—	μA	7
f _{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J _{cyc_pll}	PLL period jitter (RMS) - f_{vco} = 48 MHz - f_{vco} = 100 MHz	—	120	—	ps	8	
		—	50	—	ps		
J _{acc_pll}	PLL accumulated jitter over 1μs (RMS) - f_{vco} = 48 MHz - f_{vco} = 100 MHz	—	1350	—	ps	8	
		—	600	—	ps		
D _{lock}	Lock entry frequency tolerance		± 1.49	—	± 2.98	%	
D _{unl}	Lock exit frequency tolerance		± 4.47	—	± 5.97	%	
t _{pll_lock}	Lock detector detection time		—	—	150 × 10 ⁻⁶ + 1075(1/f _{pll_ref})	s	9

Table 21. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{pgmchk}	Program Check execution time	—	—	45	μs	1
t_{rdsrc}	Read Resource execution time	—	—	30	μs	1
t_{pgm4}	Program Longword execution time	—	65	145	μs	
$t_{ersblk256k}$	Erase Flash Block execution time • 256 KB program/data flash	—	435	3700	ms	2
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
$t_{pgmsec512}$	Program Section execution time • 512 bytes flash	—	2.4	—	ms	
$t_{pgmsec1k}$	• 1 KB flash	—	4.7	—	ms	
$t_{pgmsec2k}$	• 2 KB flash	—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	μs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	μs	
t_{ersall}	Erase All Blocks execution time	—	870	7400	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1
$t_{swapx01}$	Swap Control execution time • control code 0x01	—	200	—	μs	
$t_{swapx02}$	• control code 0x02	—	70	150	μs	
$t_{swapx04}$	• control code 0x04	—	70	150	μs	
$t_{swapx08}$	• control code 0x08	—	—	30	μs	
$t_{pgmpart64k}$ $t_{pgmpart256k}$	Program Partition for EEPROM execution time • 256 KB FlexNVM	—	450	—	ms	
$t_{setramff}$	Set FlexRAM Function execution time: • Control Code 0xFF	—	70	—	μs	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.8	1.2	ms	
$t_{setram64k}$	• 64 KB EEPROM backup	—	1.3	1.9	ms	
$t_{setram256k}$	• 256 KB EEPROM backup	—	4.5	5.5	ms	
Byte-write to FlexRAM for EEPROM operation						
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	175	260	μs	3
$t_{eewr8b32k}$	Byte-write to FlexRAM execution time: • 32 KB EEPROM backup	—	385	1800	μs	
$t_{eewr8b64k}$	• 64 KB EEPROM backup	—	475	2000	μs	
$t_{eewr8b128k}$	• 128 KB EEPROM backup	—	650	2400	μs	
$t_{eewr8b256k}$	• 256 KB EEPROM backup	—	1000	3200	μs	
Word-write to FlexRAM for EEPROM operation						

Table continues on the next page...

- EEPROM — allocated FlexNVM for each EEPROM subsystem based on DEPART; entered with the Program Partition command
- EEESPLIT — FlexRAM split factor for subsystem; entered with the Program Partition command
- EEESIZE — allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write_efficiency —
 - 0.25 for 8-bit writes to FlexRAM
 - 0.50 for 16-bit or 32-bit writes to FlexRAM
- n_{nvmcyed} — data flash cycling endurance (the following graph assumes 10,000 cycles)

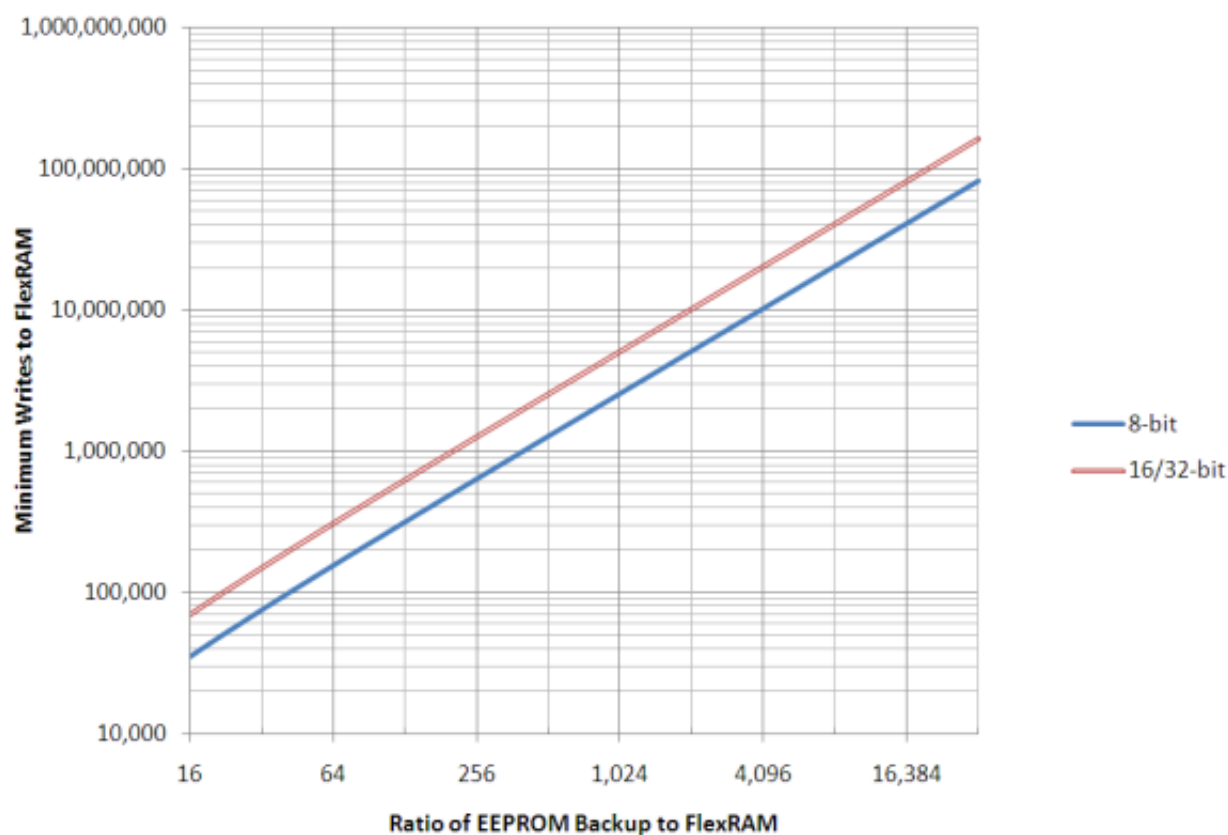


Figure 9. EEPROM backup writes to FlexRAM

6.4.2 EzPort Switching Specifications

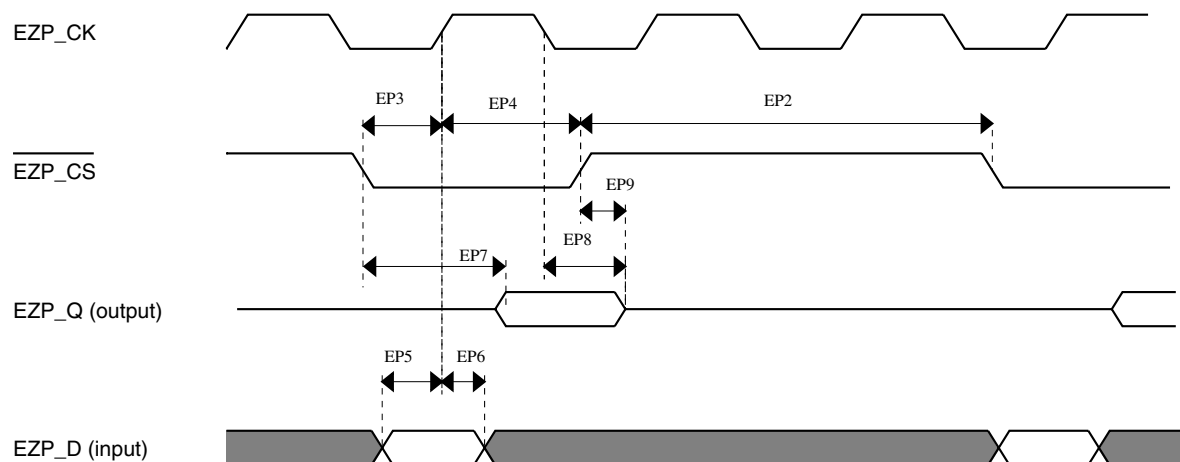
Table 24. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

Table continues on the next page...

Table 24. EzPort switching specifications (continued)

Num	Description	Min.	Max.	Unit
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	EZP_CS negation to next EZP_CS assertion	$2 \times t_{EZP_CK}$	—	ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to EZP_CS input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	16	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	EZP_CS negation to EZP_Q tri-state	—	12	ns

**Figure 10. EzPort Timing Diagram**

6.4.3 Flexbus Switching Specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

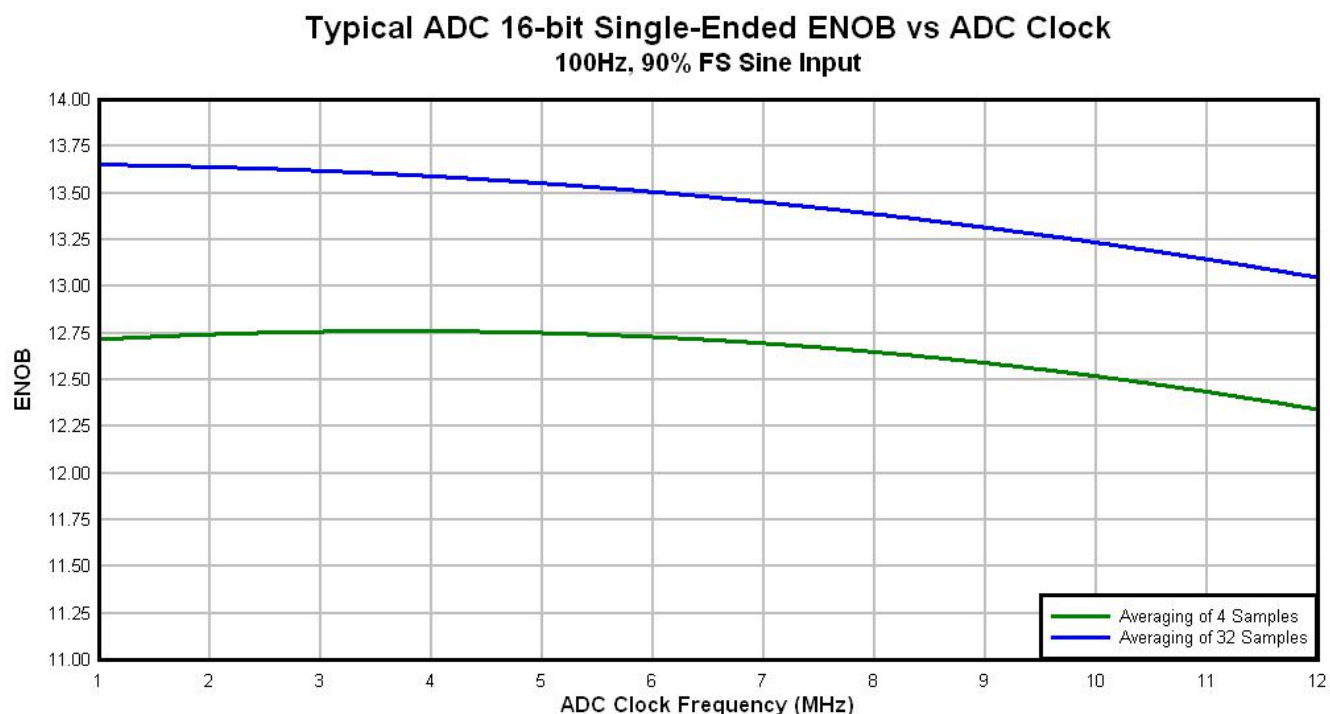


Figure 15. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.6.1.3 16-bit ADC with PGA operating conditions

Table 29. 16-bit ADC with PGA operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
V _{REFPGA}	PGA ref voltage		V _{REF_OU} T	V _{REF_OU} T	V _{REF_OU} T	V	2, 3
V _{ADIN}	Input voltage		V _{SSA}	—	V _{DDA}	V	
V _{CM}	Input Common Mode range		V _{SSA}	—	V _{DDA}	V	
R _{PGAD}	Differential input impedance	Gain = 1, 2, 4, 8 Gain = 16, 32 Gain = 64	— — —	128 64 32	— — —	kΩ	IN+ to IN- ⁴
R _{AS}	Analog source resistance		—	100	—	Ω	5
T _S	ADC sampling time		1.25	—	—	μs	6

Table continues on the next page...

Table 29. 16-bit ADC with PGA operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
C _{rate}	ADC conversion rate	≤ 13 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	18.484	—	450	Ksps	7
		16 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	37.037	—	250	Ksps	8

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. ADC must be configured to use the internal voltage reference (VREF_OUT)
3. PGA reference is internally connected to the VREF_OUT pin. If the user wishes to drive VREF_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
4. For single ended configurations the input impedance of the driven input is R_{PGAD}/2
5. The analog source resistance (R_{AS}), external to MCU, should be kept as minimum as possible. Increased R_{AS} causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
6. The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25μs time should be allowed for F_{in}=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1

6.6.1.4 16-bit ADC with PGA characteristics

Table 30. 16-bit ADC with PGA characteristics

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
I _{DDA_PGA}	Supply current	Low power (ADC_PGA[PGALPb]=0)	—	420	644	μA	2
I _{DC_PGA}	Input DC current		$\frac{2}{R_{PGAD}} \left(\frac{(V_{REFPGA} \times 0.583) - V_{CM}}{(Gain+1)} \right)$			A	3
		Gain =1, V _{REFPGA} =1.2V, V _{CM} =0.5V	—	1.54	—	μA	
		Gain =64, V _{REFPGA} =1.2V, V _{CM} =0.1V	—	0.57	—	μA	

Table continues on the next page...

Table 30. 16-bit ADC with PGA characteristics (continued)

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
ENOB	Effective number of bits	• Gain=1, Average=4	11.6	13.4	—	bits	16-bit differential mode, $f_{in}=100\text{Hz}$
		• Gain=64, Average=4	7.2	9.6	—	bits	
		• Gain=1, Average=32	12.8	14.5	—	bits	
		• Gain=2, Average=32	11.0	14.3	—	bits	
		• Gain=4, Average=32	7.9	13.8	—	bits	
		• Gain=8, Average=32	7.3	13.1	—	bits	
		• Gain=16, Average=32	6.8	12.5	—	bits	
		• Gain=32, Average=32	6.8	11.5	—	bits	
		• Gain=64, Average=32	7.5	10.6	—	bits	
SINAD	Signal-to-noise plus distortion ratio	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	

1. Typical values assume $V_{DDA}=3.0\text{V}$, $\text{Temp}=25^{\circ}\text{C}$, $f_{ADCK}=6\text{MHz}$ unless otherwise stated.
2. This current is a PGA module adder, in addition to ADC conversion currents.
3. Between $\text{IN}+$ and $\text{IN}-$. The PGA draws a DC current from the input terminals. The magnitude of the DC current is a strong function of input common mode voltage (V_{CM}) and the PGA gain.
4. $\text{Gain} = 2^{\text{PGAG}}$
5. After changing the PGA gain setting, a minimum of 2 ADC+PGA conversions should be ignored.
6. Limit the input signal swing so that the PGA does not saturate during operation. Input signal swing is dependent on the PGA reference voltage and gain setting.

6.6.2 CMP and 6-bit DAC electrical specifications

Table 31. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode ($\text{EN}=1$, $\text{PMODE}=1$)	—	—	200	μA
$I_{DDL S}$	Supply current, low-speed mode ($\text{EN}=1$, $\text{PMODE}=0$)	—	—	20	μA
V_{AIN}	Analog input voltage	$V_{SS} - 0.3$	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis ¹				
		• $\text{CR0}[\text{HYSTCTR}] = 00$	5	—	mV
		• $\text{CR0}[\text{HYSTCTR}] = 01$	10	—	mV
		• $\text{CR0}[\text{HYSTCTR}] = 10$	20	—	mV
		• $\text{CR0}[\text{HYSTCTR}] = 11$	30	—	mV
V_{CMPOH}	Output high	$V_{DD} - 0.5$	—	—	V
V_{CMPOI}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode ($\text{EN}=1$, $\text{PMODE}=1$)	20	50	200	ns

Table continues on the next page...

6.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit usb.org.

6.8.2 USB DCD electrical specifications

Table 38. USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V _{DP_SRC}	USB_DP source voltage (up to 250 μ A)	0.5	—	0.7	V
V _{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I _{DP_SRC}	USB_DP source current	7	10	13	μ A
I _{DM_SINK}	USB_DM sink current	50	100	150	μ A
R _{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	k Ω
V _{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

6.8.3 USB VREG electrical specifications

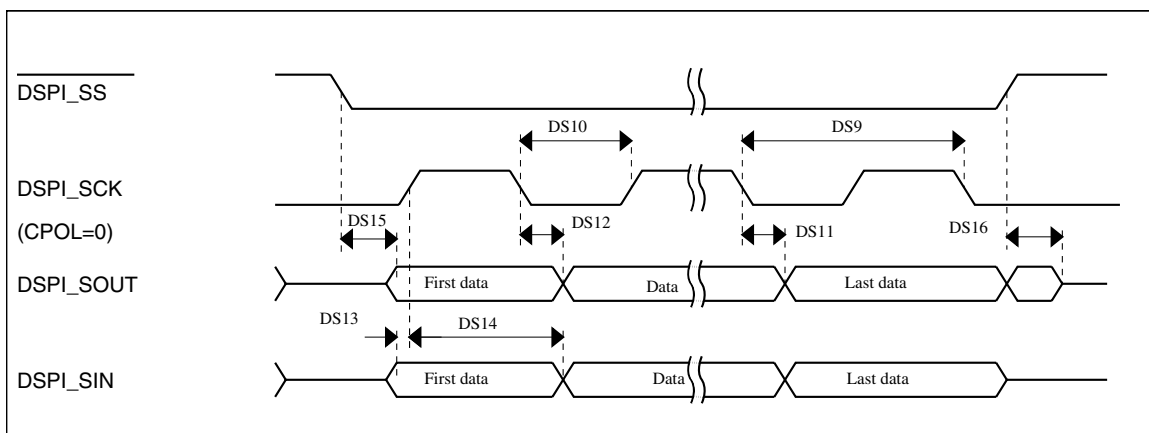
Table 39. USB VREG electrical specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
V _{REGIN}	Input supply voltage	2.7	—	5.5	V	
I _{DDon}	Quiescent current — Run mode, load current equal zero, input supply (V _{REGIN}) > 3.6 V	—	120	186	μ A	
I _{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.27	30	μ A	
I _{DDoff}	Quiescent current — Shutdown mode - V_{REGIN} = 5.0 V and temperature=25 °C - Across operating voltage and temperature	—	650	—	nA	
		—	—	4	μ A	
I _{LOADrun}	Maximum load current — Run mode	—	—	120	mA	
I _{LOADstby}	Maximum load current — Standby mode	—	—	1	mA	
V _{Reg33out}	Regulator output voltage — Input supply (V _{REGIN}) > 3.6 V - Run mode - Standby mode	3	3.3	3.6	V	
		2.1	2.8	3.6	V	
V _{Reg33out}	Regulator output voltage — Input supply (V _{REGIN}) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C _{OUT}	External output capacitor	1.76	2.2	8.16	μ F	
ESR	External output capacitor equivalent series resistance	1	—	100	m Ω	

Table continues on the next page...

Table 43. Slave mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit
DS9	DSPI_SCK input cycle time	$8 \times t_{\text{BUS}}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{\text{SCK}}/2) - 4$	$(t_{\text{SCK}}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SS to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SS input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	19	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	19	ns

**Figure 23. DSPI classic SPI timing — slave mode**

6.8.7 Inter-Integrated Circuit Interface (I²C) timing

Table 44. I²C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{\text{HD; STA}}$	4	—	0.6	—	μs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	μs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	μs
Set-up time for a repeated START condition	$t_{\text{SU; STA}}$	4.7	—	0.6	—	μs
Data hold time for I ² C bus devices	$t_{\text{HD; DAT}}$	0 ¹	3.45 ²	0 ³	0.9 ¹	μs
Data set-up time	$t_{\text{SU; DAT}}$	250 ⁴	—	100 ^{2, 5}	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	$20 + 0.1C_b$ ⁶	300	ns

Table continues on the next page...

6.8.9 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 45. SDHC switching specifications

Num	Symbol	Description	Min.	Max.	Unit
Card input clock					
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz
	f _{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t _{WL}	Clock low time	7	—	ns
SD3	t _{WH}	Clock high time	7	—	ns
SD4	t _{TLH}	Clock rise time	—	3	ns
SD5	t _{THL}	Clock fall time	—	3	ns
SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD6	t _{OD}	SDHC output delay (output valid)	-5	8.3	ns
SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD7	t _{ISU}	SDHC input setup time	5	—	ns
SD8	t _{IH}	SDHC input hold time	0	—	ns

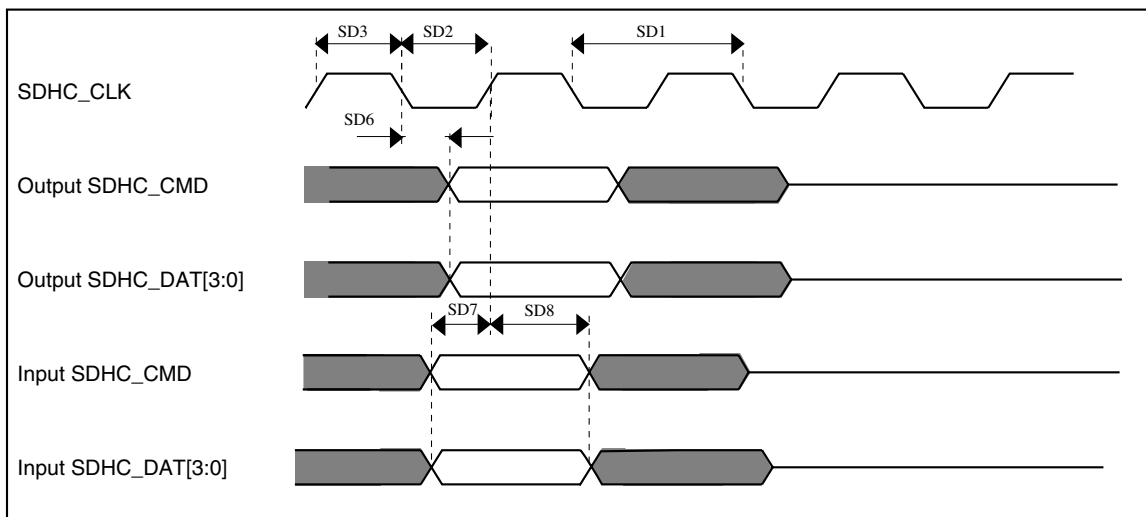


Figure 25. SDHC timing

6.8.10 I²S switching specifications

This section provides the AC timings for the I²S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S_BCLK) and/or the frame sync (I2S_FS) shown in the figures below.

Table 46. I²S master mode timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	$2 \times t_{SYS}$		ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	$5 \times t_{SYS}$	—	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	—	15	ns
S6	I2S_BCLK to I2S_FS output invalid	-2.5	—	ns
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	-3	—	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	20	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

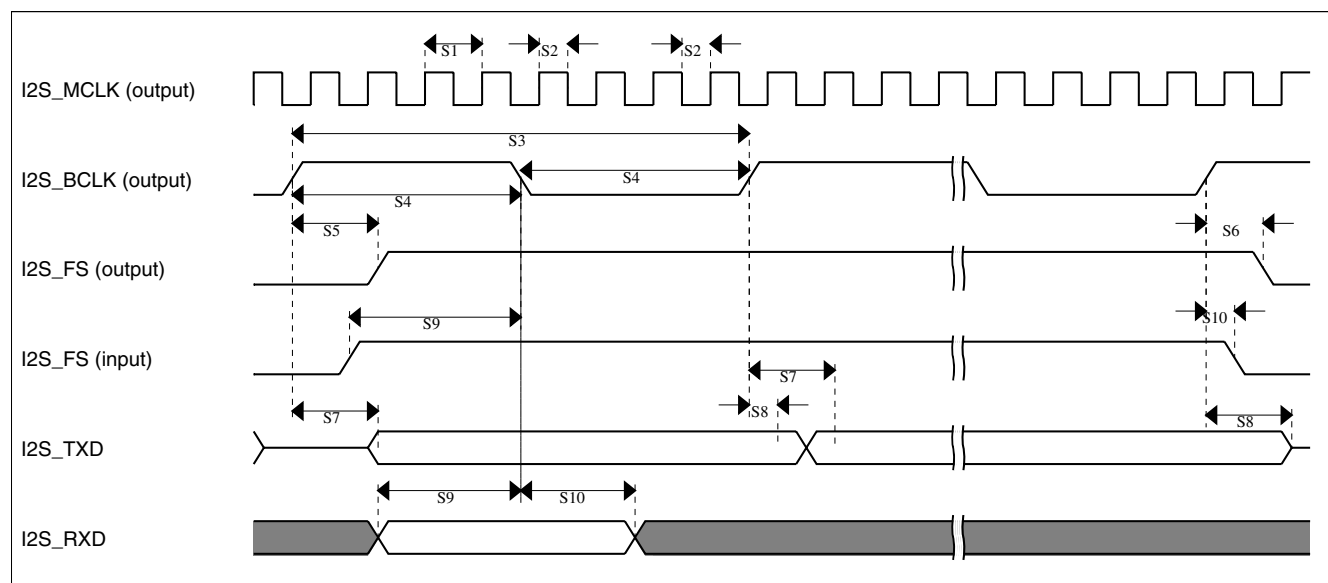


Figure 26. I²S timing — master mode

Table 49. I²S slave mode timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I ² S_BCLK cycle time (input)	8 x t _{SYS}	—	ns
S12	I ² S_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I ² S_FS input setup before I ² S_BCLK	10	—	ns
S14	I ² S_FS input hold after I ² S_BCLK	3.5	—	ns
S15	I ² S_BCLK to I ² S_TXD/I ² S_FS output valid	—	28.6	ns
S16	I ² S_BCLK to I ² S_TXD/I ² S_FS output invalid	0	—	ns
S17	I ² S_RXD setup before I ² S_BCLK	10	—	ns
S18	I ² S_RXD hold after I ² S_BCLK	2	—	ns

6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 50. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{DDTSI}	Operating voltage	1.71	—	3.6	V	
C _{ELE}	Target electrode capacitance range	1	20	500	pF	1
f _{REFmax}	Reference oscillator frequency	—	5.5	12.7	MHz	2
f _{ELEmax}	Electrode oscillator frequency	—	0.5	4.0	MHz	3
C _{REF}	Internal reference capacitor	0.5	1	1.2	pF	
V _{DELTA}	Oscillator delta voltage	100	600	760	mV	4
I _{REF}	Reference oscillator current source base current 1uA setting (REFCHRG=0) 32uA setting (REFCHRG=31)	— —	1.133 36	1.5 50	μA	3 , 5
I _{ELE}	Electrode oscillator current source base current 1uA setting (EXTCHRG=0) 32uA setting (EXTCHRG=31)	— —	1.133 36	1.5 50	μA	3 , 6
Pres5	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	7
Pres20	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	8
Pres100	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	9
MaxSens	Maximum sensitivity	0.003	12.5	—	fF/count	10
Res	Resolution	—	—	16	bits	
T _{Con20}	Response time @ 20 pF	8	15	25	μs	11
I _{TSI_RUN}	Current added in run mode	—	55	—	μA	
I _{TSI_LP}	Low power mode current adder	—	1.3	2.5	μA	12

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2. CAPTRM=7, DELVOL=7, and fixed external capacitance of 20 pF.

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
75	K12	PTA24	DISABLED		PTA24				FB_AD14			
76	J12	PTA25	DISABLED		PTA25				FB_AD13			
77	J11	PTA26	DISABLED		PTA26				FB_AD12			
78	J10	PTA27	DISABLED		PTA27				FB_AD11			
79	H12	PTA28	DISABLED		PTA28				FB_AD10			
80	H11	PTA29	DISABLED		PTA29				FB_AD19			
81	H10	PTB0/ LLWU_P5	LCD_P0/ ADC0_SE8/ ADC1_SE8/ TSIO_CH0	LCD_P0/ ADC0_SE8/ ADC1_SE8/ TSIO_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA	LCD_P0	
82	H9	PTB1	LCD_P1/ ADC0_SE9/ ADC1_SE9/ TSIO_CH6	LCD_P1/ ADC0_SE9/ ADC1_SE9/ TSIO_CH6	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_ PHB	LCD_P1	
83	G12	PTB2	LCD_P2/ ADC0_SE12/ TSIO_CH7	LCD_P2/ ADC0_SE12/ TSIO_CH7	PTB2	I2C0_SCL	UART0_RTS_ b			FTM0_FLT3	LCD_P2	
84	G11	PTB3	LCD_P3/ ADC0_SE13/ TSIO_CH8	LCD_P3/ ADC0_SE13/ TSIO_CH8	PTB3	I2C0_SDA	UART0_CTS_ b			FTM0_FLT0	LCD_P3	
85	G10	PTB4	LCD_P4/ ADC1_SE10	LCD_P4/ ADC1_SE10	PTB4					FTM1_FLT0	LCD_P4	
86	G9	PTB5	LCD_P5/ ADC1_SE11	LCD_P5/ ADC1_SE11	PTB5					FTM2_FLT0	LCD_P5	
87	F12	PTB6	LCD_P6/ ADC1_SE12	LCD_P6/ ADC1_SE12	PTB6						LCD_P6	
88	F11	PTB7	LCD_P7/ ADC1_SE13	LCD_P7/ ADC1_SE13	PTB7						LCD_P7	
89	F10	PTB8	LCD_P8	LCD_P8	PTB8		UART3_RTS_ b				LCD_P8	
90	F9	PTB9	LCD_P9	LCD_P9	PTB9	SPI1_PCS1	UART3_CTS_ b				LCD_P9	
91	E12	PTB10	LCD_P10/ ADC1_SE14	LCD_P10/ ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX			FTM0_FLT1	LCD_P10	
92	E11	PTB11	LCD_P11/ ADC1_SE15	LCD_P11/ ADC1_SE15	PTB11	SPI1_SCK	UART3_TX			FTM0_FLT2	LCD_P11	
93	H7	VSS	VSS	VSS								
94	F5	VDD	VDD	VDD								
95	E10	PTB16	LCD_P12/ TSIO_CH9	LCD_P12/ TSIO_CH9	PTB16	SPI1_SOUT	UART0_RX			EWM_IN	LCD_P12	
96	E9	PTB17	LCD_P13/ TSIO_CH10	LCD_P13/ TSIO_CH10	PTB17	SPI1_SIN	UART0_TX			EWM_OUT_b	LCD_P13	
97	D12	PTB18	LCD_P14/ TSIO_CH11	LCD_P14/ TSIO_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_ BCLK		FTM2_QD_ PHA	LCD_P14	
98	D11	PTB19	LCD_P15/ TSIO_CH12	LCD_P15/ TSIO_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS		FTM2_QD_ PHB	LCD_P15	
99	D10	PTB20	LCD_P16	LCD_P16	PTB20	SPI2_PCS0				CMP0_OUT	LCD_P16	

Pinout

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
100	D9	PTB21	LCD_P17	LCD_P17	PTB21	SPI2_SCK				CMP1_OUT	LCD_P17	
101	C12	PTB22	LCD_P18	LCD_P18	PTB22	SPI2_SOUT				CMP2_OUT	LCD_P18	
102	C11	PTB23	LCD_P19	LCD_P19	PTB23	SPI2_SIN	SPI0_PCS5				LCD_P19	
103	B12	PTC0	LCD_P20/ ADC0_SE14/ TSI0_CH13	LCD_P20/ ADC0_SE14/ TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG	I2S0_TXD			LCD_P20	
104	B11	PTC1/ LLWU_P6	LCD_P21/ ADC0_SE15/ TSI0_CH14	LCD_P21/ ADC0_SE15/ TSI0_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_ b	FTM0_CH0			LCD_P21	
105	A12	PTC2	LCD_P22/ ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	LCD_P22/ ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	PTC2	SPI0_PCS2	UART1_CTS_ b	FTM0_CH1			LCD_P22	
106	A11	PTC3/ LLWU_P7	LCD_P23/ CMP1_IN1	LCD_P23/ CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2			LCD_P23	
107	H8	VSS	VSS	VSS								
108	C10	VLL3	VLL3	VLL3								
109	C9	VLL2	VLL2	VLL2								
110	B9	VLL1	VLL1	VLL1								
111	B10	VCAP2	VCAP2	VCAP2								
112	A10	VCAP1	VCAP1	VCAP1								
113	A9	PTC4/ LLWU_P8	LCD_P24	LCD_P24	PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT	LCD_P24	
114	D8	PTC5/ LLWU_P9	LCD_P25	LCD_P25	PTC5/ LLWU_P9	SPI0_SCK		LPT0_ALT2		CMP0_OUT	LCD_P25	
115	C8	PTC6/ LLWU_P10	LCD_P26/ CMP0_IN0	LCD_P26/ CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG				LCD_P26	
116	B8	PTC7	LCD_P27/ CMP0_IN1	LCD_P27/ CMP0_IN1	PTC7	SPI0_SIN					LCD_P27	
117	A8	PTC8	LCD_P28/ ADC1_SE4b/ CMP0_IN2	LCD_P28/ ADC1_SE4b/ CMP0_IN2	PTC8		I2S0_MCLK	I2S0_CLKIN			LCD_P28	
118	D7	PTC9	LCD_P29/ ADC1_SE5b/ CMP0_IN3	LCD_P29/ ADC1_SE5b/ CMP0_IN3	PTC9			I2S0_RX_ BCLK		FTM2_FLT0	LCD_P29	
119	C7	PTC10	LCD_P30/ ADC1_SE6b/ CMP0_IN4	LCD_P30/ ADC1_SE6b/ CMP0_IN4	PTC10	I2C1_SCL		I2S0_RX_FS			LCD_P30	
120	B7	PTC11/ LLWU_P11	LCD_P31/ ADC1_SE7b	LCD_P31/ ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA		I2S0_RXD			LCD_P31	
121	A7	PTC12	LCD_P32	LCD_P32	PTC12		UART4_RTS_ b				LCD_P32	
122	D6	PTC13	LCD_P33	LCD_P33	PTC13		UART4_CTS_ b				LCD_P33	
123	C6	PTC14	LCD_P34	LCD_P34	PTC14		UART4_RX				LCD_P34	
124	B6	PTC15	LCD_P35	LCD_P35	PTC15		UART4_TX				LCD_P35	