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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	16MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	External
Program Memory Type	NVSRAM
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-MQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds5001fp-16

ORDERING INFORMATION

PART	TEMP RANGE	MAX CLOCK SPEED (MHz)	PIN-PACKAGE
DS5001FP-16	0°C to +70°C	16	80 MQFP
DS5001FP-16+	0°C to +70°C	16	80 MQFP
DS5001FP-16N	-40°C to +85°C	16	80 MQFP
DS5001FP-16N+	-40°C to +85°C	16	80 MQFP
DS5001FP-12-44	0°C to +70°C	12	44MQFP
DS5001FP-12-44+	0°C to +70°C	12	44 MQFP

+ *Denotes a Pb-free/RoHS-compliant device.*

DESCRIPTION

The DS5001FP 128k soft microprocessor chip is an 8051-compatible microprocessor based on NV RAM technology and designed for systems that need large quantities of nonvolatile memory. It provides full compatibility with the 8051 instruction set, timers, serial port, and parallel I/O ports. By using NV RAM instead of ROM, the user can program and then reprogram the microprocessor while in-system. The application software can even change its own operation, which allows frequent software upgrades, adaptive programs, customized systems, etc. In addition, by using NV SRAM, the DS5001FP is ideal for data logging applications. It also connects easily to a Dallas real-time clock.

The DS5001FP provides the benefits of NV RAM without using I/O resources. It uses a nonmultiplexed byte-wide address and data bus for memory access. This bus performs all memory access and provides decoded chip enables for SRAM, which leaves the 32 I/O port pins free for application use. The DS5001FP uses ordinary SRAM and battery-backs the memory contents for over 10 years at room temperature with a small external battery. A DS5001FP also provides high-reliability operation in harsh environments. These features include the ability to save the operating state, power-fail reset, power-fail interrupt, and watchdog timer.

A user programs the DS5001FP through its on-chip serial bootstrap loader. The bootstrap loader supervises the loading of software into NV RAM, validates it, and then becomes transparent to the user. Software can be stored in multiple 32kB or one 128kB CMOS SRAM(s). Using its internal partitioning, the DS5001FP can divide a common RAM into user-selectable program and data segments. This partition can be selected at program loading time, but can then be modified later at any time. The microprocessor decodes memory access to the SRAM and addresses memory through its byte-wide bus. Memory portions designated code or ROM are automatically write-protected by the microprocessor. Combining program and data storage in one device saves board space and cost.

The DS5001FP offers several bank switches for access to even more memory. In addition to the primary data area of 64kB, a peripheral selector creates a second 64kB data space with four accompanying chip enables. This area can be used for memory-mapped peripherals or more data storage. The DS5001FP can also use its expanded bus on ports 0 and 2 (like an 8051) to access an additional 64kB of data space. Lastly, the DS5001FP provides one additional bank switch that changes up to 60kB of the NV RAM program space into data memory. Thus, with a small amount of logic, the DS5001 accesses up to 252kB of data memory.

The DS2251T is available (Refer to the data sheet at www.maxim-ic.com/microcontrollers.) for users who want a preconstructed module using the DS5001FP, RAM, lithium cell, and a real-time clock. For more details, refer to the *Secure Microcontroller User's Guide*. For users desiring software security, the DS5002FP is functionally identical to the DS5001FP but provides superior firmware security. The 44-pin version of the device is functionally identical to the 80-pin version but sports a reduced pin count and footprint.

PIN DESCRIPTION

PIN 80 PIN	PIN 44 PIN	NAME	FUNCTION
11, 9, 7, 5, 1, 79, 77, 75	31 (P0.5)	**P0.0–P0.7**	**General-Purpose I/O Port 0.** This port is open-drain and cannot drive a logic 1. It requires external pullups. Port 0 is also the multiplexed expanded address/data bus. When used in this mode, it does not require pullups.
15, 17, 19, 21, 25, 27, 29, 31	44 (P1.3)	**P1.0–P1.7**	**General-Purpose I/O Port 1**
49, 50, 51, 56, 58, 60, 64, 66	—	**P2.0–P2.7**	**General-Purpose I/O Port 2.** Also serves as the MSB of the address in expanded memory accesses, and as pins of the RPC mode when used.
36	8	**P3.0/RXD**	**General-Purpose I/O Port Pin 3.0**. Also serves as the receive signal for the on board UART. This pin should ***not*** be connected directly to a PC COM port.
38	10	**P3.1/TXD**	**General-Purpose I/O Port Pin 3.1.** Also serves as the transmit signal for the on board UART. This pin should ***not*** be connected directly to a PC COM port.
39	—	**P3.2/ $\overline{\text{INT0}}$**	**General-Purpose I/O Port Pin 3.2.** Also serves as the active-low external interrupt 0.
40	11	**P3.3/ $\overline{\text{INT1}}$**	**General-Purpose I/O Port Pin 3.3.** Also serves as the active-low external interrupt 1.
41	—	**P3.4/T0**	**General-Purpose I/O Port Pin 3.4.** Also serves as the timer 0 input.
44	12	**P3.5/T1**	**General-Purpose I/O Port Pin 3.5.** Also serves as the timer 1 input.
45	13	**P3.6/ $\overline{\text{WR}}$**	**General-Purpose I/O Port Pin.** Also serves as the write strobe for expanded bus operation.
46	—	**P3.7/ $\overline{\text{RD}}$**	**General-Purpose I/O Port Pin.** Also serves as the read strobe for expanded bus operation.
68	25	**$\overline{\text{PSEN}}$**	**Program Store Enable.** This active-low signal is used to enable an external program memory when using the expanded bus. It is normally an output and should be unconnected if not used. $\overline{\text{PSEN}}$ also is used to invoke the bootstrap loader. At this time, $\overline{\text{PSEN}}$ is pulled down externally. This should only be done once the DS5001FP is already in a reset state. The device that pulls down should be open drain since it must not interfere with $\overline{\text{PSEN}}$ under normal operation.
34	6	**RST**	**Active-High Reset Input.** A logic 1 applied to this pin will activate a reset state. This pin is pulled down internally so this pin can be left unconnected if not used. An RC power-on reset circuit is not needed and is ***not*** recommended.
70	27	**ALE**	**Address Latch Enable.** Used to demultiplex the multiplexed expanded address/data bus on port 0. This pin is normally connected to the clock input on a ’373 type transparent latch.
47, 48	14, 15	**XTAL2, XTAL1**	**Crystal Connections**. Used to connect an external crystal to the internal oscillator. XTAL1 is the input to an inverting amplifier and XTAL2 is the output.
52	16	**GND**	**Logic Ground**
13	39	**V_{CC}**	**Power Supply, +5V**
12	38	**V_{CCO}**	**V_{CC} Output.** This is switched between V_{CC} and V_{LI} by internal circuits based on the level of V_{CC}. When power is above the lithium input, power will be drawn from V_{CC}. The lithium cell remains isolated from a load. When V_{CC} is below V_{LI}, the V_{CCO} switches to the V_{LI} source. V_{CCO} should be connected to the V_{CC} pin of an SRAM.
54	17	**V_{LI}**	**Lithium Voltage Input.** Connect to a lithium cell greater than V_{LIMIN} and no greater than V_{LImax} as shown in the electrical specifications. Nominal value is +3V.

PIN DESCRIPTION (continued)

PIN		NAME	FUNCTION
80 PIN	44 PIN		
53, 16, 8, 18, 80, 76, 4, 6, 20, 24, 26, 28, 30, 33, 35, 37	41, 36, 42, 32, 30, 34, 35, 43, 1, 2, 3, 4, 5, 7, 9	**BA14–BA0**	**Byte-Wide Address Bus Bits 14–0**. This bus is combined with the nonmultiplexed data bus (BD7–0) to access NV SRAM. Decoding is performed using $\overline{CE1}$ through $\overline{CE4}$. Therefore, BA15 is not actually needed. Read/write access is controlled by R/$\overline{W}$. BA14–0 connect directly to an 8k, 32k, or 128k SRAM. If an 8k RAM is used, BA13 and BA14 are unconnected. If a 128k SRAM is used, the micro converts $\overline{CE2}$ and $\overline{CE3}$ to serve as A16 and A15 respectively.
71, 69, 67, 65, 61, 59, 57, 55	28, 26, 24, 23, 21, 20, 19, 18	**BD7–0**	**Byte-Wide Data Bus Bits 7–0**. This 8-bit, bidirectional bus is combined with the nonmultiplexed address bus (BA14–0) to access NV SRAM. Decoding is performed on $\overline{CE1}$ and $\overline{CE2}$. Read/write access is controlled by R/$\overline{W}$. BD7–0 connect directly to an SRAM, and optionally to a real-time clock or other peripheral.
10	37	**R/$\overline{W}$**	**Read/Write.** This signal provides the write enable to the SRAMs on the byte-wide bus. It is controlled by the memory map and partition. The blocks selected as program (ROM) are write-protected.
74	29	**$\overline{CE1}$**	**Chip Enable 1.** This is the primary decoded chip enable for memory access on the byte-wide bus. It connects to the chip enable input of one SRAM. $\overline{CE1}$ is lithium-backed. It remains in a logic high inactive state when V_{CC} falls below V_{LI}.
72	—	**$\overline{CE1N}$**	**Non-Battery-Backed Version of Chip Enable 1.** This can be used with a 32kB EPROM. It should not be used with a battery-backed chip.
2	33	**$\overline{CE2}$**	**Chip Enable 2.** This chip enable is provided to access a second 32k block of memory. It connects to the chip enable input of one SRAM. When MSEL = 0, the micro converts $\overline{CE2}$ into A16 for a 128k x 8 SRAM. $\overline{CE2}$ is lithium-backed and remains at a logic high when V_{CC} falls below V_{LI}.
63	22	**$\overline{CE3}$**	**Chip Enable 3.** This chip enable is provided to access a third 32k block of memory. It connects to the chip enable input of one SRAM. When MSEL = 0, the micro converts $\overline{CE3}$ into A15 for a 128k x 8 SRAM. $\overline{CE3}$ is lithium-backed and remains at a logic high when V_{CC} falls below V_{LI}.
62	—	**$\overline{CE4}$**	**Chip Enable 4.** This chip enable is provided to access a fourth 32k block of memory. It connects to the chip-enable input of one SRAM. When MSEL = 0, this signal is unused. $\overline{CE4}$ is lithium-backed and remains at a logic high when $V_{CC} < V_{LI}$.
78	—	**$\overline{PE1}$**	**Peripheral Enable 1.** Accesses data memory between addresses 0000h and 3FFFh when the PES bit is set to a logic 1. Commonly used to chip enable a byte-wide real-time clock such as the DS1283. $\overline{PE1}$ is lithium-backed and remains at a logic high when V_{CC} falls below V_{LI}. Connect $\overline{PE1}$ to battery-backed functions only.
3	—	**$\overline{PE2}$**	**Peripheral Enable 2.** Accesses data memory between addresses 4000h and 7FFFh when the PES bit is set to a logic 1. $\overline{PE2}$ is lithium-backed and remains at a logic high when V_{CC} falls below V_{LI}. Connect $\overline{PE2}$ to battery-backed functions only.
22	—	**$\overline{PE3}$**	**Peripheral Enable 3.** Accesses data memory between addresses 8000h and BFFFh when the PES bit is set to a logic 1. $\overline{PE3}$ is not lithium-backed and can be connected to any type of peripheral function. If connected to a battery-backed chip, it needs additional circuitry to maintain the chip enable in an inactive state when $V_{CC} < V_{LI}$.
23	—	**$\overline{PE4}$**	**Peripheral Enable 4.** Accesses data memory between addresses C000h and FFFFh when the PES bit is set to a logic 1. $\overline{PE4}$ is not lithium-backed and can be connected to any type of peripheral function. If connected to a battery-backed chip, it needs additional circuitry to maintain the chip enable in an inactive state when $V_{CC} < V_{LI}$.
32	—	**$\overline{PROG}$**	**Invokes the bootstrap loader on a falling edge.** This signal should be debounced so that only one edge is detected. If connected to ground, the micro enters bootstrap loading on power-up. This signal is pulled up internally.

PIN DESCRIPTION (continued)

PIN		NAME	FUNCTION
80 PIN	44 PIN		
42	—	$\overline{\text{VRST}}$	**This I/O pin (open drain with internal pullup) indicates that the power supply (V_{CC}) has fallen below the V_{CCmin} level and the micro is in a reset state.** When this occurs, the DS5001FP drives this pin to a logic 0. Because the micro is lithium-backed, this signal is guaranteed even when V_{CC} = 0V. Because it is an I/O pin, it also forces a reset if pulled low externally. This allows multiple parts to synchronize their power-down resets.
43	—	$\overline{\text{PF}}$	**This output goes to a logic 0 to indicate that $V_{CC} < V_{LI}$ and the micro has switched to lithium backup.** Because the micro is lithium-backed, this signal is guaranteed even when V_{CC} = 0V. The normal application of this signal is to control lithium-powered current to isolate battery-backed functions from non-battery-backed functions.
14	40	**MSEL**	**Memory Select.** This signal controls the memory size selection. When MSEL = +5V, the DS5001FP expects to use 32k x 8 SRAMs. When MSEL = 0V, the DS5001FP expects to use a 128k x 8 SRAM. MSEL must be connected regardless of partition, mode, etc.
73	—	**N.C.**	**No Connection**

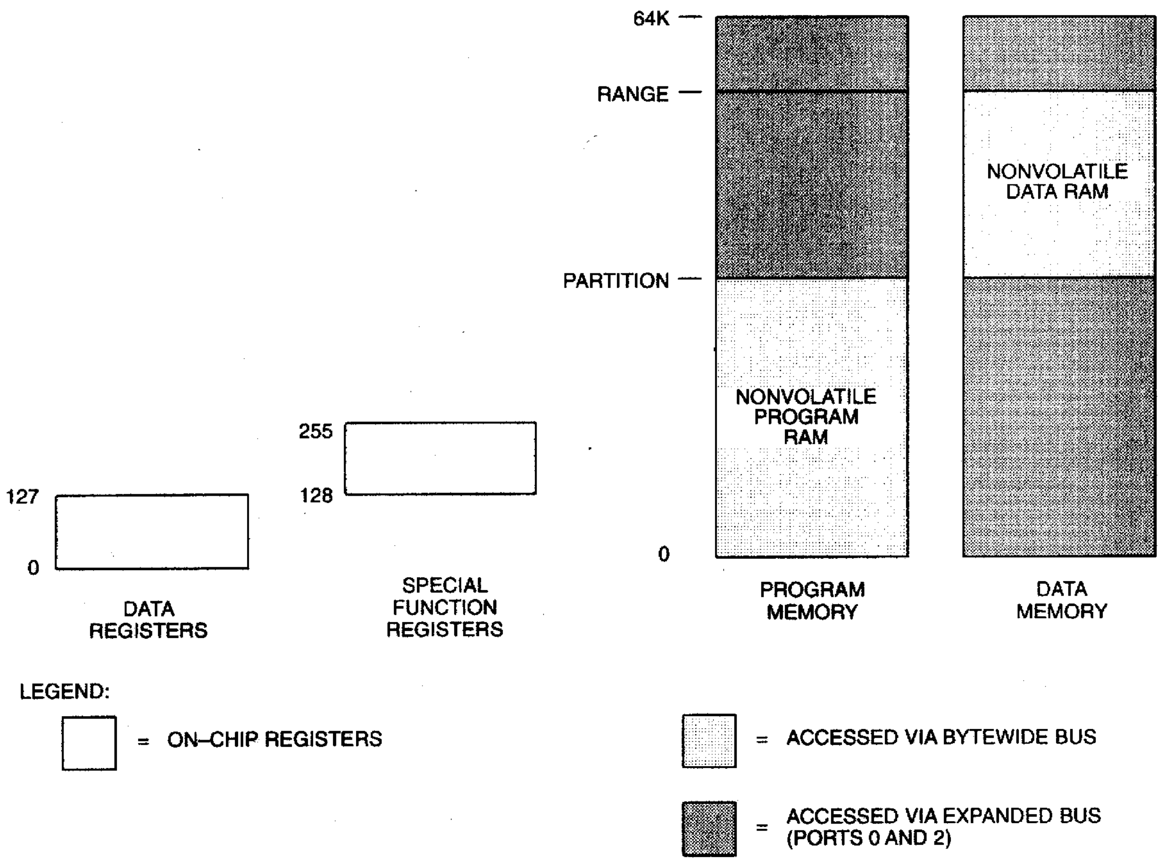
INSTRUCTION SET

The DS5001FP executes an instruction set that is object code-compatible with the industry standard 8051 microcontroller. As a result, software development packages such as assemblers and compilers that have been written for the 8051 are compatible with the DS5001FP. A complete description of the instruction set and operation are provided in the *Secure Microcontroller User's Guide*. Also note that the DS5001FP is embodied in the DS2251T module. The DS2251T combines the DS5001FP with between 32k and 128k of SRAM, a lithium cell, and a real-time clock. This is packaged in a 72-pin SIMM module.

MEMORY ORGANIZATION

Figure 2 illustrates the memory map accessed by the DS5001FP. The entire 64k of program and 64k of data are potentially available to the byte-wide bus. This preserves the I/O ports for application use. The user controls the portion of memory that is actually mapped to the byte-wide bus by selecting the program range and data range. Any area not mapped into the NV RAM is reached by the expanded bus on ports 0 and 2. An alternate configuration allows dynamic partitioning of a 64k space as shown in Figure 3. Selecting PES=1 provides another 64k of potential data storage or memory-mapped peripheral space as shown in Figure 4. These selections are made using special function registers. The memory map and its controls are covered in detail in the *Secure Microcontroller User's Guide*.

Figure 3. MEMORY MAP IN PARTITIONABLE MODE (PM = 0)



NOTE: PARTITIONABLE MODE IS NOT SUPPORTED WHEN MSEL PIN = 0 (128kB MODE).

Figure 4. MEMORY MAP WITH PES = 1

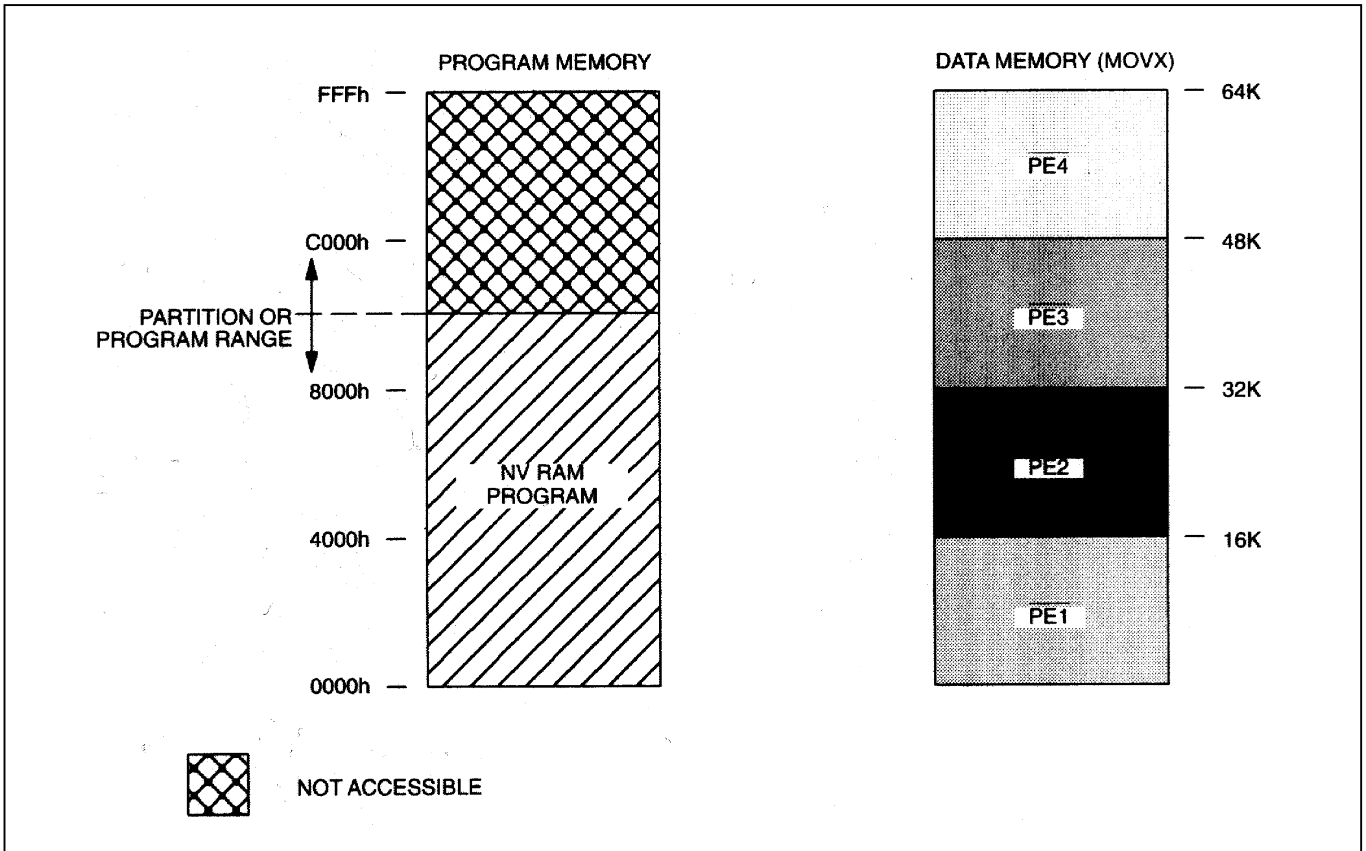


Figure 5 illustrates a typical memory connection for a system using a 128kB SRAM. Note that in this configuration, both program and data are stored in a common RAM chip Figure 6 shows a similar system with using two 32kB SRAMs. The byte-wide address bus connects to the SRAM address lines. The bidirectional byte-wide data bus connects the data I/O lines of the SRAM.

Figure 5. CONNECTION TO 128k x 8 SRAM

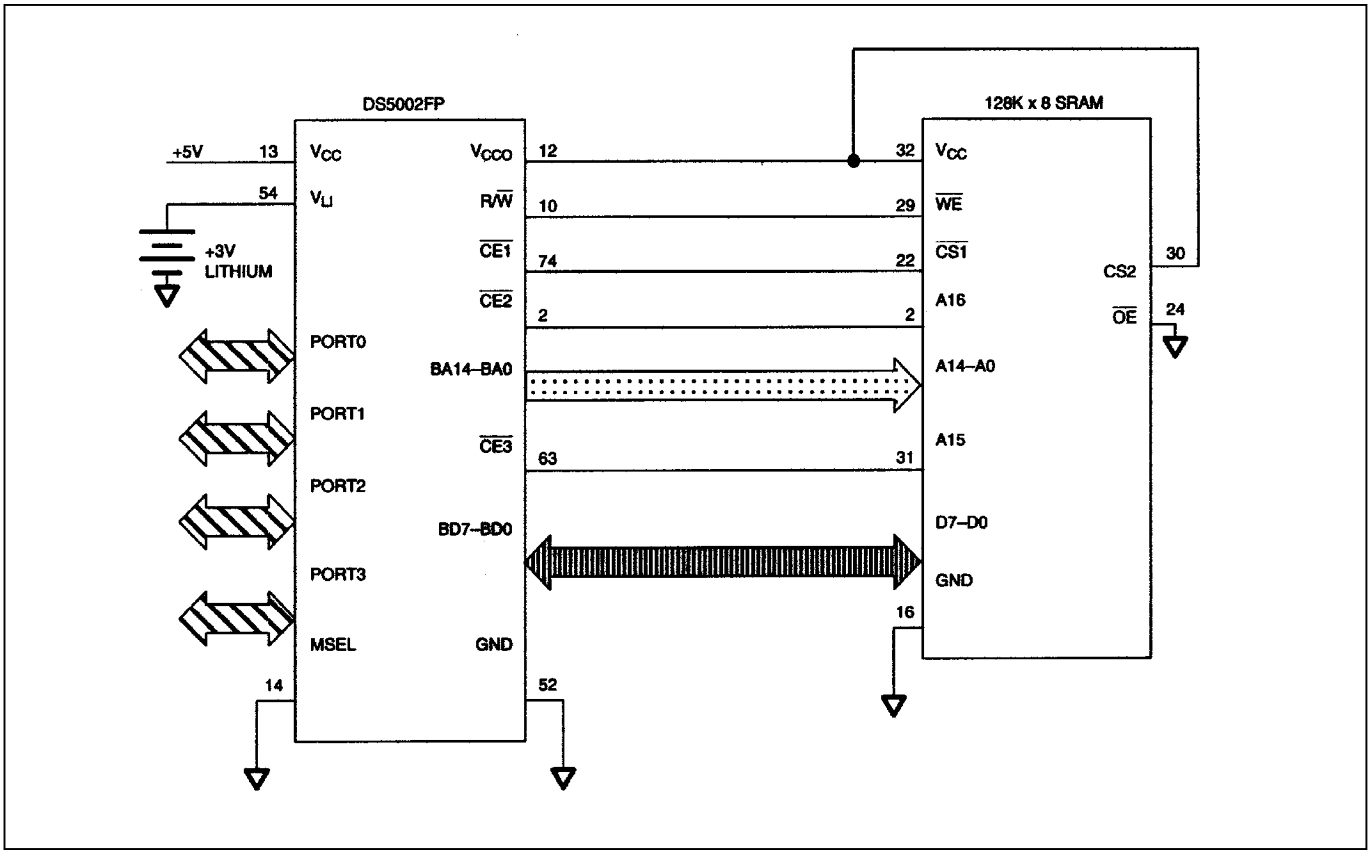
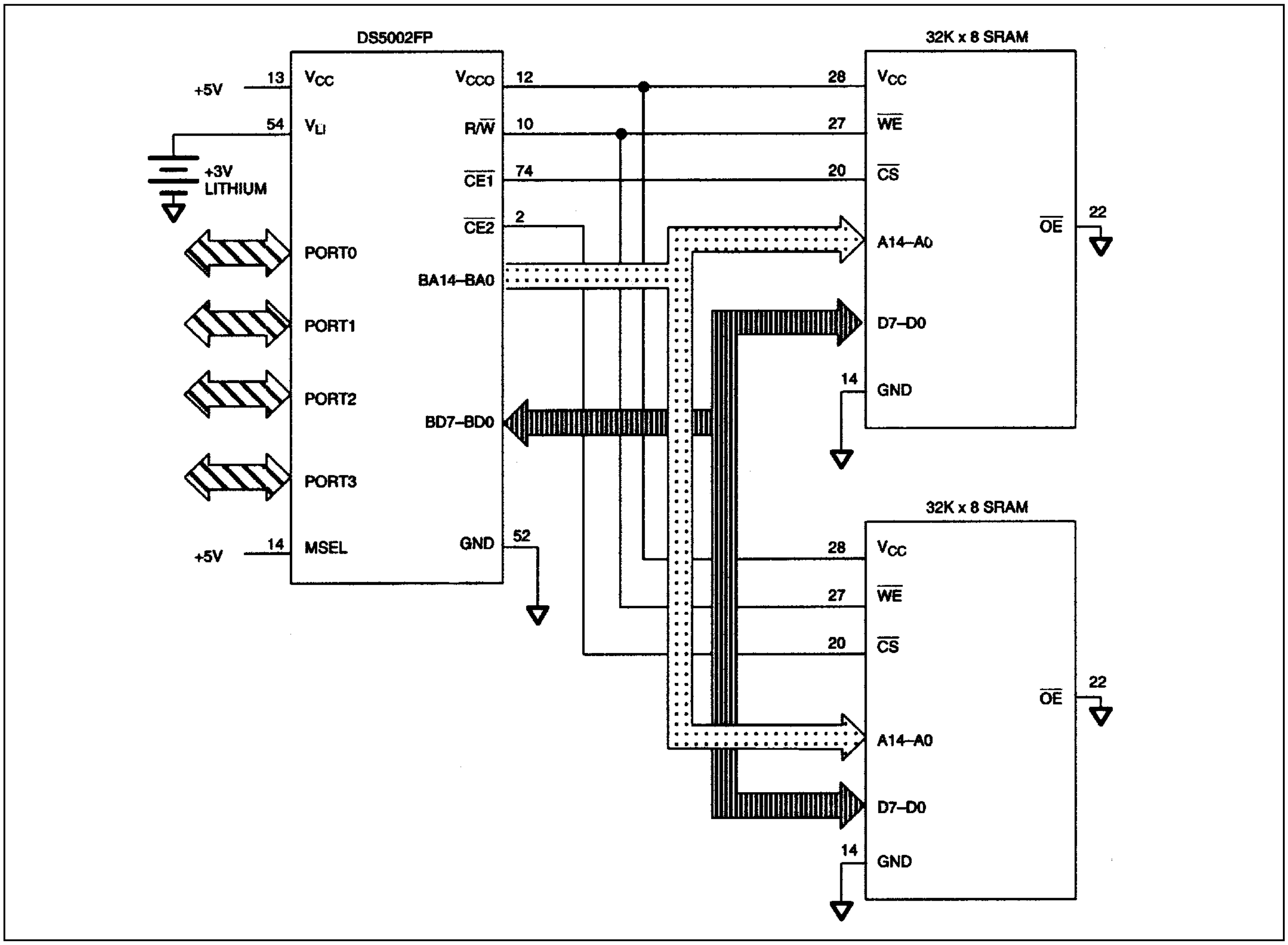


Figure 6. DS5001FP CONNECTION TO 64k x 8 SRAM



POWER MANAGEMENT

The DS5001FP monitors V_{CC} to provide power-fail reset, early warning power-fail interrupt, and switch over to lithium backup. It uses an internal bandgap reference in determining the switch points. These are called V_{PFW}, V_{CCMIN}, and V_{LI}, respectively. When V_{CC} drops below V_{PFW}, the DS5001FP performs an interrupt vector to location 2Bh if the power-fail warning was enabled. Full processor operation continues regardless. When power falls further to V_{CCMIN}, the DS5001FP invokes a reset state. No further code execution is performed unless power rises back above V_{CCMIN}. All decoded chip enables and the $R/\overline{W}$ signal go to an inactive (logic 1) state. V_{CC} is still the power source at this time. When V_{CC} drops further to below V_{LI}, internal circuitry switches to the lithium cell for power. The majority of internal circuits are disabled and the remaining nonvolatile states are retained. Any devices connected V_{CCO} are powered by the lithium cell at this time. V_{CCO} is at the lithium battery voltage minus approximately 0.45V. This drop varies depending on the load. Low power SRAMs should be used for this reason. When using the DS5001FP, the user must select the appropriate battery to match the RAM data retention current and the desired backup lifetime. Note that the lithium cell is only loaded when $V_{CC} < V_{LI}$. The *User's Guide* has more information on this topic. The trip points V_{CCMIN} and V_{PFW} are listed in the *Electrical Specifications* section.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground…………………………..……………………….-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Related to Ground……………………………………………………………-0.3V to 6.0V
Operating Temperature Range…………………………………………………………………...-40°C to +85°C
Storage Temperature Range (Note 1)…………………………………………………………..-55°C to +125°C
Soldering Temperature………………………………………………………See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Note 1: Storage temperature is defined as the temperature of the device when V_{CC} = 0V and V_{LI} = 0V. In this state, the contents of SRAM are not battery-backed and are undefined.

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

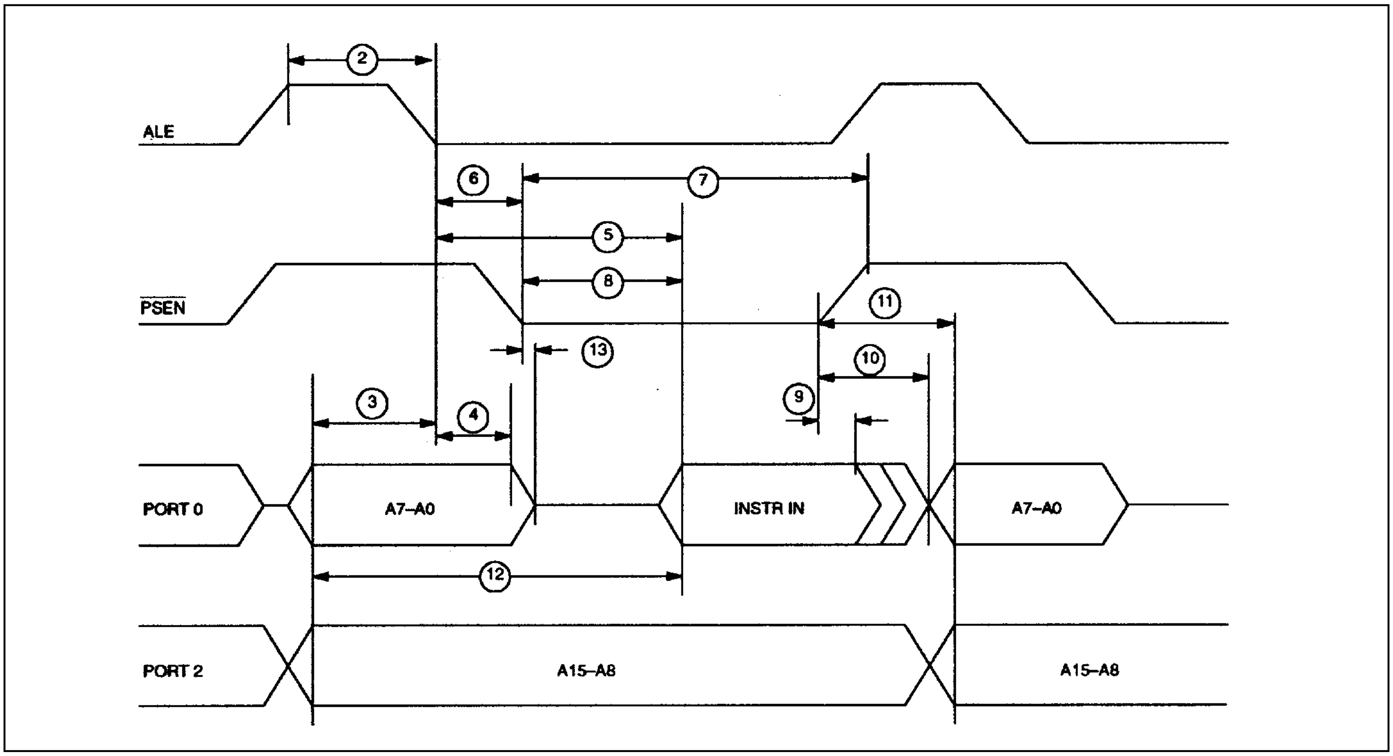
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Low Voltage	V_{IL}	-0.3		+0.8	V	1
Input High Voltage	V_{IH1}	2.0		V_{CC} + 0.3	V	1
Input High Voltage (RST, XTAL1, $\overline{\text{PROG}}$)	V_{IH2}	3.5		V_{CC} + 0.3	V	1
Output Low Voltage at I_{OL} = 1.6mA (Ports 1, 2, 3, $\overline{\text{PF}}$)	V_{OL1}		0.15	0.45	V	1, 11
Output Low Voltage at I_{OL} = 3.2mA (Ports 0, ALE, $\overline{\text{PSEN}}$, BA15–0, BD7–0, R/$\overline{\text{W}}$, $\overline{\text{CE1N}}$, $\overline{\text{CE}}$ 1–4, $\overline{\text{PE}}$ 1–4, V_{RST})	V_{OL2}		0.15	0.45	V	1
Output High Voltage at I_{OH} = -80µA (Ports 1, 2, 3)	V_{OH1}	2.4	4.8		V	1
Output High Voltage at I_{OH} = -400µA (Ports 0, ALE, $\overline{\text{PSEN}}$, $\overline{\text{PF}}$, BA15–0, BD7–0, R/$\overline{\text{W}}$, $\overline{\text{CE1N}}$, $\overline{\text{CE}}$ 1–4, $\overline{\text{PE}}$ 1–4, V_{RST})	V_{OH2}	2.4	4.8		V	1
Input Low Current V_{IN} = 0.45V (Ports 1, 2, 3)	I_{IL}			-50	µA	
Transition Current; 1 to 0 V_{IN} = 2.0V (Ports 1, 2, 3) (0°C to +70°C)	I_{TL}			-500	µA	
Transition Current; 1 to 0 V_{IN} = 2.0V (Ports 1, 2, 3) (-40°C to +85°C)	I_{TL}			-600	µA	10

DC CHARACTERISTICS (continued)

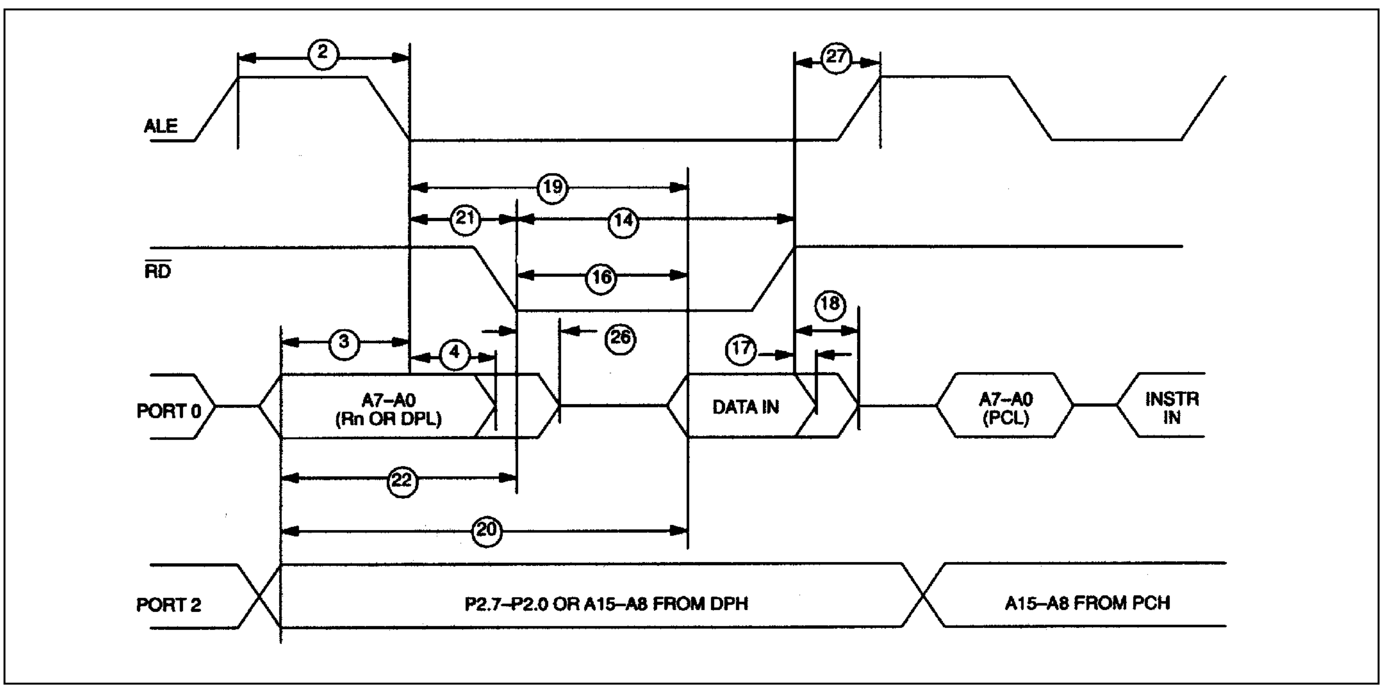
(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current 0.45 < V_{IN} < V_{CC} (Port 0, MSEL)	I_{IL}			+10	µA	
RST Pulldown Resistor (0°C to +70°C)	R_{RE}	40		150	kΩ	
RST Pulldown Resistor (-40°C to +85°C)	R_{RE}	30		180	kΩ	10
$\overline{VRST}$ Pullup Resistor	R_{VR}		4.7		kΩ	
$\overline{PROG}$ Pullup Resistor	R_{PR}		40		kΩ	
Power-Fail Warning Voltage (0°C to +70°C)	V_{PFW}	4.25	4.37	4.50	V	1
Power-Fail Warning Voltage (-40°C to +85°C)	V_{PFW}	4.1	4.37	4.6	V	1, 10
Minimum Operating Voltage (0°C to +70°C)	V_{CCMIN}	4.00	4.12	4.25	V	1
Minimum Operating Voltage (-40°C to +85°C)	V_{CCMIN}	3.85	4.09	4.25	V	1, 10
Operating Voltage	V_{CC}	V_{CCMIN}		5.5	V	1
Lithium Supply Voltage	V_{LI}	2.5		4.0	V	1
Operating Current at 16MHz	I_{CC}			36	mA	2
Idle Mode Current at 12MHz (0°C to +70°C)	I_{IDLE}			7.0	mA	3
Idle Mode Current at 12MHz (-40°C to +85°C)	I_{IDLE}			8.0	mA	3, 10
Stop Mode Current	I_{STOP}			80	µA	4
Pin Capacitance	C_{IN}			10	pF	5
Output Supply Voltage (V_{CCO})	V_{CCO1}	V_{CC} -0.45			V	1, 2
Output Supply Battery-Backed Mode (V_{CCO}, $\overline{CE}$ 1-4, $\overline{PE}$ 1-2) (0°C to +70°C)	V_{CCO2}	V_{LI} -0.65			V	1, 8
Output Supply Battery-Backed Mode (V_{CCO}, $\overline{CE}$ 1-4, $\overline{PE}$ 1-2) (-40°C to +85°C)	V_{CCO2}	V_{LI} -0.9			V	1, 8, 10
Output Supply Current at V_{CCO} = V_{CC} - 0.45V	I_{CCO1}			75	mA	6
Lithium-Backed Quiescent Current (0°C to +70°C)	I_{LI}		5	75	nA	7
Lithium-Backed Quiescent Current (-40°C to +85°C)	I_{LI}		75	500	nA	7
Reset Trip Point in Stop Mode — With BAT = 3.0V (0°C to +70°C)		4.0		4.25		1
Reset Trip Point in Stop Mode — With BAT = 3.0V (-40°C to +85°C)		3.85		4.25		1, 10
Reset Trip Point in Stop Mode — With BAT = 3.0V (0°C to +70°C)		4.4		4.65		1

EXPANDED PROGRAM-MEMORY READ CYCLE



EXPANDED DATA-MEMORY READ CYCLE

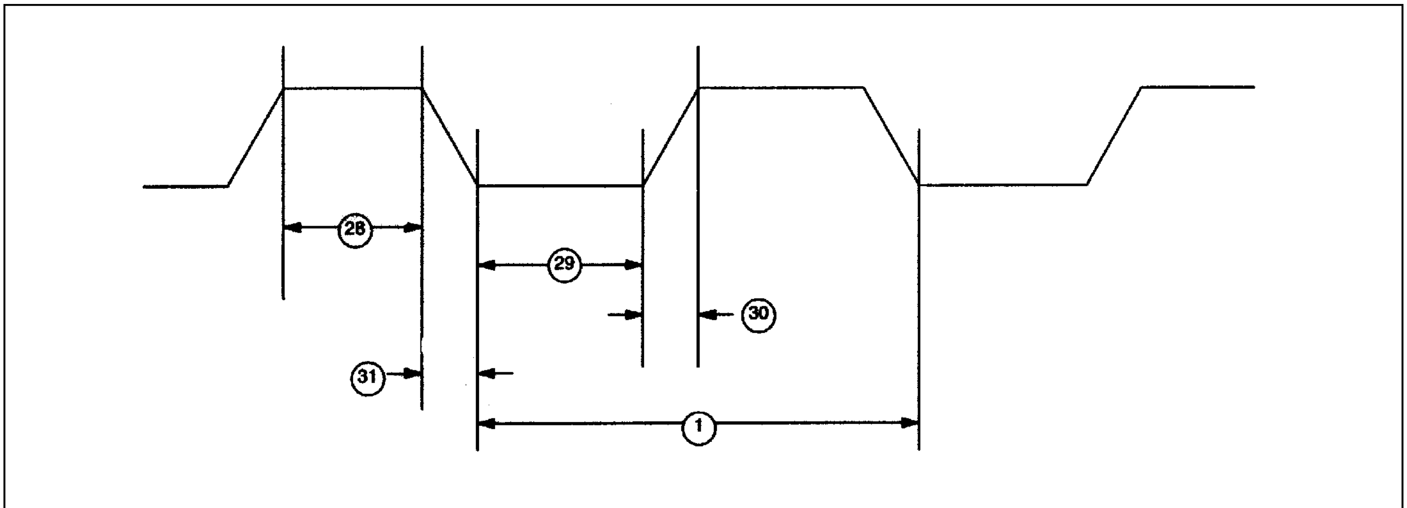


AC CHARACTERISTICS: EXTERNAL CLOCK DRIVE

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

#	PARAMETER		SYMBOL	MIN	MAX	UNITS
28	External Clock-High Time	at 12MHz	t_{CLKHPW}	20		ns
		at 16MHz		15		
29	External Clock-Low Time	at 12MHz	t_{CLKLPW}	20		ns
		at 16MHz		15		
30	External Clock-Rise Time	at 12MHz	t_{CLKR}		20	ns
		at 16MHz			15	
31	External Clock-Fall Time	at 12MHz	t_{CLKF}		20	ns
		at 16MHz			15	

EXTERNAL CLOCK TIMING

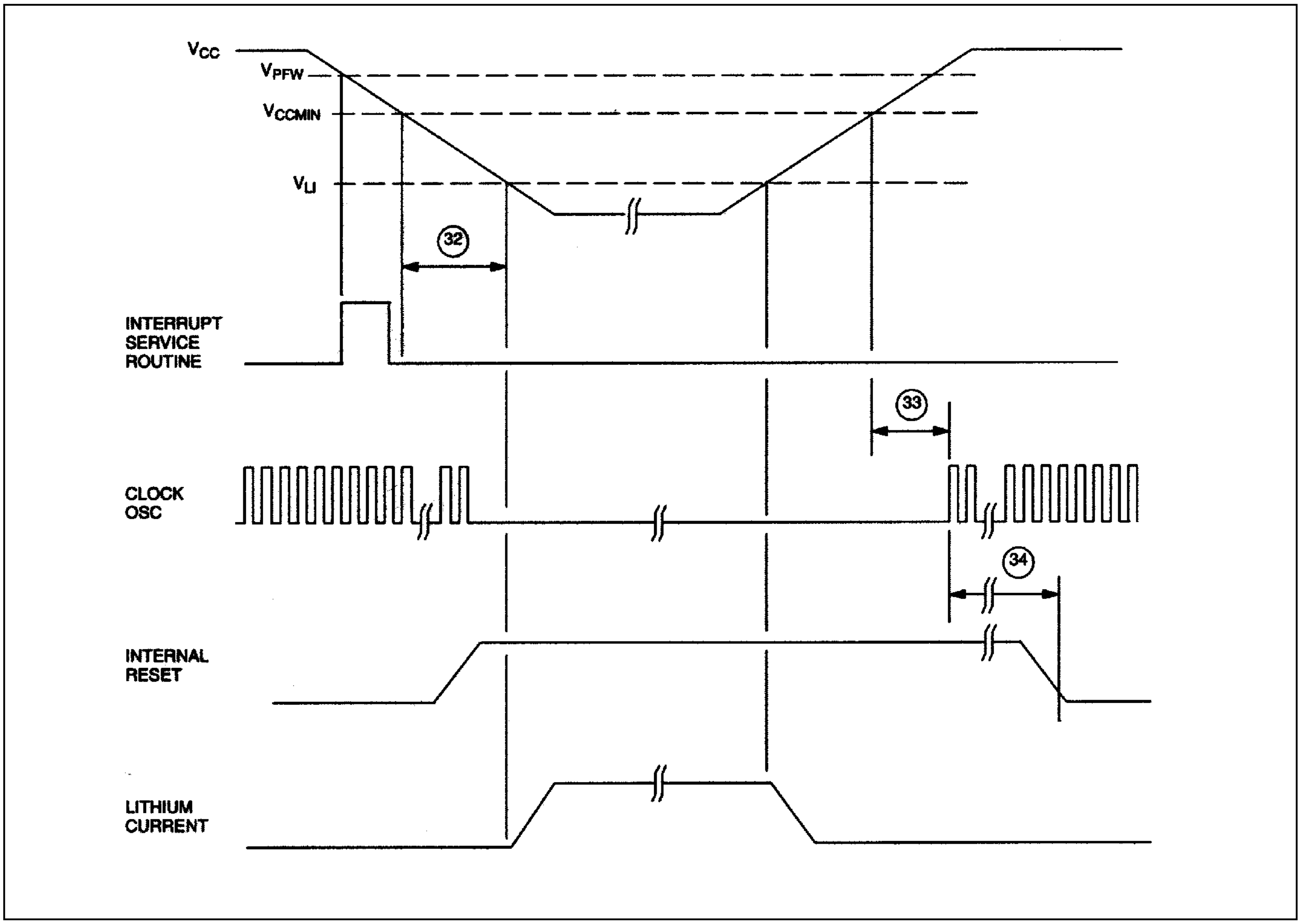


AC CHARACTERISTICS: POWER CYCLE TIME

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
32	Slew Rate from V_{CCMIN} to V_{LI}	t_F	130		µs
33	Crystal Startup Time	t_{CSU}		(Note 9)	
34	Power-On Reset Delay	t_{POR}		21,504	t_{CLK}

POWER CYCLE TIMING

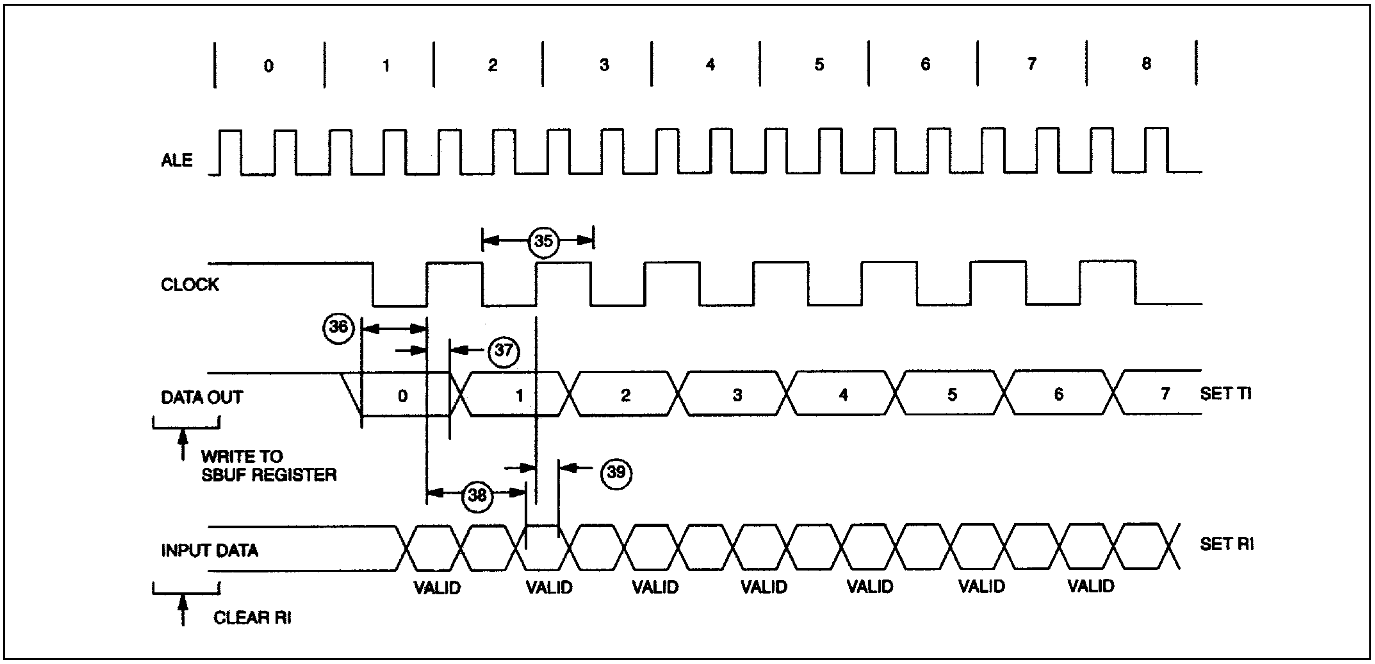


AC CHARACTERISTICS: SERIAL PORT TIMING—MODE 0

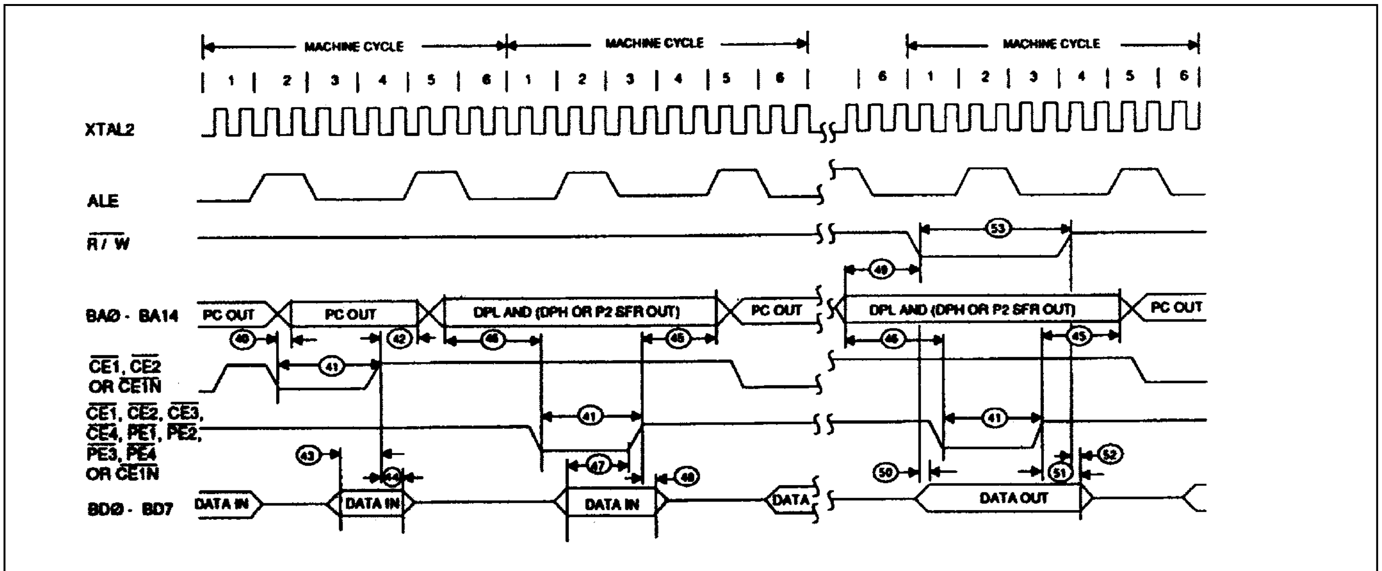
(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
35	Serial-Port Clock-Cycle Time	t_{SPCLK}	$12t_{CLK}$		µs
36	Output-Data Setup to Rising-Clock Edge	t_{DOCH}	$10t_{CLK}$ - 133		ns
37	Output-Data Hold After Rising-Clock Edge	t_{CHDO}	$2t_{CLK}$ - 117		ns
38	Clock-Rising Edge to Input-Data Valid	t_{CHDV}		$10t_{CLK}$ - 133	ns
39	Input-Data Hold After Rising-Clock Edge	t_{CHDIV}	0		ns

SERIAL PORT TIMING—MODE 0



BYTE-WIDE BUS TIMING



RPC AC CHARACTERISTICS: DBB READ

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
54	$\overline{CS}$, A_0 Setup to $\overline{RD}$	t_{AR}	0		ns
55	$\overline{CS}$, A_0 Hold After $\overline{RD}$	t_{RA}	0		ns
56	$\overline{RD}$ Pulse Width	t_{RR}	160		ns
57	$\overline{CS}$, A_0 to Data-Out Delay	t_{AD}		130	ns
58	$\overline{RD}$ to Data-Out Delay	t_{RD}	0	130	ns
59	$\overline{RD}$ to Data-Float Delay	t_{RDZ}		85	ns

RPC AC CHARACTERISTICS: DBB WRITE

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
60	$\overline{CS}$, A_0 Setup to $\overline{WR}$	t_{AW}	0		ns
61A	$\overline{CS}$, Hold After $\overline{WR}$	t_{WA}	0		ns
61B	A_0, Hold After $\overline{WR}$	t_{WA}	20		ns
62	$\overline{WR}$ Pulse Width	t_{WW}	160		ns
63	Data Setup to $\overline{WR}$	t_{DW}	130		ns
64	Data Hold After $\overline{WR}$	t_{WD}	20		ns

AC CHARACTERISTICS: DMA

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
65	$\overline{\text{DACK}}$ to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t_{ACC}	0		ns
66	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ to $\overline{\text{DACK}}$	t_{CAC}	0		ns
67	$\overline{\text{DACK}}$ to Data Valid	t_{ACD}	0	130	ns
68	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ to DRQ Cleared	t_{CRQ}		110	ns

AC CHARACTERISTICS: $\overline{\text{PROG}}$

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
69	$\overline{\text{PROG}}$ Low to Active	t_{PRA}	48		CLKS
70	$\overline{\text{PROG}}$ High to Inactive	t_{PRI}	48		CLKS

NOTES:

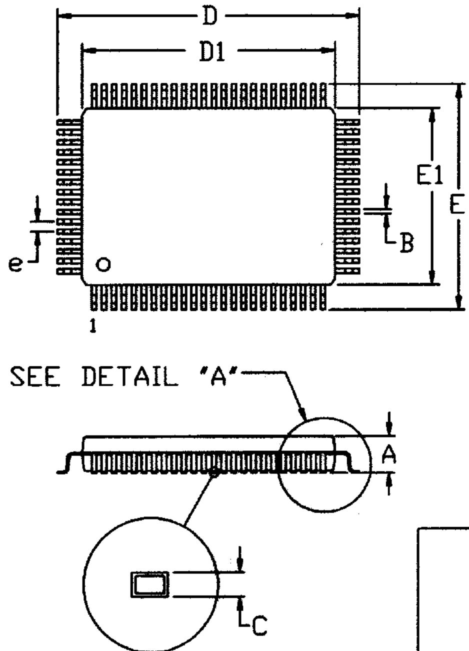
All parameters apply to both commercial and industrial temperature operation unless otherwise noted.

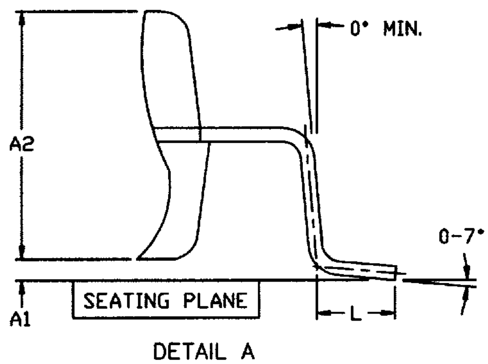
1) All voltages are referenced to ground.
2) Maximum operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF} = 10ns, V_{IL} = 0.5V; XTAL2 disconnected; RST = PORT0 = V_{CC}, MSEL = V_{SS}.
3) Idle mode, I_{IDLE}, is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF} = 10ns, V_{IL} = 0.5V; XTAL2 disconnected; PORT0 = V_{CC}, RST = MSEL = V_{SS}.
4) Stop mode, I_{STOP}, is measured with all output pins disconnected; PORT0 = V_{CC}; XTAL2 not connected; RST = MSEL = XTAL1 = V_{SS}.
5) Pin capacitance is measured with a test frequency: 1MHz, T_A = +25°C.
6) I_{CCO1} is the maximum average operating current that can be drawn from V_{CCO} in normal operation.
7) I_{LI} is the current drawn from V_{LI} input when V_{CC} = 0V and V_{CCO} is disconnected.
8) V_{CCO2} is measured with $V_{CC} < V_{LI}$, and a maximum load of 10µA on V_{CCO}.
9) Crystal startup time is the time required to get the mass of the crystal into vibrational motion from the time that power is first applied to the circuit until the first clock pulse is produced by the on-chip oscillator. The user should check with the crystal vendor for a worst-case specification on this time.
10) This parameter applies to industrial temperature operation.
11) $\overline{PF}$ pin operation is specified with $V_{BAT} \geq 3.0V$.

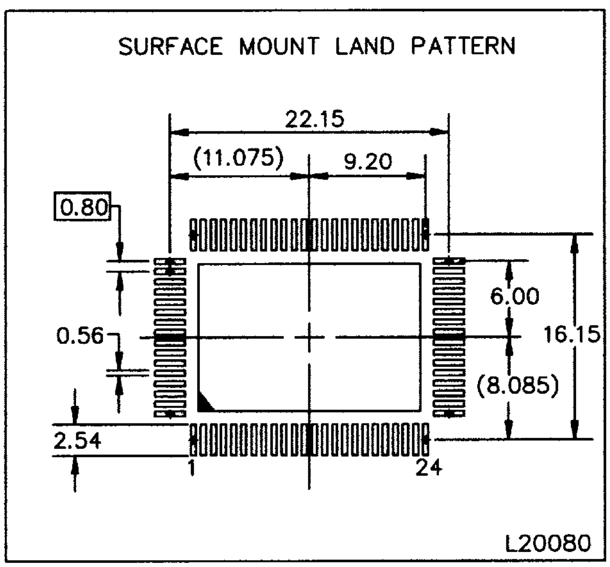
PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/DallasPackInfo.)

80-PIN MQFP



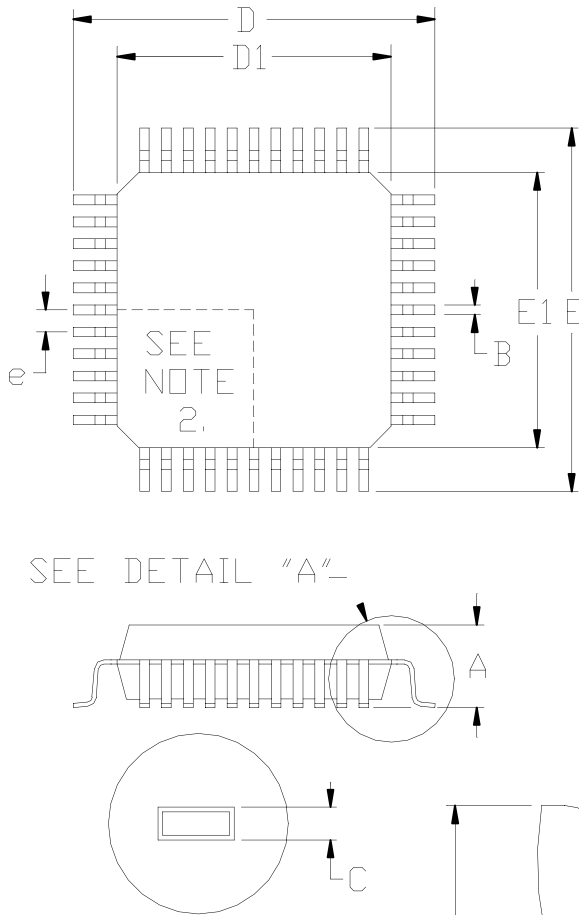




DIM	MM	
	MIN	MAX
A	-	3.40
A1	0.25	-
A2	2.55	2.87
B	0.30	0.50
C	0.13	0.23
D	23.70	24.10
D1	19.90	20.10
E	17.70	18.10
E1	13.90	14.10
e	0.80 BSC	
L	0.65	0.95

56-G4005-001

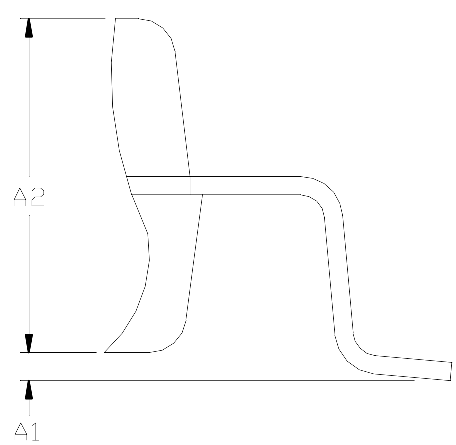
44-PIN MQFP



NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIED ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSION; ±D ON LOWER

DIM	MIN	MAX
A	—	2.45
A1	0.10	0.30
A2	1.95	2.10
D	13.65	14.30
D1	9.90	10.10
E	13.65	14.30
E1	9.90	10.10
L	0.63	1.03
e	0.80 BSC	
B	0.30	0.45
C	0.13	0.23



DETAIL A

DIMENSIONS ARE IN MILLIMETERS

REVISION HISTORY

The following represent the key differences between the 112795 and 073096 version of the DS5001FP data sheet. Please review this summary carefully.

1) Change V_{CC02} specification from V_{LI} - 0.5 to V_{LI} - 0.65 (PCN F62501).
2) Update mechanical specifications.

The following represent the key differences between the 073096 and 111996 version of the DS5001FP data sheet. Please review this summary carefully.

1) Change V_{CC01} from V_{CC} - 0.3 to V_{CC} - 0.35.

The following represent the key differences between the 111996 and 061297 version of the DS5001FP data sheet. Please review this summary carefully.

1) $\overline{PF}$ signal moved from V_{OL2} test specification to V_{OL1}. PCN No. (D72502)
2) AC characteristics for battery-backed SDI pulse specification added.

The following represent the key differences between the 061297 and 051099 version of the DS5001FP data sheet. Please review this summary carefully.

1) Reduced absolute maximum voltage to V_{CC} + 0.5V.
2) Added note clarifying storage temperature specification is for non-battery-backed state.
3) Changed R_{RE} min (industrial temp range) from 40kΩ to 30kΩ.
4) Changed V_{PFW} max (industrial temp range) from 4.5V to 4.6V.
5) Added industrial specification for I_{LI}.
6) Reduced t_{CE1HOV} and t_{CEHDV} from 10ns to 0ns.

The following represent the key differences between the 051099 and 052499 version of the DS5001FP data sheet. Please review this summary carefully.

1) Minor markups and ready for approval.

The following represent the key differences between the 052499 and 052302 version of the DS5001FP data sheet. Please review this summary carefully.

1) Added information relating to 44-pin package.
2) Updated V_{CCO1} and I_{CCO1} specifications to reflect 0.45V internal voltage drop instead of 0.35V.

The following represent the key differences between the 052302 and 070605 version of the DS5001FP data sheet. Please review this summary carefully.

1) Added Pb-free part to Ordering Information table.
2) Added operating voltage specification. (This is not a new specification because operating voltage is implied in the testing limits, but rather a clarification.)
3) Updated Absolute Maximum Ratings soldering temperature to reference JEDEC standard.

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