Analog Devices Inc./Maxim Integrated - DS5001FP-16N+ Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	16MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	External
Program Memory Type	NVSRAM
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-MQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds5001fp-16n

ORDERING INFORMATION

PART	TEMP RANGE	MAX CLOCK SPEED (MHz)	PIN-PACKAGE
DS5001FP-16	0°C to +70°C	16	80 MQFP
DS5001FP-16+	0°C to +70°C	16	80 MQFP
DS5001FP-16N	-40°C to +85°C	16	80 MQFP
DS5001FP-16N+	-40°C to +85°C	16	80 MQFP
DS5001FP-12-44	0°C to +70°C	12	44MQFP
DS5001FP-12-44+	0°C to +70°C	12	44 MQFP

+ *Denotes a Pb-free/RoHS-compliant device.*

DESCRIPTION

The DS5001FP 128k soft microprocessor chip is an 8051-compatible microprocessor based on NV RAM technology and designed for systems that need large quantities of nonvolatile memory. It provides full compatibility with the 8051 instruction set, timers, serial port, and parallel I/O ports. By using NV RAM instead of ROM, the user can program and then reprogram the microprocessor while in-system. The application software can even change its own operation, which allows frequent software upgrades, adaptive programs, customized systems, etc. In addition, by using NV SRAM, the DS5001FP is ideal for data logging applications. It also connects easily to a Dallas real-time clock.

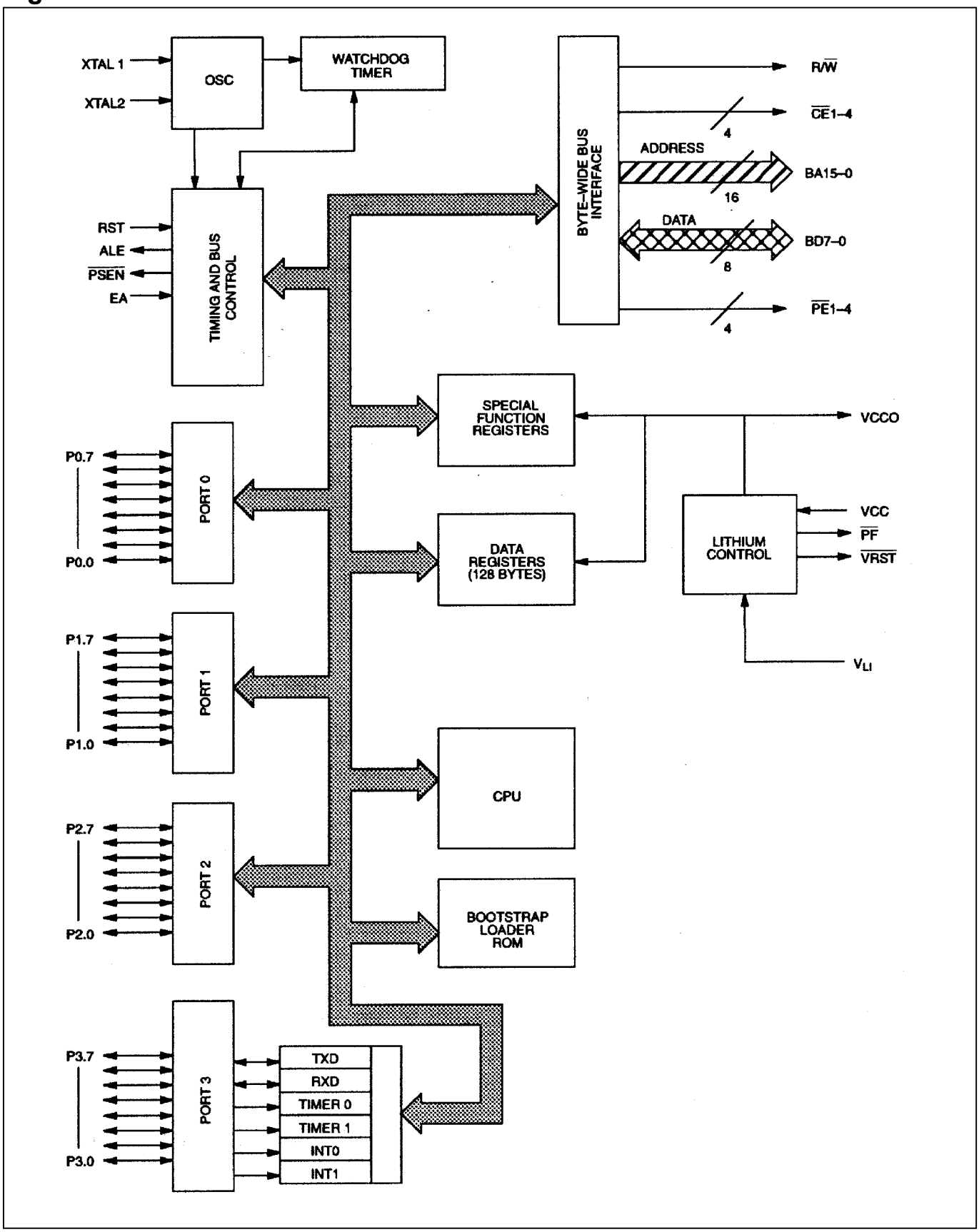
The DS5001FP provides the benefits of NV RAM without using I/O resources. It uses a nonmultiplexed byte-wide address and data bus for memory access. This bus performs all memory access and provides decoded chip enables for SRAM, which leaves the 32 I/O port pins free for application use. The DS5001FP uses ordinary SRAM and battery-backs the memory contents for over 10 years at room temperature with a small external battery. A DS5001FP also provides high-reliability operation in harsh environments. These features include the ability to save the operating state, power-fail reset, power-fail interrupt, and watchdog timer.

A user programs the DS5001FP through its on-chip serial bootstrap loader. The bootstrap loader supervises the loading of software into NV RAM, validates it, and then becomes transparent to the user. Software can be stored in multiple 32kB or one 128kB CMOS SRAM(s). Using its internal partitioning, the DS5001FP can divide a common RAM into user-selectable program and data segments. This partition can be selected at program loading time, but can then be modified later at any time. The microprocessor decodes memory access to the SRAM and addresses memory through its byte-wide bus. Memory portions designated code or ROM are automatically write-protected by the microprocessor. Combining program and data storage in one device saves board space and cost.

The DS5001FP offers several bank switches for access to even more memory. In addition to the primary data area of 64kB, a peripheral selector creates a second 64kB data space with four accompanying chip enables. This area can be used for memory-mapped peripherals or more data storage. The DS5001FP can also use its expanded bus on ports 0 and 2 (like an 8051) to access an additional 64kB of data space. Lastly, the DS5001FP provides one additional bank switch that changes up to 60kB of the NV RAM program space into data memory. Thus, with a small amount of logic, the DS5001 accesses up to 252kB of data memory.

The DS2251T is available (Refer to the data sheet at www.maxim-ic.com/microcontrollers.) for users who want a preconstructed module using the DS5001FP, RAM, lithium cell, and a real-time clock. For more details, refer to the *Secure Microcontroller User's Guide*. For users desiring software security, the DS5002FP is functionally identical to the DS5001FP but provides superior firmware security. The 44-pin version of the device is functionally identical to the 80-pin version but sports a reduced pin count and footprint.

Figure 1. BLOCK DIAGRAM



PIN DESCRIPTION (continued)

PIN		NAME	FUNCTION
80 PIN	44 PIN		
53, 16, 8, 18, 80, 76, 4, 6, 20, 24, 26, 28, 30, 33, 35, 37	41, 36, 42, 32, 30, 34, 35, 43, 1, 2, 3, 4, 5, 7, 9	**BA14–BA0**	**Byte-Wide Address Bus Bits 14–0**. This bus is combined with the nonmultiplexed data bus (BD7–0) to access NV SRAM. Decoding is performed using $\overline{CE1}$ through $\overline{CE4}$. Therefore, BA15 is not actually needed. Read/write access is controlled by R/$\overline{W}$. BA14–0 connect directly to an 8k, 32k, or 128k SRAM. If an 8k RAM is used, BA13 and BA14 are unconnected. If a 128k SRAM is used, the micro converts $\overline{CE2}$ and $\overline{CE3}$ to serve as A16 and A15 respectively.
71, 69, 67, 65, 61, 59, 57, 55	28, 26, 24, 23, 21, 20, 19, 18	**BD7–0**	**Byte-Wide Data Bus Bits 7–0**. This 8-bit, bidirectional bus is combined with the nonmultiplexed address bus (BA14–0) to access NV SRAM. Decoding is performed on $\overline{CE1}$ and $\overline{CE2}$. Read/write access is controlled by R/$\overline{W}$. BD7–0 connect directly to an SRAM, and optionally to a real-time clock or other peripheral.
10	37	**R/$\overline{W}$**	**Read/Write.** This signal provides the write enable to the SRAMs on the byte-wide bus. It is controlled by the memory map and partition. The blocks selected as program (ROM) are write-protected.
74	29	**$\overline{CE1}$**	**Chip Enable 1.** This is the primary decoded chip enable for memory access on the byte-wide bus. It connects to the chip enable input of one SRAM. $\overline{CE1}$ is lithium-backed. It remains in a logic high inactive state when V_{CC} falls below V_{LI}.
72	—	**$\overline{CE1N}$**	**Non-Battery-Backed Version of Chip Enable 1.** This can be used with a 32kB EPROM. It should not be used with a battery-backed chip.
2	33	**$\overline{CE2}$**	**Chip Enable 2.** This chip enable is provided to access a second 32k block of memory. It connects to the chip enable input of one SRAM. When MSEL = 0, the micro converts $\overline{CE2}$ into A16 for a 128k x 8 SRAM. $\overline{CE2}$ is lithium-backed and remains at a logic high when V_{CC} falls below V_{LI}.
63	22	**$\overline{CE3}$**	**Chip Enable 3.** This chip enable is provided to access a third 32k block of memory. It connects to the chip enable input of one SRAM. When MSEL = 0, the micro converts $\overline{CE3}$ into A15 for a 128k x 8 SRAM. $\overline{CE3}$ is lithium-backed and remains at a logic high when V_{CC} falls below V_{LI}.
62	—	**$\overline{CE4}$**	**Chip Enable 4.** This chip enable is provided to access a fourth 32k block of memory. It connects to the chip-enable input of one SRAM. When MSEL = 0, this signal is unused. $\overline{CE4}$ is lithium-backed and remains at a logic high when $V_{CC} < V_{LI}$.
78	—	**$\overline{PE1}$**	**Peripheral Enable 1.** Accesses data memory between addresses 0000h and 3FFFh when the PES bit is set to a logic 1. Commonly used to chip enable a byte-wide real-time clock such as the DS1283. $\overline{PE1}$ is lithium-backed and remains at a logic high when V_{CC} falls below V_{LI}. Connect $\overline{PE1}$ to battery-backed functions only.
3	—	**$\overline{PE2}$**	**Peripheral Enable 2.** Accesses data memory between addresses 4000h and 7FFFh when the PES bit is set to a logic 1. $\overline{PE2}$ is lithium-backed and remains at a logic high when V_{CC} falls below V_{LI}. Connect $\overline{PE2}$ to battery-backed functions only.
22	—	**$\overline{PE3}$**	**Peripheral Enable 3.** Accesses data memory between addresses 8000h and BFFFh when the PES bit is set to a logic 1. $\overline{PE3}$ is not lithium-backed and can be connected to any type of peripheral function. If connected to a battery-backed chip, it needs additional circuitry to maintain the chip enable in an inactive state when $V_{CC} < V_{LI}$.
23	—	**$\overline{PE4}$**	**Peripheral Enable 4.** Accesses data memory between addresses C000h and FFFFh when the PES bit is set to a logic 1. $\overline{PE4}$ is not lithium-backed and can be connected to any type of peripheral function. If connected to a battery-backed chip, it needs additional circuitry to maintain the chip enable in an inactive state when $V_{CC} < V_{LI}$.
32	—	**$\overline{PROG}$**	**Invokes the bootstrap loader on a falling edge.** This signal should be debounced so that only one edge is detected. If connected to ground, the micro enters bootstrap loading on power-up. This signal is pulled up internally.

PIN DESCRIPTION (continued)

PIN		NAME	FUNCTION
80 PIN	44 PIN		
42	—	$\overline{\text{VRST}}$	**This I/O pin (open drain with internal pullup) indicates that the power supply (V_{CC}) has fallen below the V_{CCmin} level and the micro is in a reset state.** When this occurs, the DS5001FP drives this pin to a logic 0. Because the micro is lithium-backed, this signal is guaranteed even when V_{CC} = 0V. Because it is an I/O pin, it also forces a reset if pulled low externally. This allows multiple parts to synchronize their power-down resets.
43	—	$\overline{\text{PF}}$	**This output goes to a logic 0 to indicate that $V_{CC} < V_{LI}$ and the micro has switched to lithium backup.** Because the micro is lithium-backed, this signal is guaranteed even when V_{CC} = 0V. The normal application of this signal is to control lithium-powered current to isolate battery-backed functions from non-battery-backed functions.
14	40	**MSEL**	**Memory Select.** This signal controls the memory size selection. When MSEL = +5V, the DS5001FP expects to use 32k x 8 SRAMs. When MSEL = 0V, the DS5001FP expects to use a 128k x 8 SRAM. MSEL must be connected regardless of partition, mode, etc.
73	—	**N.C.**	**No Connection**

INSTRUCTION SET

The DS5001FP executes an instruction set that is object code-compatible with the industry standard 8051 microcontroller. As a result, software development packages such as assemblers and compilers that have been written for the 8051 are compatible with the DS5001FP. A complete description of the instruction set and operation are provided in the *Secure Microcontroller User's Guide*. Also note that the DS5001FP is embodied in the DS2251T module. The DS2251T combines the DS5001FP with between 32k and 128k of SRAM, a lithium cell, and a real-time clock. This is packaged in a 72-pin SIMM module.

MEMORY ORGANIZATION

Figure 2 illustrates the memory map accessed by the DS5001FP. The entire 64k of program and 64k of data are potentially available to the byte-wide bus. This preserves the I/O ports for application use. The user controls the portion of memory that is actually mapped to the byte-wide bus by selecting the program range and data range. Any area not mapped into the NV RAM is reached by the expanded bus on ports 0 and 2. An alternate configuration allows dynamic partitioning of a 64k space as shown in Figure 3. Selecting PES=1 provides another 64k of potential data storage or memory-mapped peripheral space as shown in Figure 4. These selections are made using special function registers. The memory map and its controls are covered in detail in the *Secure Microcontroller User's Guide*.

Figure 2. MEMORY MAP IN NONPARTITIONABLE MODE (PM = 1)

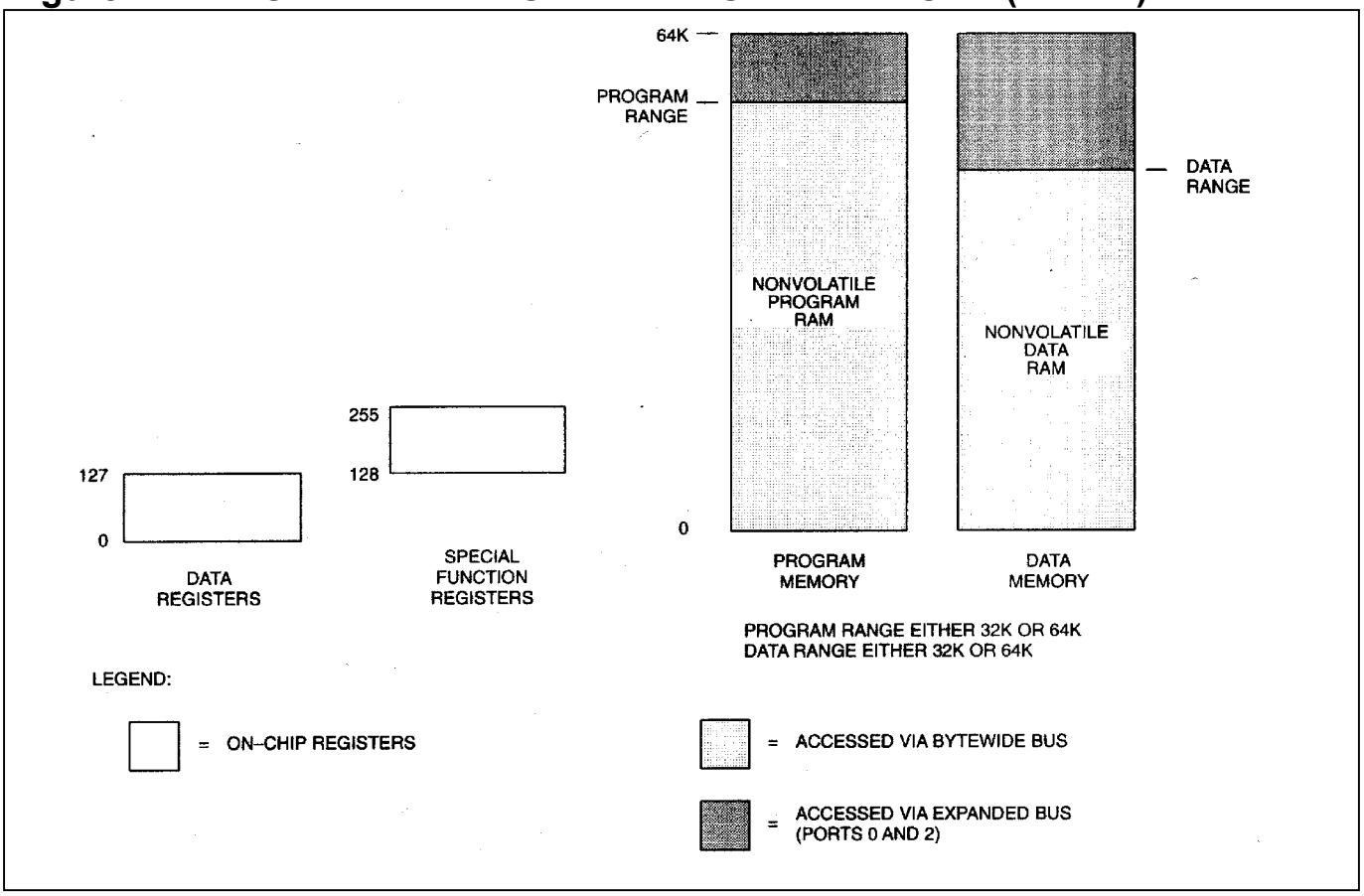
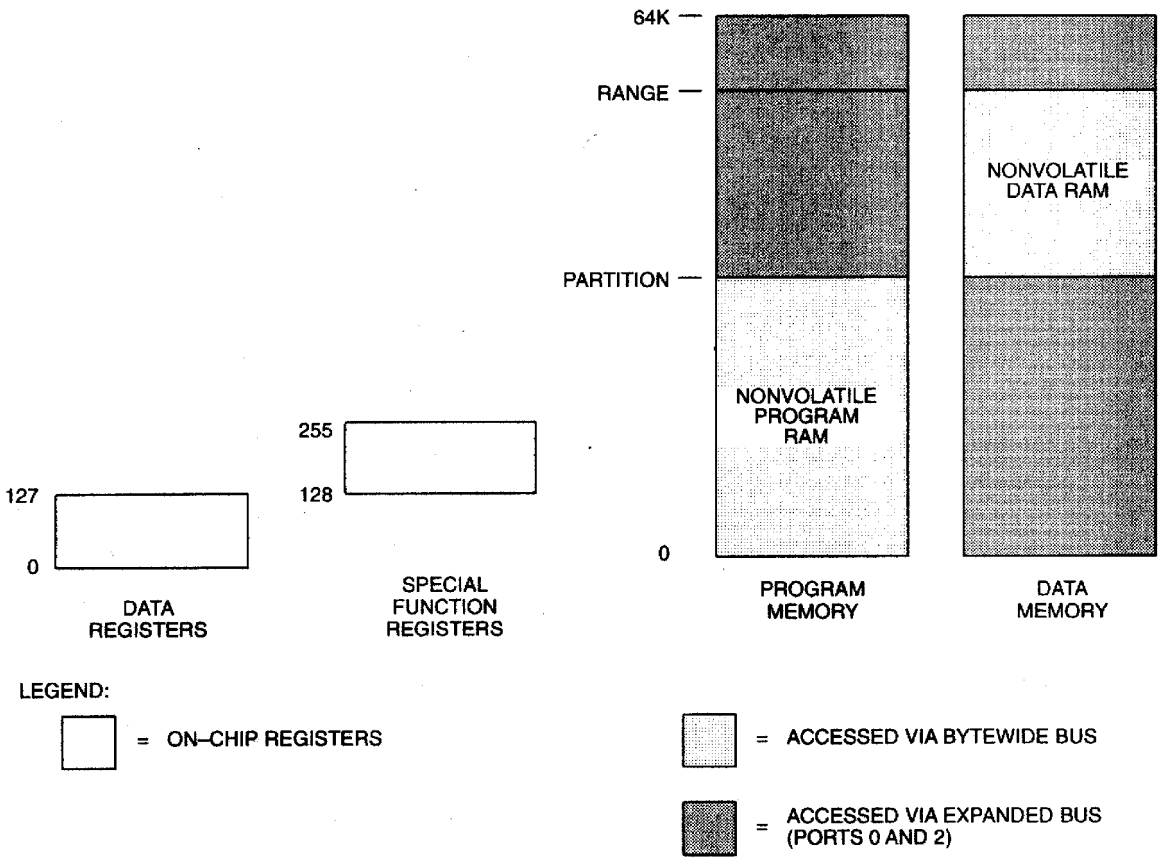


Figure 3. MEMORY MAP IN PARTITIONABLE MODE (PM = 0)



NOTE: PARTITIONABLE MODE IS NOT SUPPORTED WHEN MSEL PIN = 0 (128kB MODE).

Figure 4. MEMORY MAP WITH PES = 1

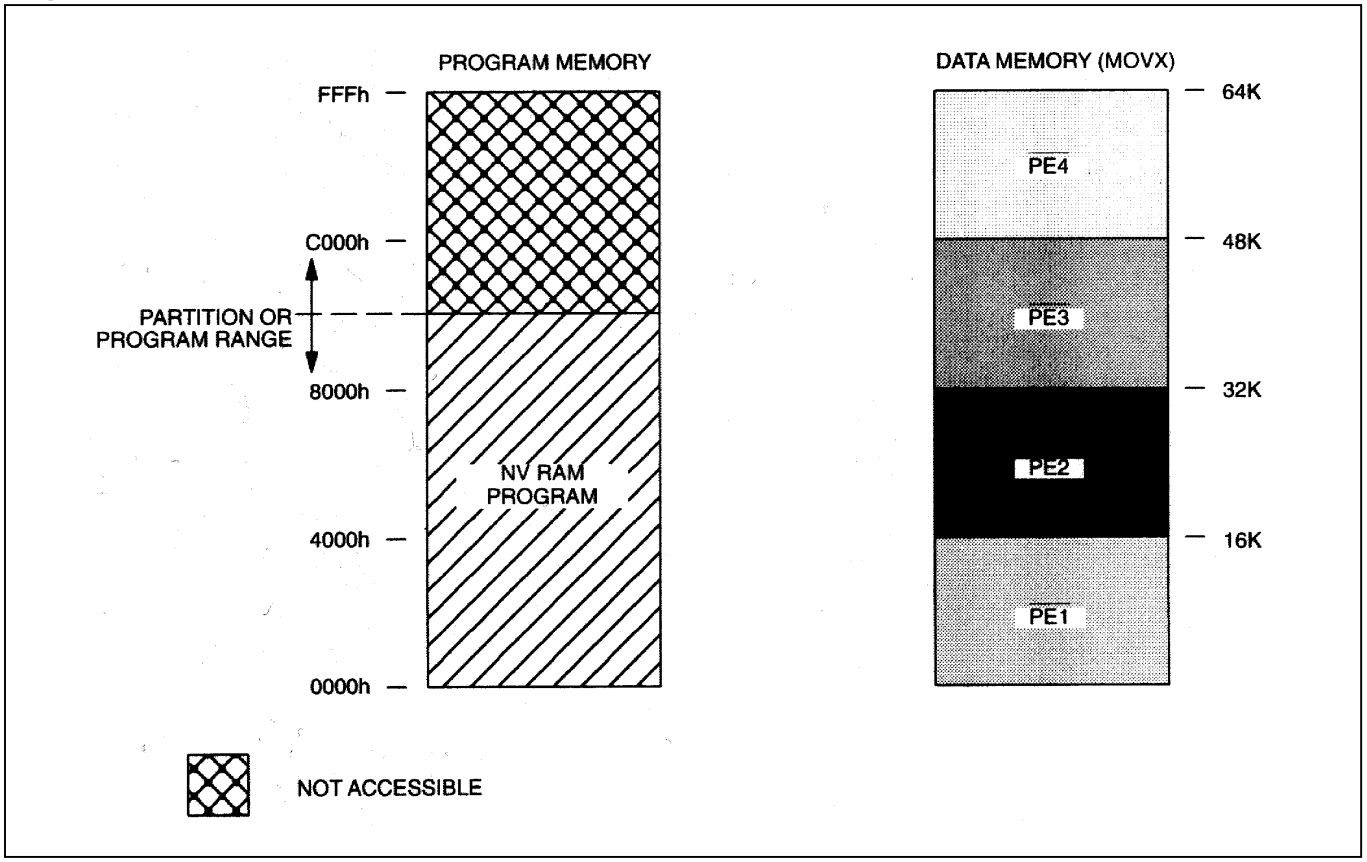
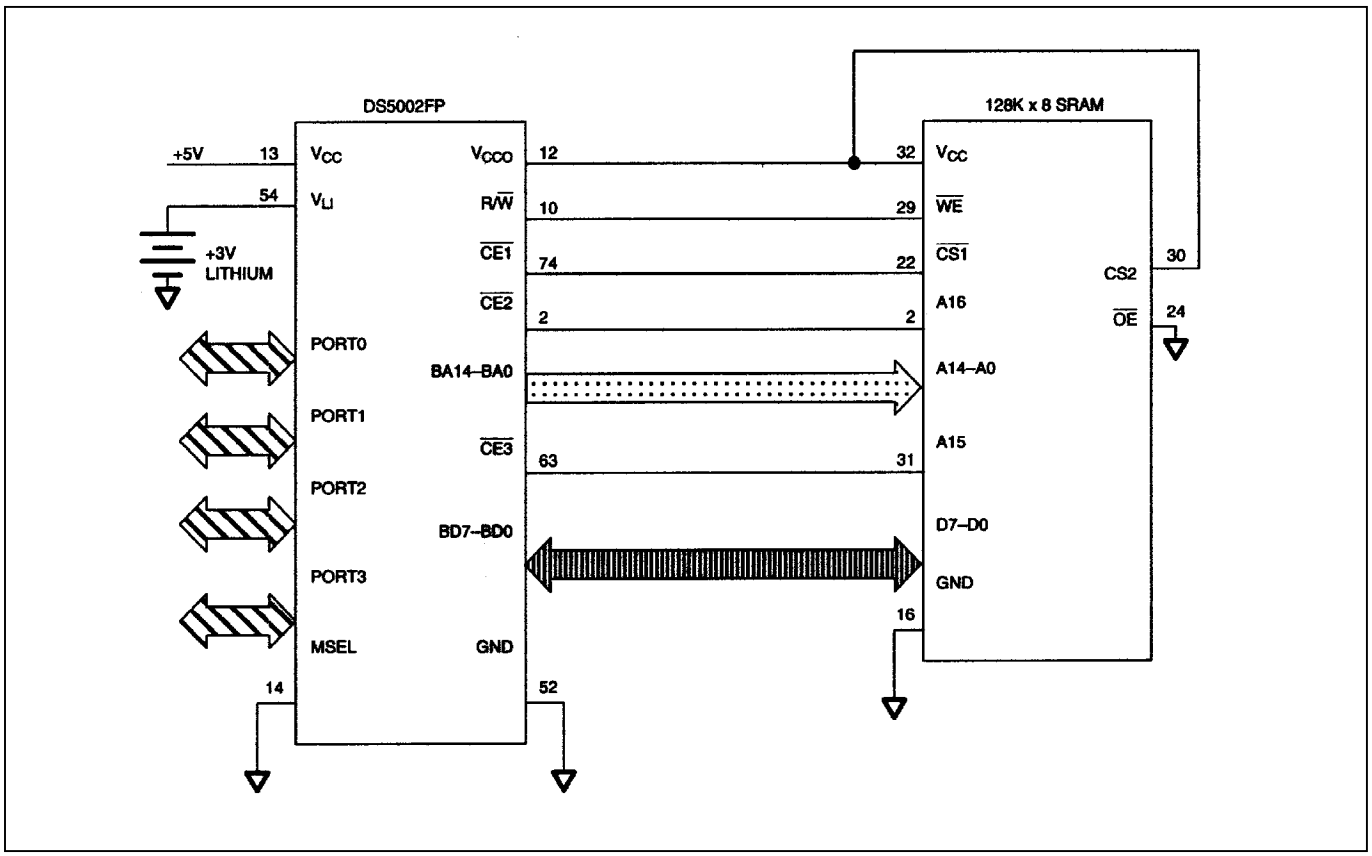


Figure 5 illustrates a typical memory connection for a system using a 128kB SRAM. Note that in this configuration, both program and data are stored in a common RAM chip Figure 6 shows a similar system with using two 32kB SRAMs. The byte-wide address bus connects to the SRAM address lines. The bidirectional byte-wide data bus connects the data I/O lines of the SRAM.

Figure 5. CONNECTION TO 128k x 8 SRAM



ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..……-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Related to Ground……-0.3V to 6.0V
Operating Temperature Range……...-40°C to +85°C
Storage Temperature Range (Note 1)……..-55°C to +125°C
Soldering Temperature…….See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Note 1: Storage temperature is defined as the temperature of the device when V_{CC} = 0V and V_{LI} = 0V. In this state, the contents of SRAM are not battery-backed and are undefined.

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Low Voltage	V_{IL}	-0.3		+0.8	V	1
Input High Voltage	V_{IH1}	2.0		V_{CC} + 0.3	V	1
Input High Voltage (RST, XTAL1, $\overline{PROG}$)	V_{IH2}	3.5		V_{CC} + 0.3	V	1
Output Low Voltage at I_{OL} = 1.6mA (Ports 1, 2, 3, $\overline{PF}$)	V_{OL1}		0.15	0.45	V	1, 11
Output Low Voltage at I_{OL} = 3.2mA (Ports 0, ALE, $\overline{PSEN}$, BA15–0, BD7–0, R/$\overline{W}$, $\overline{CE1N}$, $\overline{CE}$ 1–4, $\overline{PE}$ 1–4, V_{RST})	V_{OL2}		0.15	0.45	V	1
Output High Voltage at I_{OH} = -80µA (Ports 1, 2, 3)	V_{OH1}	2.4	4.8		V	1
Output High Voltage at I_{OH} = -400µA (Ports 0, ALE, $\overline{PSEN}$, $\overline{PF}$, BA15–0, BD7–0, R/$\overline{W}$, $\overline{CE1N}$, $\overline{CE}$ 1–4, $\overline{PE}$ 1–4, V_{RST})	V_{OH2}	2.4	4.8		V	1
Input Low Current V_{IN} = 0.45V (Ports 1, 2, 3)	I_{IL}			-50	µA	
Transition Current; 1 to 0 V_{IN} = 2.0V (Ports 1, 2, 3) (0°C to +70°C)	I_{TL}			-500	µA	
Transition Current; 1 to 0 V_{IN} = 2.0V (Ports 1, 2, 3) (-40°C to +85°C)	I_{TL}			-600	µA	10

DC CHARACTERISTICS (continued)

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

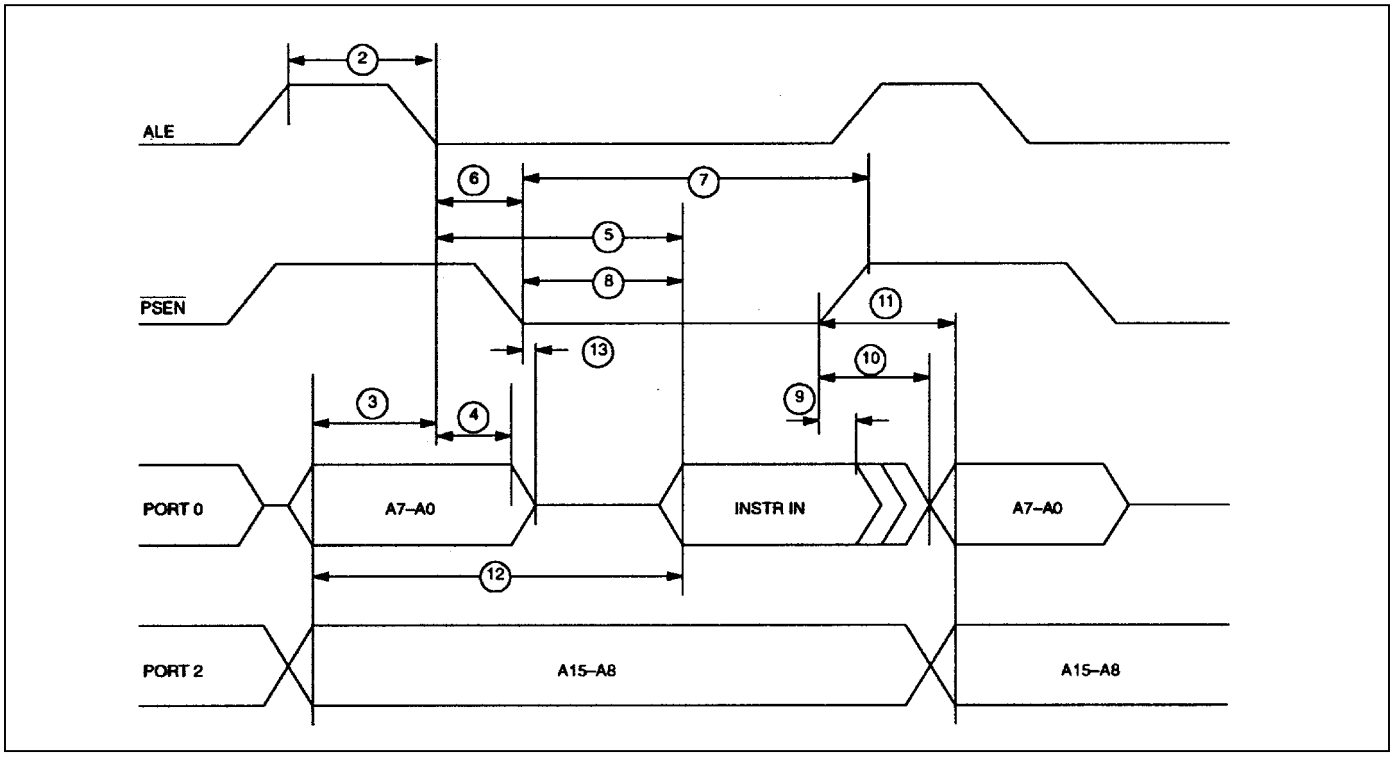
PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current 0.45 < V_{IN} < V_{CC} (Port 0, MSEL)		I_{IL}			+10	µA	
RST Pulldown Resistor (0°C to +70°C)		R_{RE}	40		150	kΩ	
RST Pulldown Resistor (-40°C to +85°C)		R_{RE}	30		180	kΩ	10
$\overline{VRST}$ Pullup Resistor		R_{VR}		4.7		kΩ	
$\overline{PROG}$ Pullup Resistor		R_{PR}		40		kΩ	
Power-Fail Warning Voltage (0°C to +70°C)		V_{PFW}	4.25	4.37	4.50	V	1
Power-Fail Warning Voltage (-40°C to +85°C)		V_{PFW}	4.1	4.37	4.6	V	1, 10
Minimum Operating Voltage (0°C to +70°C)		V_{CCMIN}	4.00	4.12	4.25	V	1
Minimum Operating Voltage (-40°C to +85°C)		V_{CCMIN}	3.85	4.09	4.25	V	1, 10
Operating Voltage		V_{CC}	V_{CCMIN}		5.5	V	1
Lithium Supply Voltage		V_{LI}	2.5		4.0	V	1
Operating Current at 16MHz		I_{CC}			36	mA	2
Idle Mode Current at 12MHz (0°C to +70°C)		I_{IDLE}			7.0	mA	3
Idle Mode Current at 12MHz (-40°C to +85°C)		I_{IDLE}			8.0	mA	3, 10
Stop Mode Current		I_{STOP}			80	µA	4
Pin Capacitance		C_{IN}			10	pF	5
Output Supply Voltage (V_{CCO})		V_{CCO1}	V_{CC} -0.45			V	1, 2
Output Supply Battery-Backed Mode (V_{CCO}, $\overline{CE}$ 1-4, $\overline{PE}$ 1-2) (0°C to +70°C)		V_{CCO2}	V_{LI} -0.65			V	1, 8
Output Supply Battery-Backed Mode (V_{CCO}, $\overline{CE}$ 1-4, $\overline{PE}$ 1-2) (-40°C to +85°C)		V_{CCO2}	V_{LI} -0.9			V	1, 8, 10
Output Supply Current at V_{CCO} = V_{CC} - 0.45V		I_{CCO1}			75	mA	6
Lithium-Backed Quiescent Current (0°C to +70°C)		I_{LI}		5	75	nA	7
Lithium-Backed Quiescent Current (-40°C to +85°C)		I_{LI}		75	500	nA	7
Reset Trip Point in Stop Mode	With BAT = 3.0V (0°C to +70°C)		4.0		4.25		1
	With BAT = 3.0V (-40°C to +85°C)		3.85		4.25		1, 10
	With BAT = 3.0V (0°C to +70°C)		4.4		4.65		1

AC CHARACTERISTICS: EXPANDED BUS MODE TIMING SPECIFICATIONS

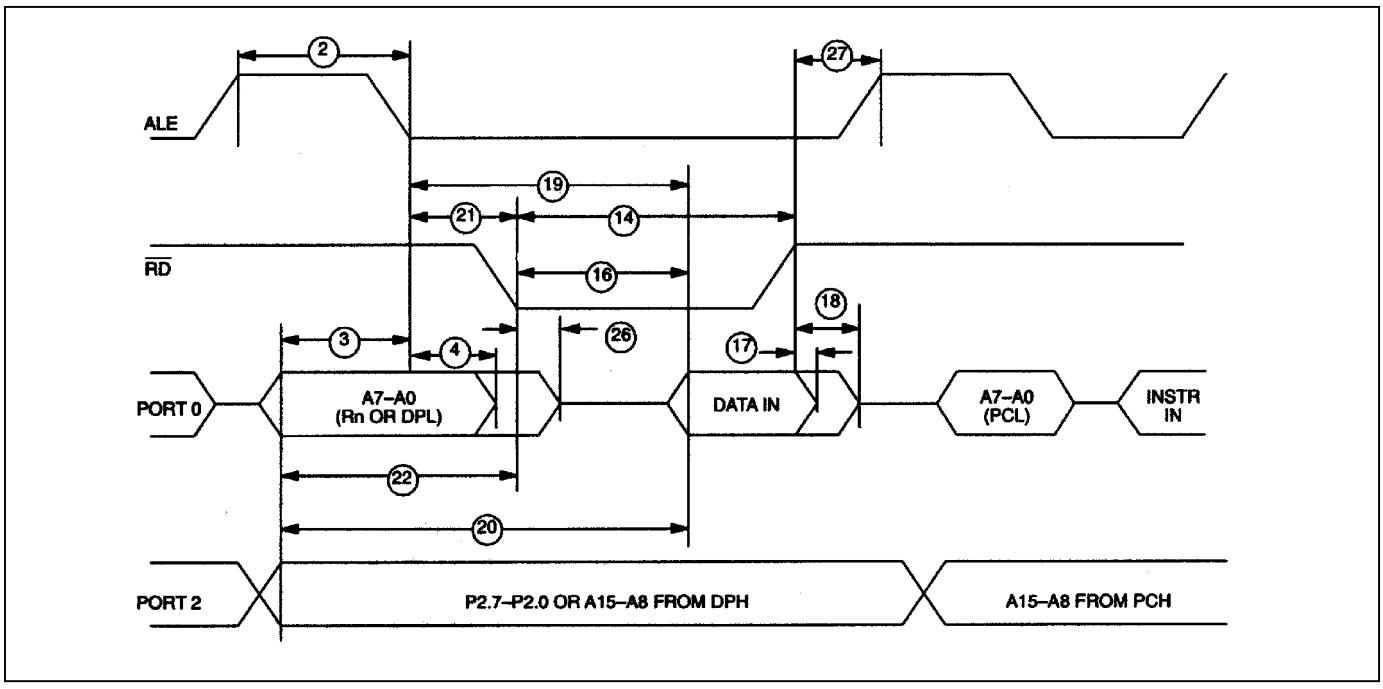
(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

#	PARAMETER		SYMBOL	MIN	MAX	UNITS
1	Oscillator Frequency		$1/t_{CLK}$	1.0	16	MHz
2	ALE Pulse Width		t_{ALPW}	$2t_{CLK}$ - 40		ns
3	Address Valid to ALE Low		t_{AVALL}	t_{CLK} - 40		ns
4	Address Hold After ALE Low		t_{AVAAV}	t_{CLK} - 35		ns
5	ALE Low to Valid Instruction In	at 12MHz	t_{ALLVI}		$4t_{CLK}$ - 150	ns
		at 16MHz			$4t_{CLK}$ - 90	
6	ALE Low to $\overline{PSEN}$ Low		t_{ALLPSL}	t_{CLK} - 25		ns
7	$\overline{PSEN}$ Pulse Width		t_{PSPW}	$3t_{CLK}$ - 35		ns
8	$\overline{PSEN}$ Low to Valid Instruction In	at 12MHz	t_{PSLVI}		$3t_{CLK}$ - 150	ns
		at 16MHz			$3t_{CLK}$ - 90	
9	Input Instruction Hold After $\overline{PSEN}$ Going High		t_{PSIV}	0		ns
10	Input Instruction Float After $\overline{PSEN}$ Going High		t_{PSIX}		t_{CLK} - 20	ns
11	Address Hold After $\overline{PSEN}$ Going High		t_{PSAV}	t_{CLK} - 8		ns
12	Address Valid to Valid Instruction In	at 12MHz	t_{AVVI}		$5t_{CLK}$ - 150	ns
		at 16MHz			$5t_{CLK}$ - 90	
13	$\overline{PSEN}$ Low to Address Float		t_{PSLAZ}	0		ns
14	$\overline{RD}$ Pulse Width		t_{RDPW}	$6t_{CLK}$ - 100		ns
15	$\overline{WR}$ Pulse Width		t_{WRPW}	$6t_{CLK}$ - 100		ns
16	$\overline{RD}$ Low to Valid Data In	at 12MHz	t_{RDLDV}		$5t_{CLK}$ - 165	ns
		at 16MHz			$5t_{CLK}$ - 105	
17	Data Hold After $\overline{RD}$ High		t_{RDHDV}	0		ns
18	Data Float After $\overline{RD}$ High		t_{RDHDZ}		$2t_{CLK}$ - 70	ns
19	ALE Low to Valid Data In	at 12MHz	t_{ALLVD}		$8t_{CLK}$ - 150	ns
		at 16MHz			$8t_{CLK}$ - 90	
20	Valid Address to Valid Data In	at 12MHz	t_{AVDV}		$9t_{CLK}$ - 165	ns
		at 16MHz			$9t_{CLK}$ - 105	
21	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low		t_{ALLRDL}	$3t_{CLK}$ - 50	$3t_{CLK}$ + 50	ns
22	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low		t_{AVRDL}	$4t_{CLK}$ - 130		ns
23	Data Valid to $\overline{WR}$ Going Low		t_{DVWRL}	t_{CLK} - 60		ns
24	Data Valid to $\overline{WR}$ High	at 12MHz	t_{DVWRH}	$7t_{CLK}$ - 150		ns
		at 16MHz		$7t_{CLK}$ - 90		
25	Data Valid After $\overline{WR}$ High		t_{WRHDV}	t_{CLK} - 50		ns
26	$\overline{RD}$ Low to Address Float		t_{RDLAZ}		0	ns
27	$\overline{RD}$ or $\overline{WR}$ High to ALE High		t_{RDHALH}	t_{CLK} - 40	t_{CLK} + 50	ns

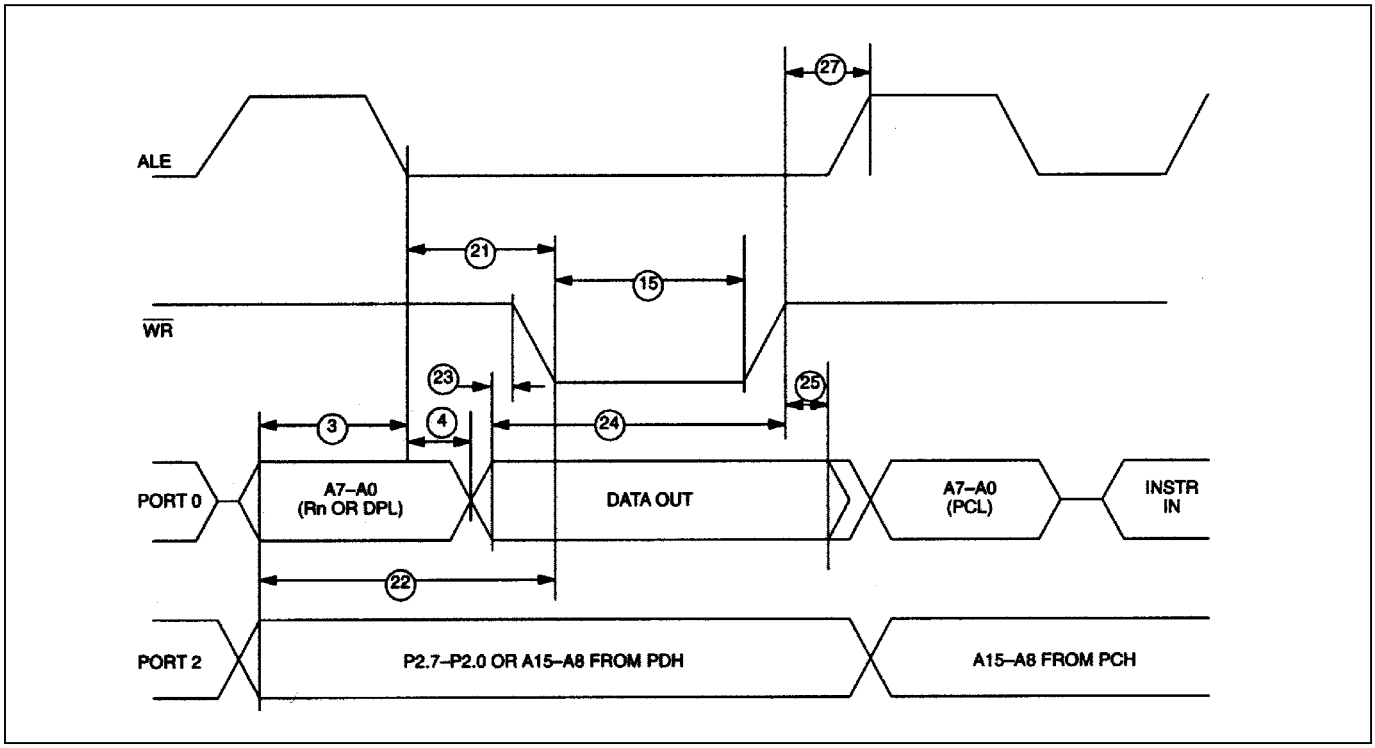
EXPANDED PROGRAM-MEMORY READ CYCLE



EXPANDED DATA-MEMORY READ CYCLE



EXPANDED DATA-MEMORY WRITE CYCLE

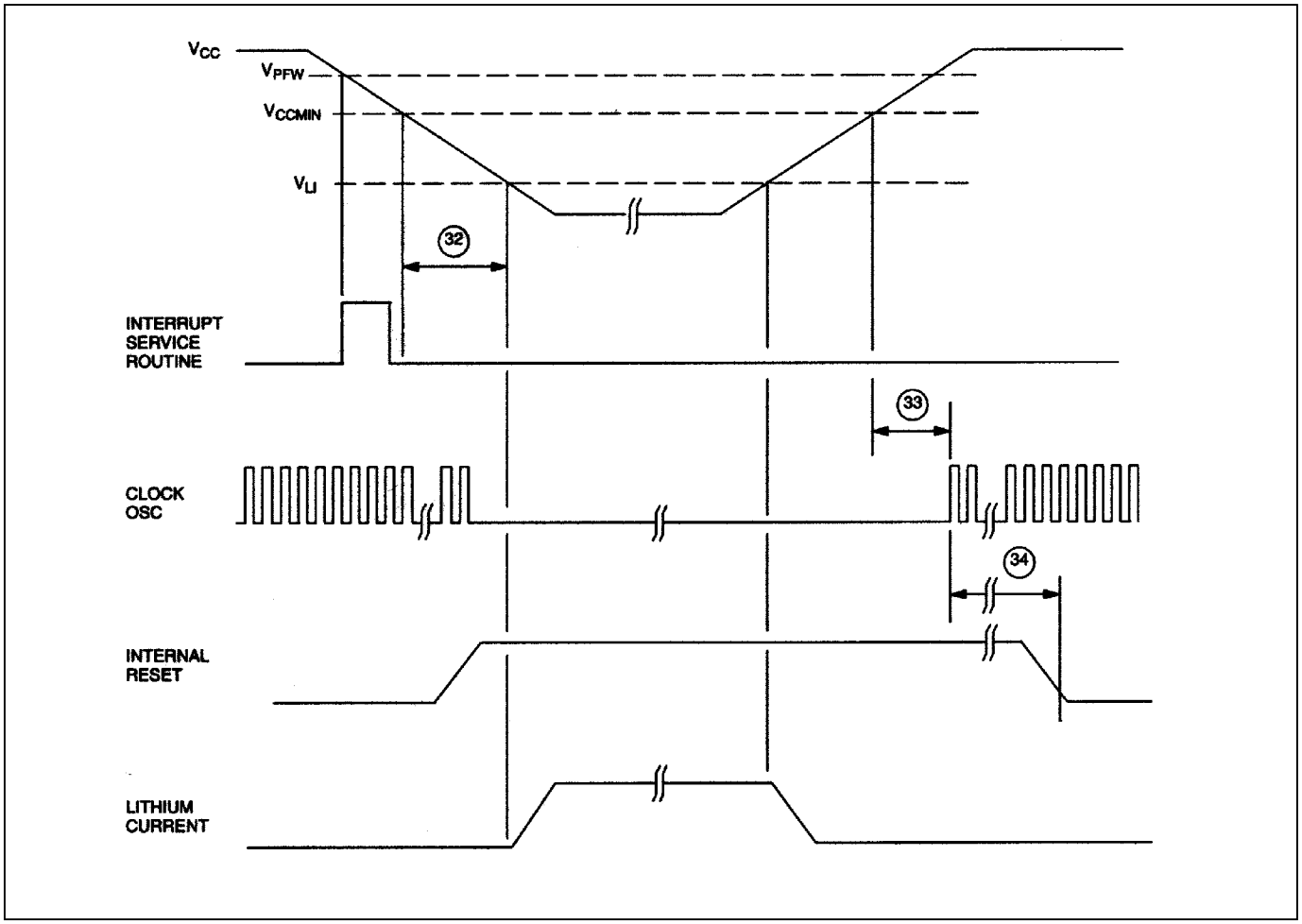


AC CHARACTERISTICS: POWER CYCLE TIME

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
32	Slew Rate from V_{CCMIN} to V_{LI}	t_F	130		µs
33	Crystal Startup Time	t_{CSU}		(Note 9)	
34	Power-On Reset Delay	t_{POR}		21,504	t_{CLK}

POWER CYCLE TIMING

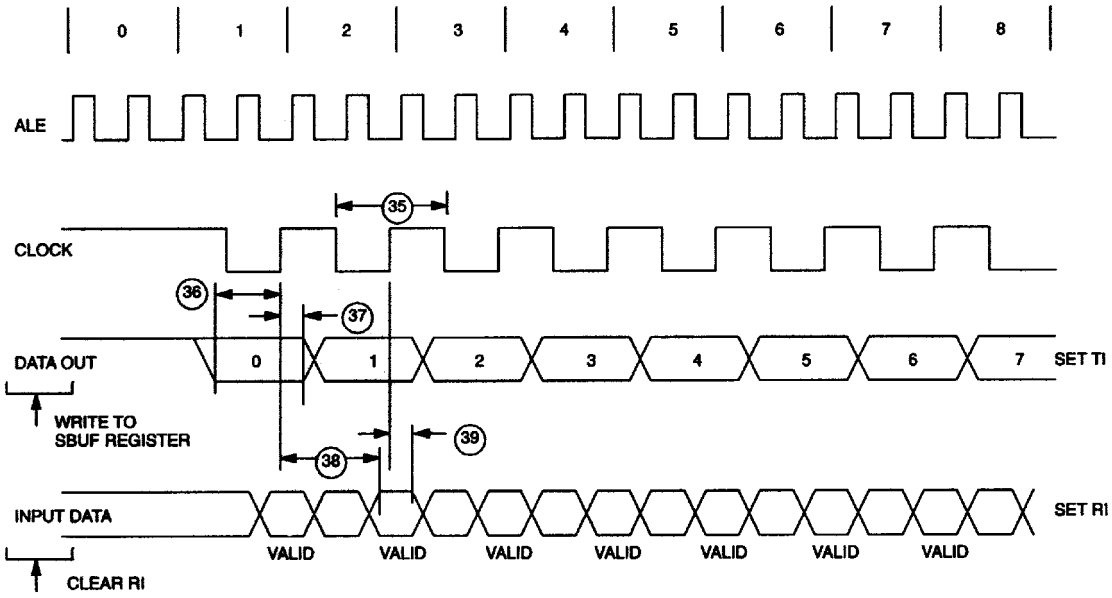


AC CHARACTERISTICS: SERIAL PORT TIMING—MODE 0

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
35	Serial-Port Clock-Cycle Time	t_{SPCLK}	$12t_{CLK}$		µs
36	Output-Data Setup to Rising-Clock Edge	t_{DOCH}	$10t_{CLK}$ - 133		ns
37	Output-Data Hold After Rising-Clock Edge	t_{CHDO}	$2t_{CLK}$ - 117		ns
38	Clock-Rising Edge to Input-Data Valid	t_{CHDV}		$10t_{CLK}$ - 133	ns
39	Input-Data Hold After Rising-Clock Edge	t_{CHDIV}	0		ns

SERIAL PORT TIMING—MODE 0

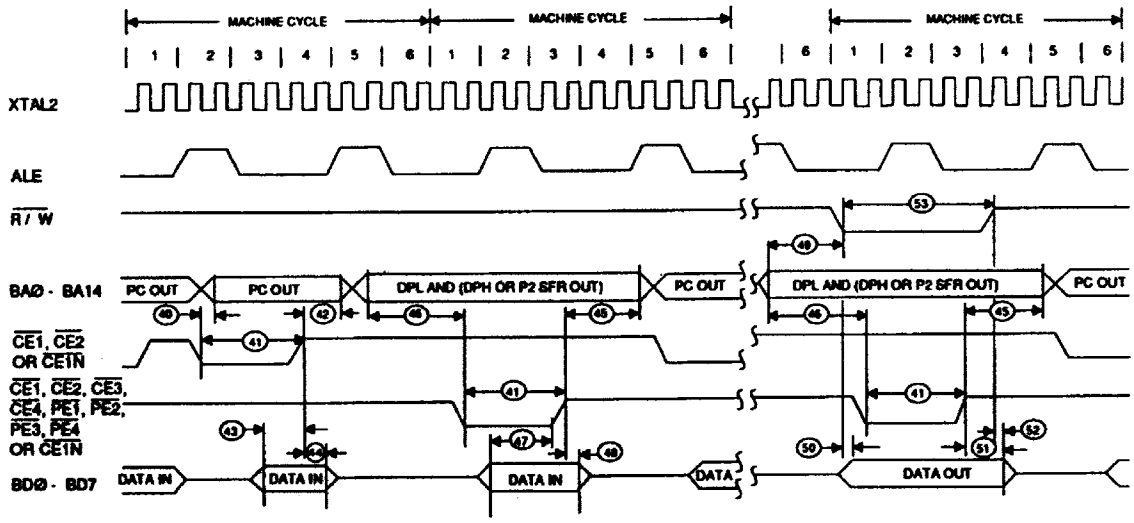


AC CHARACTERISTICS: BYTE-WIDE ADDRESS/DATA BUS TIMING

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
40	Delay to Byte-Wide Address Valid from $\overline{CE1}$, $\overline{CE2}$, or $\overline{CE1N}$ Low During Op Code Fetch	t_{CE1LPA}		30	ns
41	Pulse Width of $\overline{CE}$ 1-4, $\overline{PE}$ 1-4 or $\overline{CE1N}$	t_{CEPW}	$4t_{CLK}$ - 35		ns
42	Byte-Wide Address Hold After $\overline{CE1}$, $\overline{CE2}$, or $\overline{CE1N}$ High During Op Code Fetch	t_{CE1HPA}	$2t_{CLK}$ - 20		ns
43	Byte-Wide Data Setup to $\overline{CE1}$, $\overline{CE2}$, or $\overline{CE1N}$ High During Op Code Fetch	t_{OVCE1H}	$1t_{CLK}$ + 40		ns
44	Byte-Wide Data Hold After $\overline{CE1}$, $\overline{CE2}$ or $\overline{CE1N}$ High During Op Code Fetch	t_{CE1HOV}	0		ns
45	Byte-Wide Address Hold After $\overline{CE}$ 1-4, $\overline{PE}$ 1-4, or $\overline{CE1N}$ High During MOVX	t_{CEHDA}	$4t_{CLK}$ - 30		ns
46	Delay from Byte-Wide Address Valid $\overline{CE}$ 1-4, $\overline{PE}$ 1-4, or $\overline{CE1N}$ Low During MOVX	t_{CELDA}	$4t_{CLK}$ - 35		ns
47	Byte-Wide Data Setup to $\overline{CE}$ 1-4, $\overline{PE}$ 1-4, or $\overline{CE1N}$ High During MOVX (read)	t_{DACEH}	$1t_{CLK}$ + 40		ns
48	Byte-Wide Data Hold After $\overline{CE}$ 1-4, $\overline{PE}$ 1-4, or $\overline{CE1N}$ High During MOVX (read)	t_{CEHDV}	0		ns
49	Byte-Wide Address Valid to R/$\overline{W}$ Active During MOVX (write)	t_{AVRWL}	$3t_{CLK}$ - 35		ns
50	Delay from R/$\overline{W}$ Low to Valid Data Out During MOVX (write)	t_{RWLDV}	20		ns
51	Valid Data-Out Hold Time from $\overline{CE}$ 1-4, $\overline{PE}$ 1-4, or $\overline{CE1N}$ High	t_{CEHDV}	$1t_{CLK}$ - 15		ns
52	Valid Data-Out Hold Time from R/$\overline{W}$ High	t_{RWHDV}	0		ns
53	Write Pulse Width (R/$\overline{W}$ Low Time)	t_{RWLPW}	$6t_{CLK}$ - 20		ns

BYTE-WIDE BUS TIMING



RPC AC CHARACTERISTICS: DBB READ

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

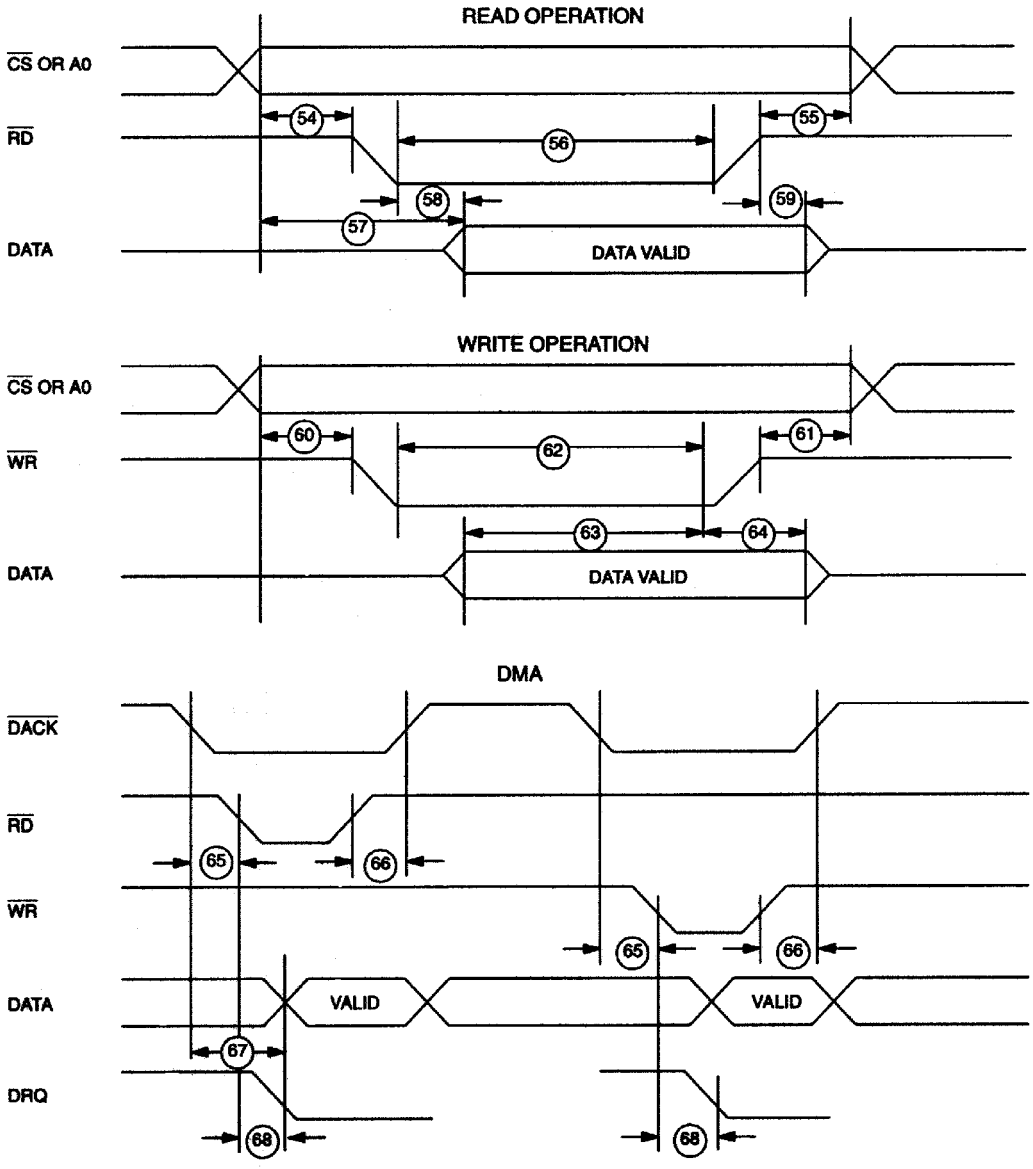
#	PARAMETER	SYMBOL	MIN	MAX	UNITS
54	$\overline{CS}$, A_0 Setup to $\overline{RD}$	t_{AR}	0		ns
55	$\overline{CS}$, A_0 Hold After $\overline{RD}$	t_{RA}	0		ns
56	$\overline{RD}$ Pulse Width	t_{RR}	160		ns
57	$\overline{CS}$, A_0 to Data-Out Delay	t_{AD}		130	ns
58	$\overline{RD}$ to Data-Out Delay	t_{RD}	0	130	ns
59	$\overline{RD}$ to Data-Float Delay	t_{RDZ}		85	ns

RPC AC CHARACTERISTICS: DBB WRITE

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
60	$\overline{CS}$, A_0 Setup to $\overline{WR}$	t_{AW}	0		ns
61A	$\overline{CS}$, Hold After $\overline{WR}$	t_{WA}	0		ns
61B	A_0, Hold After $\overline{WR}$	t_{WA}	20		ns
62	$\overline{WR}$ Pulse Width	t_{WW}	160		ns
63	Data Setup to $\overline{WR}$	t_{DW}	130		ns
64	Data Hold After $\overline{WR}$	t_{WD}	20		ns

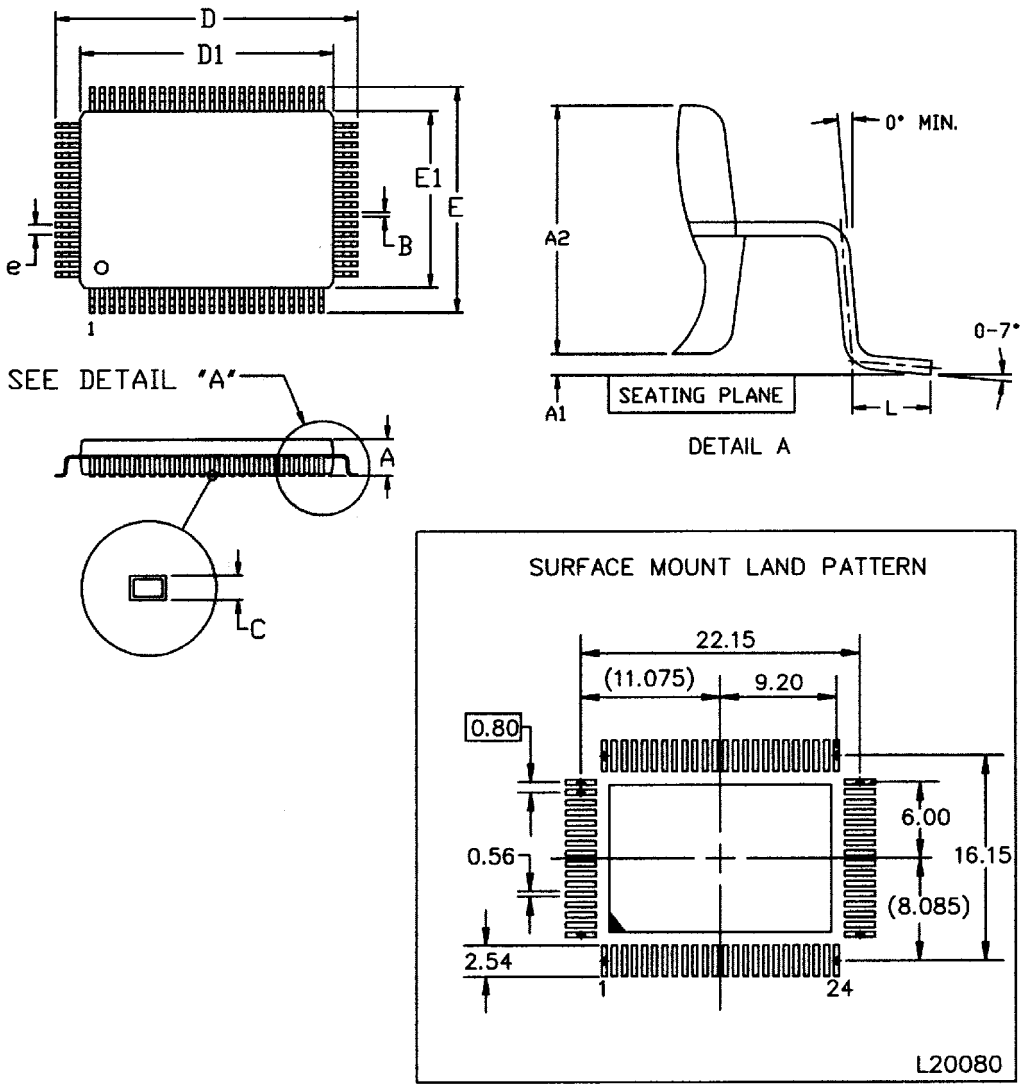
RPC TIMING MODE



PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

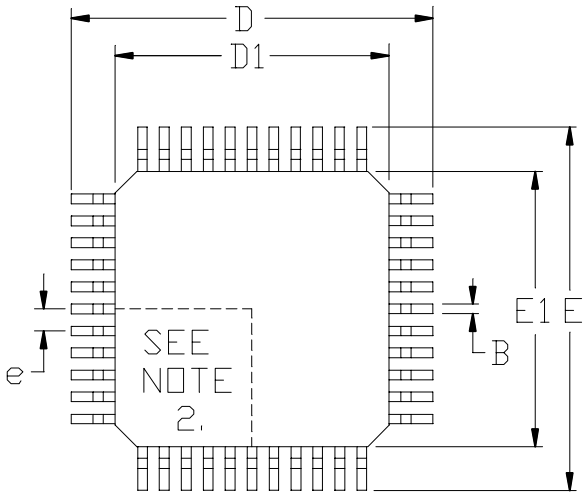
80-PIN MQFP



DIM	MM	
	MIN	MAX
A	-	3.40
A1	0.25	-
A2	2.55	2.87
B	0.30	0.50
C	0.13	0.23
D	23.70	24.10
D1	19.90	20.10
E	17.70	18.10
E1	13.90	14.10
e	0.80 BSC	
L	0.65	0.95

56-G4005-001

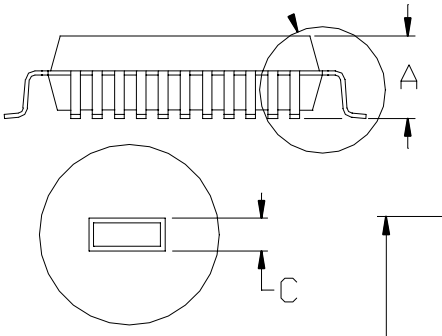
44-PIN MQFP



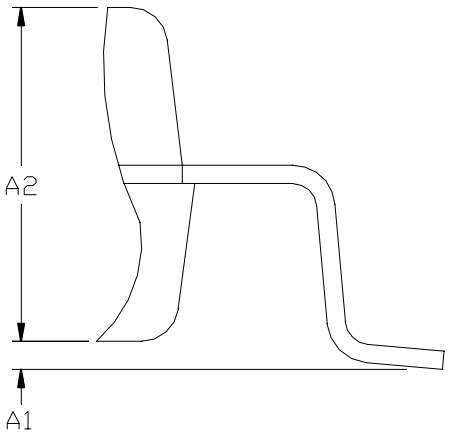
NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIED ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSION; ±D ON LOWER

SEE DETAIL "A"



DIM	MIN	MAX
A	–	2.45
A1	0.10	0.30
A2	1.95	2.10
D	13.65	14.30
D1	9.90	10.10
E	13.65	14.30
E1	9.90	10.10
L	0.63	1.03
e	0.80 BSC	
B	0.30	0.45
C	0.13	0.23



DETAIL A

DIMENSIONS ARE IN MILLIMETERS