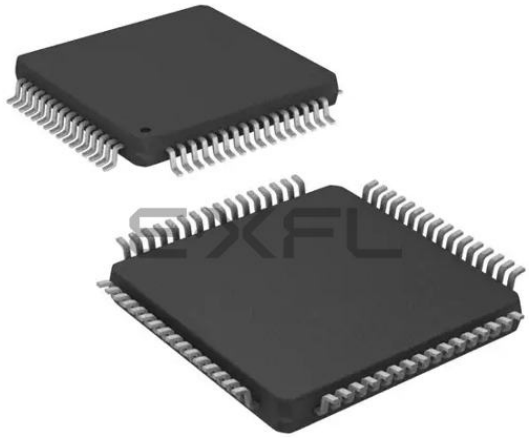

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128ga406t-i-pt

TABLE 1-1: DEVICE FEATURES FOR THE PIC24FJ256GA412/GB412 FAMILY: 64-PIN

Features	PIC24FJXXXGA/GB406					
	64GA	128GA	256GA	64GB	128GB	256GB
Operating Frequency	DC – 32 MHz					
Program Memory (bytes)	64K	128K	256K	64K	128K	256K
Program Memory (instructions)	22,016	44,032	88,064	22,016	44,032	88,064
Data Memory (bytes)	8K	16K		8K	16K	
Interrupt Sources (soft vectors/ NMI traps)	113 (107/6)					
I/O Ports	Ports B, C, D, E, F, G					
Total I/O Pins	53			52		
Remappable Pins	30 (29 I/Os, 1 input only)			29 (28 I/Os, 1 input only)		
Timers:						
Total Number (16-bit)	19(1,2)					
32-Bit (from paired 16-bit timers)	9					
Input Capture w/Timer Channels	6(2)					
Output Compare/PWM Channels	6(2)					
Capture/Compare/PWM/Timer:						
Single Output (SCCP)	6(2)					
Multiple Output (MCCP)	1(2)					
Serial Communications:						
UART	6(2)					
SPI (3-wire/4-wire)	4(2)					
I^2C	3					
USB On-The-Go	No			Yes		
Cryptographic Engine	Yes					
Parallel Communications (EPMP/PSP)	Yes					
10/12-Bit Analog-to-Digital Converter (A/D) (input channels)	16					
Digital-to-Analog Converter (DAC)	1					
Analog Comparators	3					
CTMU Interface	Yes					
LCD Controller (available pixels)	248 (35 SEG x 8 COM)			240 (34 SEG x 8 COM)		
JTAG Boundary Scan	Yes					
Resets (and delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, $\overline{MCLR}$, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)					
Instruction Set	77 Base Instructions, Multiple Addressing Mode Variations					
Packages	64-Pin TQFP and QFN					

Note 1: Includes the Timer modes of the SCCP and MCCP modules.

2: Some instantiations of these modules are only available through remappable pins.

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
OCM1A	4	10	E3	O	DIG	MCCP1 Outputs
OCM1B	5	11	F4	O	DIG	
OCM1C	—	1	B2	O	DIG	
OCM1D	—	6	D1	O	DIG	
OCM1E	—	91	C5	O	DIG	
OCM1F	—	92	B5	O	DIG	
OCM2	6	12	F2	O	DIG	SCCP2 Output
OCM3	11	20	H1	O	DIG	SCCP3 Output
OSCI	39	63	F9	I	ANA/ST	Main Oscillator Input Connection
OSCO	40	64	F11	O	—	Main Oscillator Output Connection
PGEC1	15	24	K1	I	ST	ICSP™ Programming Clock
PGEC2	17	26	L1	I	ST	
PGEC3	11	20	H1	I	ST	
PGED1	16	25	K2	I/O	DIG/ST	ICSP Programming Data
PGED2	18	27	J3	I/O	DIG/ST	
PGED3	12	21	H2	I/O	DIG/ST	
PMA0/PMALL	30	44	L8	I/O	DIG/ST/TTL	Parallel Master Port Address<0>/Address Latch Low
PMA1/PMALH	29	43	K7	I/O	DIG/ST/TTL	Parallel Master Port Address<1>/Address Latch High
PMA14/PMCS/ APMCS1	45	71	C11	I/O	DIG/ST/TTL	Parallel Master Port Address<14>/Slave Chip Select/Alternate Chip Select 1 Strobe
PMA15/APMCS2	44	70	D11	I/O	DIG/ST/TTL	Parallel Master Port Address<15>/Alternate Chip Select 2 Strobe
PMA6	16	29	K3	O	DIG	Parallel Master Port Address
PMA7	22	28	L2	O	DIG	
PMA8	32	50	L11	I/O	DIG/ST/TTL	Parallel Master Port Address (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMA9	31	49	L10	I/O	DIG/ST/TTL	
PMA10	28	42	L7	I/O	DIG/ST/TTL	
PMA11	27	41	J7	I/O	DIG/ST/TTL	
PMA12	24	35	K5	I/O	DIG/ST/TTL	
PMA13	23	34	H5	I/O	DIG/ST/TTL	
PMA16	—	95	E16	O	DIG	
PMA17	—	92	E11	O	DIG	
PMA18	—	40	K6	O	DIG	
PMA19	—	19	G2	O	DIG	
PMA2/PMALU	8	14	F3	O	DIG	Parallel Master Port Address<2>/Address Latch Upper
PMA3	6	12	F2	O	DIG	Parallel Master Port Address
PMA4	5	11	F4	O	DIG	
PMA5	4	10	E3	O	DIG	
PMA20	—	59	G10	O	DIG	Parallel Master Port Address (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMA21	—	60	G11	O	DIG	
PMA22	—	66	E11	O	DIG	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

4.1.4 FLASH CONFIGURATION WORDS

In PIC24FJ256GA412/GB412 family devices, the top nine words of on-chip program memory are reserved for configuration information. On device Reset, the configuration information is copied into the actual Configuration registers, located in configuration space.

The address range of the Flash Configuration Words for devices in the PIC24FJ256GA412/GB412 family are shown in Table 4-2. Their location in the memory map is shown with the other memory vectors in Figure 4-1. Additional details on the device Configuration Words are provided in **Section 33.0 "Special Features"**.

4.1.4.1 Dual Partition Configuration Words

In Dual Partition Flash modes, each partition has its own set of Flash Configuration Words. The full set of Configuration registers in the Active Partition is used to determine the device's configuration; the Configuration Words in the Inactive Partition are used to determine the device's configuration when that partition becomes active. However, some of the Configuration registers in the Inactive Partition (FSEC, FBSLIM and FSIGN) may be used to determine how the Active Partition is able or allowed to access the Inactive Partition.

4.1.5 ONE-TIME-PROGRAMMABLE (OTP) MEMORY

PIC24FJ256GA412/GB412 family devices provide 384 bytes of One-Time-Programmable (OTP) memory, located at addresses, 801380h through 8013FEh. This memory can be used for persistent storage of application-specific information that will not be erased by reprogramming the device. This includes many types of information, such as (but not limited to):

- Application checksums
- Code revision information
- Product information
- Serial numbers
- System manufacturing dates
- Manufacturing lot numbers

OTP memory may be programmed in any mode, including user RTSP mode, but it cannot be erased. Data is not cleared by a Chip Erase. Once programmed, it cannot be rewritten.

Do not perform repeated write operations on the OTP.

TABLE 4-2: FLASH CONFIGURATION WORDS FOR PIC24FJ256GA412/GB412 FAMILY DEVICES

Device Family	Program Memory (Words)	Configuration Word Address Range	
		Single Partition	Dual Partition(1)
PIC24FJ64GA4XX/GB4XX	22,016	00AF80h:00AFB0h	005780h:0057FCh
PIC24FJ128GA4XX/GB4XX	44,032	015780h:0157B0h	00AB80h:00ABFCh
PIC24FJ256GA4XX/GB4XX	88,065	02AF80h:02AFB0h	015780h:0157FCh

Note 1: Addresses for the Active Partition are shown. For the Inactive Partitions, add 400000h.

8.0 INTERRUPT CONTROLLER

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Interrupts"** (DS70000600). The information in this data sheet supersedes the information in the FRM.

The PIC24F interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the PIC24F CPU. It has the following features:

- Up to 8 Processor Exceptions and Software Traps
- Seven User-Selectable Priority Levels
- Interrupt Vector Table (IVT) with up to 118 Vectors
- Unique Vector for Each Interrupt or Exception Source
- Fixed Priority within a Specified User Priority Level
- Alternate Interrupt Vector Table (AIVT) for Debug Support
- Fixed Interrupt Entry and Return Latencies

8.1 Interrupt Vector Table

The Interrupt Vector Table (IVT) is shown in Figure 8-1. The IVT resides in program memory, starting at location, 000004h. The IVT contains 126 vectors, consisting of 8 non-maskable trap vectors, plus up to 118 source interrupts. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority; this is linked to their position in the vector table. All other things being equal, lower addresses have a higher natural priority. For example, the interrupt associated with Vector 0 will take priority over interrupts at any other vector address.

PIC24FJ256GA412/GB412 family devices implement non-maskable traps and unique interrupts. These are summarized in Table 8-1 and Table 8-2.

8.1.1 ALTERNATE INTERRUPT VECTOR TABLE

The Alternate Interrupt Vector Table (AIVT) is located after the IVT, as shown in Figure 8-1. The ALTIVT (INTCON2<8>) control bit provides access to the AIVT. If the ALTIVT bit is set, all interrupt and exception processes will use the alternate vectors instead of the default vectors. The alternate vectors are organized in the same manner as the default vectors.

The AIVT supports emulation and debugging efforts by providing a means to switch between an application, and a support environment, without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time. If the AIVT is not needed, the AIVT should be programmed with the same addresses used in the IVT.

8.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The PIC24F devices clear their registers in response to a Reset, which forces the PC to zero. The microcontroller then begins program execution at location, 000000h. The user programs a GOTO instruction at the Reset address, which redirects program execution to the appropriate start-up routine.

Note:	Any unimplemented or unused vector locations in the IVT and AIVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

REGISTER 8-9: IFS3: INTERRUPT FLAG STATUS REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CCP1IF	RTCIF	DMA5IF	SPI3RXIF	SPI2RXIF	SPI1RXIF	SPI4RXIF	KEYSTRIF
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
CRYDNIF	INT4IF	INT3IF	—	CCT7IF	MI2C2IF	SI2C2IF	CCT6IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CCP1IF:** MCCP1 Capture/Compare Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 14 **RTCIF:** Real-Time Clock and Calendar Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13 **DMA5IF:** DMA Channel 5 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12 **SPI3RXIF:** SPI3 Receive Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 11 **SPI2RXIF:** SPI2 Receive Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 10 **SPI1RXIF:** SPI1 Receive Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 9 **SPI4RXIF:** SPI4 Receive Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 8 **KEYSTRIF:** Cryptographic Key Store Program Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 7 **CRYDNIF:** Cryptographic Operation Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6 **INT4IF:** External Interrupt 4 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5 **INT3IF:** External Interrupt 3 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4 **Unimplemented:** Read as '0'

bit 3 **CCT7IF:** SCCP7 Timer Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 8-25: IPC3: INTERRUPT PRIORITY CONTROL REGISTER 3

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	NVMIP2	NVMIP1	NVMIP0	—	DMA1IP2	DMA1IP1	DMA1IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	AD1IP2	AD1IP1	AD1IP0	—	U1TXIP2	U1TXIP1	U1TXIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-11 **NVMIP<2:0>:** Flash Memory Write/Program Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 10-8 **DMA1IP<2:0>:** DMA Channel 1 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **AD1IP<2:0>:** 12-Bit Pipeline A/D Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **U1TXIP<2:0>:** UART1 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-49: IPC27: INTERRUPT PRIORITY CONTROL REGISTER 27

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U5RXIP2	U5RXIP1	U5RXIP0	—	RTCTSIP2	RTCTSIP1	RTCTSIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	I2C3BCIP2	I2C3BCIP1	I2C3BCIP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **U5RXIP<2:0>:** UART5 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 1 **Unimplemented:** Read as '0'

bit 10-8 **RTCTSIP<2:0>:** RTCC Timestamp Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **I2C3BCIP<2:0>:** I2C3 Bus Collision Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

REGISTER 11-31: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP17R5	RP17R4	RP17R3	RP17R2	RP17R1	RP17R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP16R5	RP16R4	RP16R3	RP16R2	RP16R1	RP16R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP17R<5:0>:** RP17 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP17 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP16R<5:0>:** RP16 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP16 (see Table 11-12 for peripheral function numbers).

REGISTER 11-32: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP19R5	RP19R4	RP19R3	RP19R2	RP19R1	RP19R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP18R5	RP18R4	RP18R3	RP18R2	RP18R1	RP18R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP19R<5:0>:** RP19 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP19 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP18R<5:0>:** RP18 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP18 (see Table 11-12 for peripheral function numbers).

REGISTER 19-4: UxTXREG: UARTx TRANSMIT REGISTER (NORMALLY WRITE-ONLY)

W-x	U-0	U-0	U-0	U-0	U-0	U-0	W-x
LAST(1)	—	—	—	—	—	—	TX8
bit 15							bit 8

W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **LAST:** Last Byte Indicator for Smart Card Support bit(1)

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **TX8:** Data of the Transmitted Character bit (in 9-bit mode)

bit 7-0 **TX<7:0>:** Data of the Transmitted Character bits

Note 1: This bit is only available for UART1 and UART2.

22.0 LIQUID CRYSTAL DISPLAY (LCD) CONTROLLER

Note:	This data sheet summarizes the features of the PIC24FJ256GA412/GB412 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Liquid Crystal Display (LCD)"** (DS30009740) which is available from the Microchip web site (www.microchip.com).

The Liquid Crystal Display (LCD) Controller generates the data and timing control required to directly drive a static or multiplexed LCD panel. The module can drive up to 8 Commons signals on all devices, and from 34 to 64 Segments, depending on the specific device.

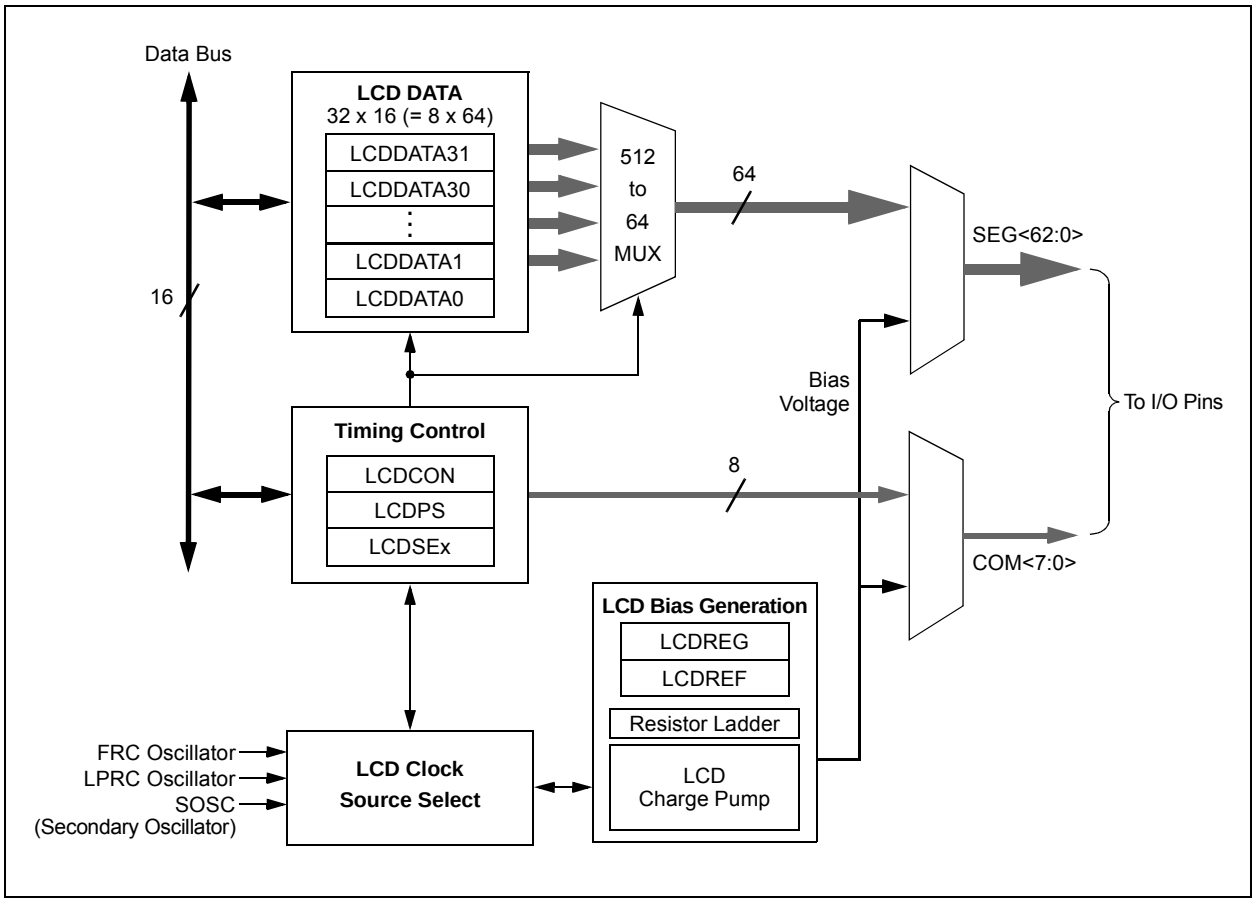
Note:	To be driven by the LCD controller, pins must be set as analog inputs. For the port corresponding to the desired Common or Segment pin, set TRISx = 1 and ANSx = 1.

The LCD Controller has these features:

- Direct Driving of LCD Panel
- Three LCD Clock Sources with Selectable Prescaler
- Up to Eight Commons:
  - Static (one Common)
  - 1/2 multiplex (two Commons)
  - 1/3 multiplex (three Commons)
  - 1/8 multiplex (eight Commons)
- Ability to Drive up to 34 (in 64-pin USB devices), 35 (64-pin non-USB devices) or up to 64 (all other devices) Segments, depending on the Multiplexing Mode Selected
- Static, 1/2 or 1/3 LCD Bias
- On-Chip Bias Generator with Dedicated Charge Pump to Support a Range of Fixed and Variable Bias Options
- Internal Resistors for Bias Voltage Generation
- Software Contrast Control for LCD using Internal Biasing

A simplified block diagram of the module is shown in Figure 22-1.

FIGURE 22-1: LCD CONTROLLER MODULE BLOCK DIAGRAM



REGISTER 22-6: LCDREF: LCD REFERENCE LADDER CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LCDIRE	—	LCDCST2	LCDCST1	LCDCST0	VLCD3PE	VLCD2PE	VLCD1PE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
LRLAP1	LRLAP0	LRLBP1	LRLBP0	—	LRLAT2	LRLAT1	LRLAT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **LCDIRE**: LCD Internal Reference Enable bit
1 = Internal LCD reference is enabled and connected to the internal contrast control circuit
0 = Internal LCD reference is disabled

bit 14 **Unimplemented**: Read as '0'

bit 13-11 **LCDCST<2:0>**: LCD Contrast Control bits
Selects the Resistance of the LCD Contrast Control Resistor Ladder:
111 = Resistor ladder is at maximum resistance (minimum contrast)
110 = Resistor ladder is at 6/7th of maximum resistance
101 = Resistor ladder is at 5/7th of maximum resistance
100 = Resistor ladder is at 4/7th of maximum resistance
011 = Resistor ladder is at 3/7th of maximum resistance
010 = Resistor ladder is at 2/7th of maximum resistance
001 = Resistor ladder is at 1/7th of maximum resistance
000 = Minimum resistance (maximum contrast); resistor ladder is shorted

bit 10 **VLCD3PE**: LCD Bias 3 Pin Enable bit
1 = Bias 3 level is connected to the external pin, LCDBIAS3
0 = Bias 3 level is internal (internal resistor ladder)

bit 9 **VLCD2PE**: LCD Bias 2 Pin Enable bit
1 = Bias 2 level is connected to the external pin, LCDBIAS2
0 = Bias 2 level is internal (internal resistor ladder)

bit 8 **VLCD1PE**: LCD Bias 1 Pin Enable bit
1 = Bias 1 level is connected to the external pin, LCDBIAS1
0 = Bias 1 level is internal (internal resistor ladder)

bit 7-6 **LRLAP<1:0>**: LCD Reference Ladder A Time Power Control bits
During Time Interval A:
11 = Internal LCD reference ladder is powered in High-Power mode
10 = Internal LCD reference ladder is powered in Medium Power mode
01 = Internal LCD reference ladder is powered in Low-Power mode
00 = Internal LCD reference ladder is powered down and unconnected

bit 5-4 **LRLBP<1:0>**: LCD Reference Ladder B Time Power Control bits
During Time Interval B:
11 = Internal LCD reference ladder is powered in High-Power mode
10 = Internal LCD reference ladder is powered in Medium Power mode
01 = Internal LCD reference ladder is powered in Low-Power mode
00 = Internal LCD reference ladder is powered down and unconnected

bit 3 **Unimplemented**: Read as '0'

26.0 32-BIT PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS30009729). The information in this data sheet supersedes the information in the FRM.

The 32-bit programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-Programmable CRC Polynomial Equation, up to 32 bits
- Programmable Shift Direction (little or big-endian)
- Independent Data and Polynomial Lengths
- Configurable Interrupt Output
- Data FIFO

Figure 26-1 displays a simplified block diagram of the CRC generator. A simple version of the CRC shift engine is displayed in Figure 26-2.

FIGURE 26-1: CRC MODULE BLOCK DIAGRAM

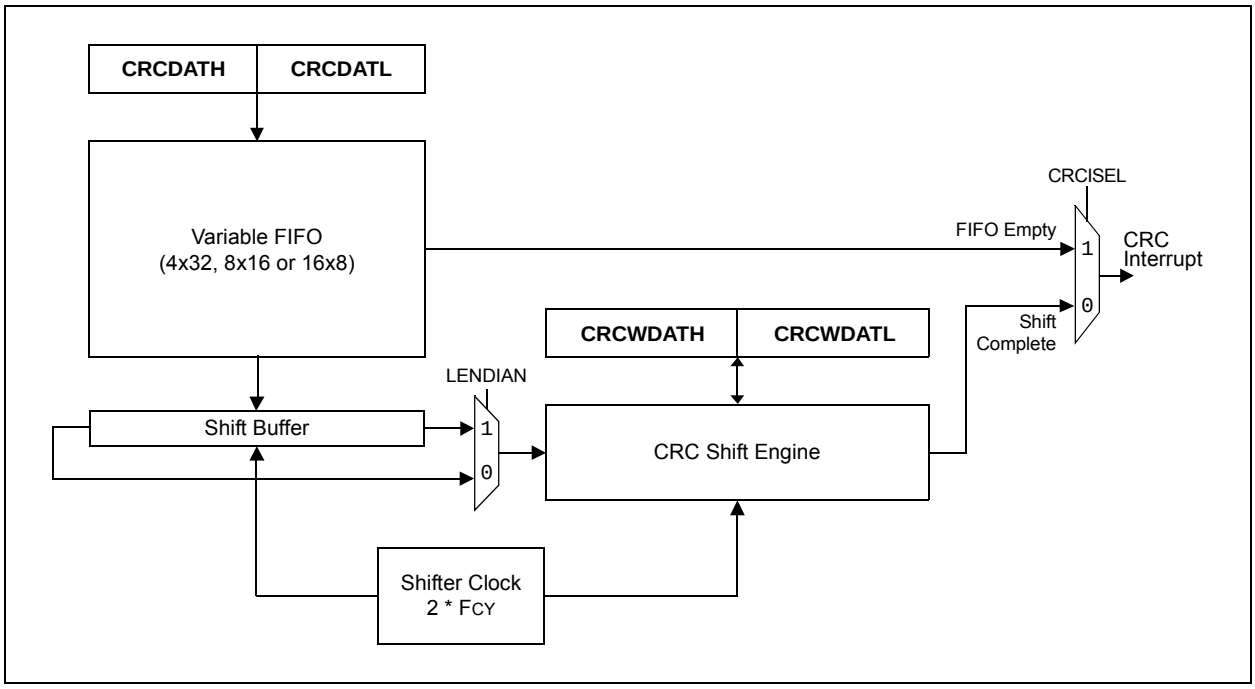
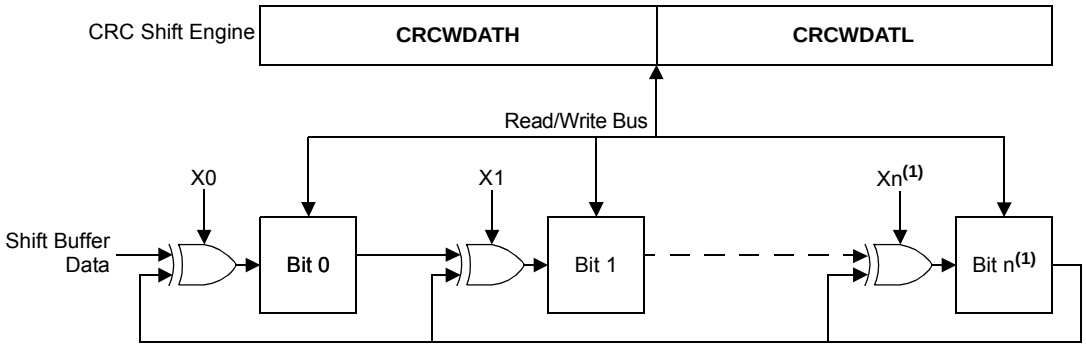


FIGURE 26-2: CRC SHIFT ENGINE DETAIL



Note 1: n = PLEN<4:1> + 1.

27.4 Registers

The 12-bit A/D Converter is controlled through a total of 13 registers:

- AD1CON1 through AD1CON5 (Register 27-1 through Register 27-5)
- AD1CHS (Register 27-6)
- AD1CHITH and AD1CHITL (Register 27-8 and Register 27-9)
- AD1CSSH and AD1CSSL (Register 27-10 and Register 27-11)
- AD1CTMENH and AD1CTMENL (Register 27-12 and Register 27-13)
- AD1DMBUF (not shown) – The 16-bit conversion buffer for Extended Buffer mode

In addition, the ANCFG register (Register 27-7) controls the band gap voltage resources for the A/D Converter, as well as other modules.

REGISTER 27-1: AD1CON1: A/D CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADON	—	ADSIDL	DMABM(1)	DMAEN	MODE12	FORM1	FORM0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
SSRC3	SSRC2	SSRC1	SSRC0	—	ASAM	SAMP	DONE
bit 7							bit 0

Legend:	C = Clearable bit	U = Unimplemented bit, read as ‘0’	
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ADON:** A/D Operating Mode bit
1 = A/D Converter module is operating
0 = A/D Converter is off

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **ADSIDL:** A/D Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **DMABM:** Extended DMA Buffer Mode Select bit(1)
1 = Extended Buffer mode: Buffer address is defined by the DMADSTn register
0 = PIA mode: Buffer addresses are defined by the DMA Controller and AD1CON4<2:0>

bit 11 **DMAEN:** Extended DMA/Buffer Enable bit
1 = Extended DMA and buffer features are enabled
0 = Extended features are disabled

bit 10 **MODE12:** 12-Bit Operation Mode bit
1 = 12-bit A/D operation
0 = 10-bit A/D operation

bit 9-8 **FORM<1:0>:** Data Output Format bits
11 = Fractional result, signed, left justified
10 = Absolute fractional result, unsigned, left justified
01 = Decimal result, signed, right justified
00 = Absolute decimal result, unsigned, right justified

Note 1: This bit is only available when Extended DMA/Buffer features are available (DMAEN = 1).

REGISTER 27-5: AD1CON5: A/D CONTROL REGISTER 5

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
ASEN	LPEN	CTMREQ	BGREQ	—	—	ASINT1	ASINT0
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	WM1	WM0	CM1	CM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ASEN:** Auto-Scan Enable bit
1 = Auto-scan is enabled
0 = Auto-scan is disabled

bit 14 **LPEN:** Low-Power Enable bit
1 = Low power is enabled after scan
0 = Full power is enabled after scan

bit 13 **CTMREQ:** CTMU Request bit
1 = CTMU is enabled when the A/D is enabled and active
0 = CTMU is not enabled by the A/D

bit 12 **BGREQ:** Band Gap Request bit
1 = Band gap is enabled when the A/D is enabled and active
0 = Band gap is not enabled by the A/D

bit 11-10 **Unimplemented:** Read as '0'

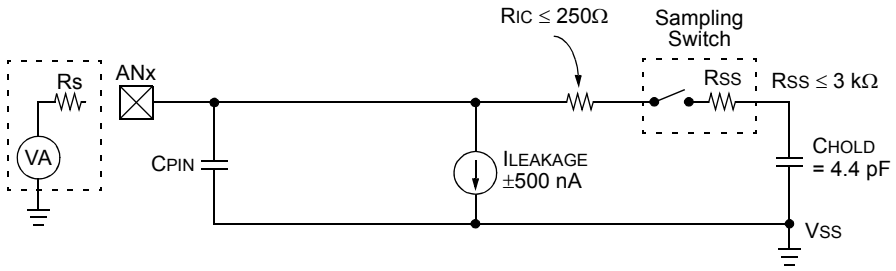
bit 9-8 **ASINT<1:0>:** Auto-Scan (Threshold Detect) Interrupt Mode bits
11 = Interrupt after Threshold Detect sequence has completed and valid compare has occurred
10 = Interrupt after valid compare has occurred
01 = Interrupt after Threshold Detect sequence has completed
00 = No interrupt

bit 7-4 **Unimplemented:** Read as '0'

bit 3-2 **WM<1:0>:** Write Mode bits
11 = Reserved
10 = Auto-compare only (conversion results are not saved, but interrupts are generated when a valid match occurs, as defined by the CMx and ASINTx bits)
01 = Convert and save (conversion results are saved to locations as determined by the register bits when a match occurs, as defined by the CMx bits)
00 = Legacy operation (conversion data is saved to a location determined by the buffer register bits)

bit 1-0 **CM<1:0>:** Compare Mode bits
11 = Outside Window mode (valid match occurs if the conversion result is outside of the window defined by the corresponding buffer pair)
10 = Inside Window mode (valid match occurs if the conversion result is inside the window defined by the corresponding buffer pair)
01 = Greater Than mode (valid match occurs if the result is greater than the value in the corresponding buffer register)
00 = Less Than mode (valid match occurs if the result is less than the value in the corresponding buffer register)

FIGURE 27-3: 10-BIT A/D CONVERTER ANALOG INPUT MODEL



Legend:		
	CPIN	= Input Capacitance
	VT	= Threshold Voltage
	ILEAKAGE	= Leakage Current at the pin due to Various Junctions
	RIC	= Interconnect Resistance
	RSS	= Sampling Switch Resistance
	CHOLD	= Sample/Hold Capacitance (from DAC)

Note: The CPIN value depends on the device package and is not tested. The effect of CPIN is negligible if Rs ≤ 5 kΩ.

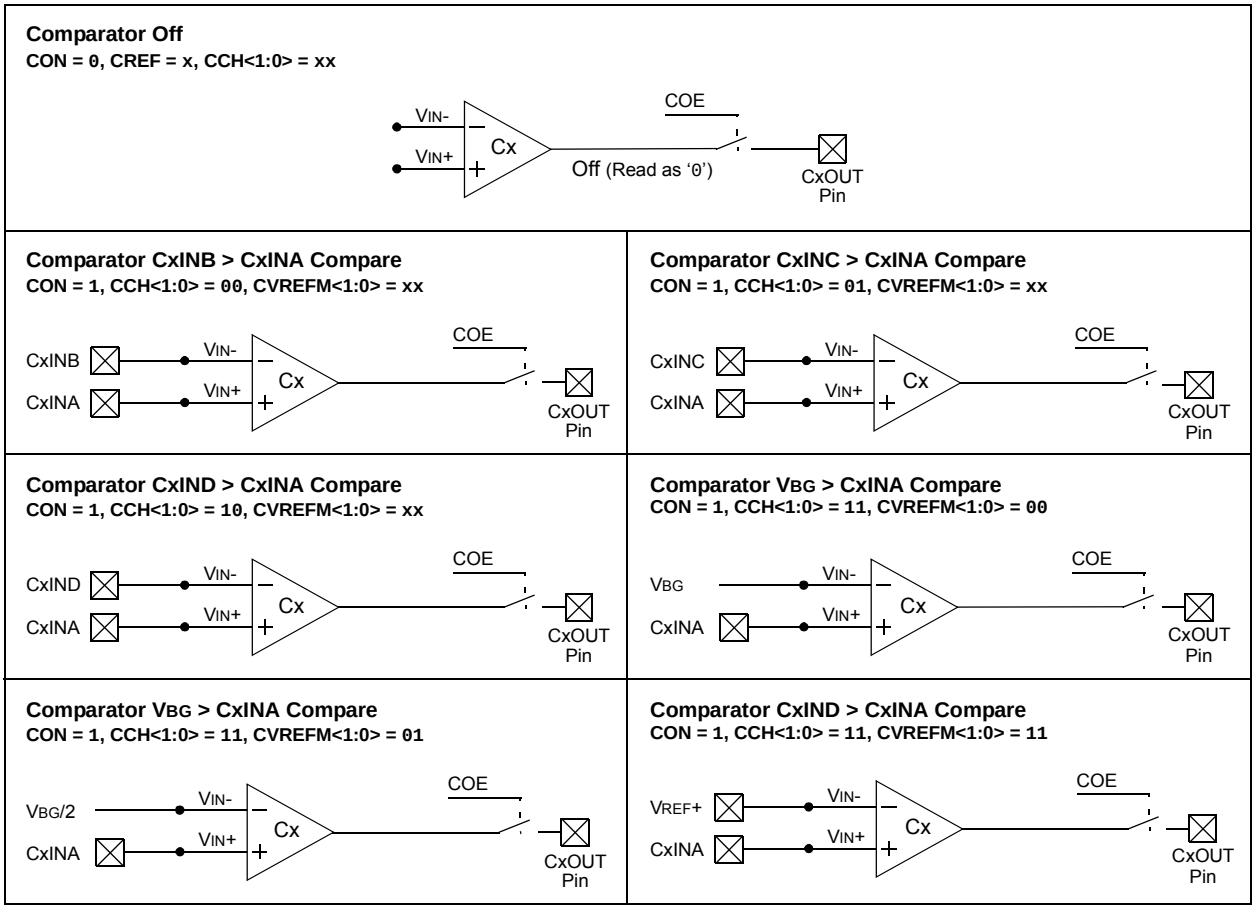
EQUATION 27-1: A/D CONVERSION CLOCK PERIOD

$$T_{AD} = T_{CY}\,(ADCS + 1)$$

$$ADCS = \frac{T_{AD}}{T_{CY}} - 1$$

Note: Based on TCY = 2/FOSC; Doze mode and PLL are disabled.

FIGURE 29-2: INDIVIDUAL COMPARATOR CONFIGURATIONS WHEN CREF = 0



REGISTER 33-10: FDEVOPT1: DEVICE OPTIONS CONFIGURATION WORD

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 15							bit 8

U-1	U-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	U-1
—	—	—	ALTVREF(1)	TMPRWIPE	TMPRPIN	ALTCMPI(2)	—
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-5 **Unimplemented:** Read as '1'

bit 4 **ALTVREF:** Alternate External Voltage Reference Location Select bit(1)
1 = VREF+/CVREF+/DVREF+ and VREF-/CVREF- are mapped to RA10 and RA9, respectively
0 = VREF+/CVREF+/DVREF+ and VREF-/CVREF- are mapped to RB0 and RB1, respectively

bit 3 **TMPRWIPE:** Erase Key RAM on Tamper Event Enable Pin bit
1 = Cryptographic Engine Key RAM is not erased on $\overline{\text{TMPR}}$ pin events
0 = Cryptographic Engine Key RAM is erased when a $\overline{\text{TMPR}}$ pin event is detected

bit 2 **TMPRPIN:** Tamper Pin Disable bit
1 = $\overline{\text{TMPR}}$ pin is disabled
0 = $\overline{\text{TMPR}}$ pin is enabled

bit 1 **ALTCMPI:** Alternate Comparator Input Location Select bit(2)
1 = C1INC, C2INC and C3INC are mapped to their default pin locations
0 = C1INC, C2INC and C3INC are all mapped to RG9

bit 0 **Unimplemented:** Read as '1'

Note 1: Unimplemented on 64-pin devices; maintain this bit as '0' in those devices.
2: Unimplemented in PIC24FJXXXGAXXX devices.

35.0 INSTRUCTION SET SUMMARY

Note: This chapter is a brief summary of the PIC24F Instruction Set Architecture (ISA) and is not intended to be a comprehensive reference source.

The PIC24F instruction set adds many enhancements to the previous PIC® MCU instruction sets, while maintaining an easy migration from previous PIC MCU instruction sets. Most instructions are a single program memory word. Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction. The instruction set is highly orthogonal and is grouped into four basic categories:

- Word or byte-oriented operations
- Bit-oriented operations
- Literal operations
- Control operations

Table 35-1 shows the general symbols used in describing the instructions. The PIC24F instruction set summary in Table 35-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register, ‘Wb’, without any address modifier
- The second source operand, which is typically a register, ‘Ws’, with or without an address modifier
- The destination of the result, which is typically a register, ‘Wd’, with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value, ‘f’
- The destination, which could either be the file register, ‘f’, or the W0 register, which is denoted as ‘WREG’

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of ‘Ws’ or ‘f’)
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register, ‘Wb’)

The literal instructions that involve data movement may use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by the value of ‘k’)
- The W register or file register where the literal value is to be loaded (specified by ‘Wb’ or ‘f’)

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register, ‘Wb’, without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register, ‘Wd’, with or without an address modifier

The control instructions may use some of the following operands:

- A program memory address
- The mode of the Table Read and Table Write instructions

All instructions are a single word, except for certain double-word instructions, which were made double-word instructions so that all the required information is available in these 48 bits. In the second word, the 8 MSbs are ‘0’s. If this second word is executed as an instruction (by itself), it will execute as a NOP.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the Program Counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles, with the additional instruction cycle(s) executed as a NOP. Notable exceptions are the BRA (unconditional/computed branch), indirect CALL/GOTO, all Table Reads and Writes, and RETURN/RETFIE instructions, which are single-word instructions but take two or three cycles.

Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles. The double-word instructions execute in two instruction cycles.

TABLE 36-6: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Operating Temperature**	**VDD**	**Conditions**
Power-Down Current (IPD)						
DC60	3.24	—	µA	-40°C	2.0V	Sleep(2)
	4.08	22	µA	+25°C		
	7.81	—	µA	+60°C		
	23.25	40	µA	+85°C		
	3.20	—	µA	-40°C	3.3V	
	4.07	25	µA	+25°C		
	7.94	—	µA	+60°C		
	19.85	42	µA	+85°C		
DC61	0.07	—	µA	-40°C	2.0V	Low-Voltage Sleep(3)
	0.07	—	µA	+25°C		
	3.54	—	µA	+60°C		
	15.30	—	µA	+85°C		
	0.10	—	µA	-40°C	3.3V	
	0.06	—	µA	+25°C		
	3.68	—	µA	+60°C		
	15.65	—	µA	+85°C		
DC70	120	—	nA	-40°C	2.0V	Deep Sleep, capacitor on VCAP is fully discharged
	80	800	nA	+25°C		
	620	—	nA	+60°C		
	1.13	5	µA	+85°C		
	110	—	nA	-40°C	3.3V	
	110	1500	nA	+25°C		
	830	—	nA	+60°C		
	3.67	10	µA	+85°C		
DC74	0.6	3	µA	-40°C to +85°C	0V	RTCC with VBAT mode (LPRC/SOSC)(4)

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The low-voltage/retention regulator is disabled; RETEN (RCON<12>) = 0, $\overline{\text{LPCFG}}$ (FPOR<2>) = 1.

3: The low-voltage/retention regulator is enabled; RETEN (RCON<12>) = 1, $\overline{\text{LPCFG}}$ (FPOR<2>) = 0.

4: The VBAT pin is connected to the battery and RTCC is running with VDD = 0.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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ISBN: 978-1-5224-1157-4