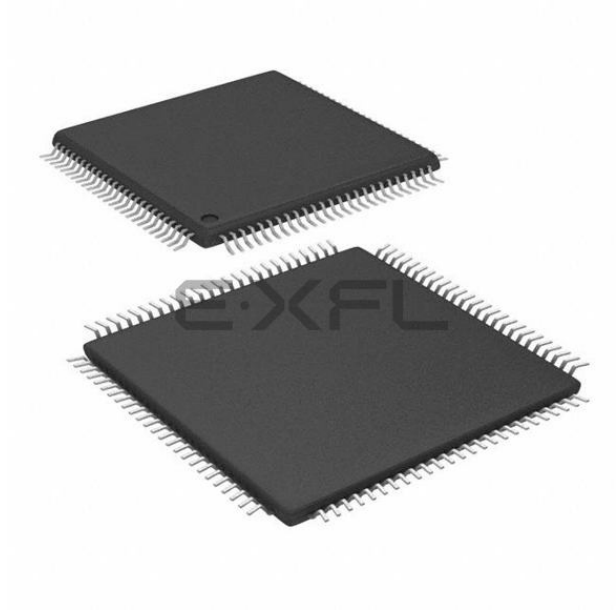
Microchip Technology - PIC24FJ128GA410-I/PT Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128ga410-i-pt

TABLE 4: COMPLETE PIN FUNCTION DESCRIPTIONS FOR PIC24FJXXXGB410 DEVICES

Pin	Function	Pin	Function
1	SEG50/OCM1C/CTED3/IOCG15/RG15	51	SEG12/**RP16**/USBID/IOCF3/RF3
2	VDD	52	SEG40/**RP30**/IOCF2/RF2
3	LCDBIAS2/IC4/CTED4/PMD5/IOCE5/RE5	53	SEG41/**RP15**/IOCF8/RF8
4	LCDBIAS1/SCL3/IC5/PMD6/IOCE6/RE6	54	VBUS/IOCF7/RF7
5	LCDBIAS0/SDA3/IC6/PMD7/IOCE7/RE7	55	VUSB3V3
6	SEG32/**RPI38**/OCM1D/IOCC1/RC1	56	D-/IOCG3/RG3
7	SEG51/**RPI39**/IOCC2/RC2	57	D+/IOCG2/RG2
8	SEG33/**RPI40**/IOCC3/RC3	58	SEG55/SCL2/IOCA2/RA2
9	SEG52/AN16/**RPI41**/PMCS2/IOCC4/RC4	59	SEG56/SDA2/PMA20/IOCA3/RA3
10	SEG0/AN17/C1IND/**RP21**/ICM1/OCM1A/PMA5/IOCG6/RG6	60	TDI/PMA21/IOCA4/RA4
11	VLCAP1/AN18/C1INC/**RP26**/OCM1B/PMA4/IOCG7/RG7	61	TDO/SEG28/IOCA5/RA5
12	VLCAP2/AN19/C2IND/**RP19**/ICM2/OCM2/PMA3/IOCG8/RG8	62	VDD
13	$\overline{\text{MCLR}}$	63	OSCI/CLKI/IOCC12/RC12
14	SEG1/AN20/C1INC/C2INC/C3INC/**RP27**/DAC1/PMA2/PMALU/IOCG9/RG9	64	OSCO/CLKO/IOCC15/RC15
15	VSS	65	VSS
16	VDD	66	SEG42/**RPI36**/SCL1/PMA22/IOCA14/RA14
17	TMS/SEG48/CTED14/IOCA0/RA0	67	SEG43/**RPI35**/SDA1/PMBE1/IOCA15/RA15
18	SEG34/**RPI33**/PMCS1/IOCE8/RE8	68	SEG13/CLC4OUT/**RP2**/RTCC/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/IOCD8/RD8
19	SEG35/AN21/**RPI34**/PMA19/IOCE9/RE9	69	SEG14/**RP4**/PMACK2/IOCD9/RD9
20	PGEC3/SEG2/AN5/C1INA/**RP18**/ICM3/OCM3/IOCB5/RB5	70	SEG15/C3IND/**RP3**/PMA15/APMCS2/IOCD10/RD10
21	PGED3/SEG3/AN4/C1INB/**RP28**/$\overline{\text{USBOEN}}$/IOCB4/RB4	71	SEG16/C3INC/**RP12**/PMA14/PMCS/APMCS1/IOCD11/RD11
22	SEG4/AN3/C2INA/IOCB3/RB3	72	SEG17/CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/IOCD0/RD0
23	SEG5/AN2/CTCMP/C2INB/**RP13**/CTED13/IOCB2/RB2	73	SOSCI/IOCC13/RC13
24	PGEC1/SEG6/VREF-/CVREF-/AN1/AN1-/**RP1**/CTED12/IOCB1/RB1	74	SOSCO/SCLKI/**RPI37**/PWRLCLK/IOCC14/RC14
25	PGED1/SEG7/VREF+/CVREF+/DVREF+/AN0/**RP0**/IOCB0/RB0	75	VSS
26	PGEC2/LCDBIAS3/AN6/**RP6**/IOCB6/RB6	76	SEG20/**RP24**/U5TX/ICM4/IOCD1/RD1
27	PGED2/SEG63/AN7/**RP7**/U6TX/IOCB7/RB7	77	SEG21/**RP23**/PMACK1/IOCD2/RD2
28	SEG36/VREF-/CVREF-/PMA7/IOCA9/RA9	78	SEG22/**RP22**/ICM7/PMBE0/IOCD3/RD3
29	SEG37/VREF+/CVREF+/DVREF+/PMA6/IOCA10/RA10	79	SEG44/**RPI42**/PMD12/IOCD12/RD12
30	AVDD	80	SEG45/PMD13/IOCD13/RD13
31	AVSS	81	SEG23/**RP25**/PMWR/PMENB/IOCD4/RD4
32	COM7/SEG31/AN8/**RP8**/PWRGT/IOCB8/RB8	82	SEG24/**RP20**/PMRD/$\overline{\text{PMWR}}$/IOCD5/RD5
33	COM6/SEG30/AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/IOCB9/RB9	83	SEG25/C3INB/U5RX/OC4/PMD14/IOCD6/RD6
34	COM5/SEG29/CVREF/AN10/SDO4/PMA13/IOCB10/RB10	84	SEG26/C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/PMD15/IOCD7/RD7
35	AN11/REFI1/$\overline{\text{SS4}}$/FSYNC4/PMA12/IOCB11/RB11	85	VCAP
36	VSS	86	VBAT
37	VDD	87	SEG27/$\overline{\text{U5CTS}}$/OC6/PMD11/IOCF0/RF0
38	TCK/IOCA1/RA1	88	COM4/SEG47/SCK4/PMD10/IOCF1/RF1
39	SEG53/**RP31**/IOCF13/RF13	89	SEG46/PMD9/IOCG1/RG1
40	SEG54/**RPI32**/CTED7/PMA18/IOCF12/RF12	90	SEG49/PMD8/IOCG0/RG0
41	SEG18/AN12/U6RX/CTED2/PMA11/IOCB12/RB12	91	SEG57/AN23/OCM1E/IOCA6/RA6
42	SEG19/AN13/SDI4/CTED1/PMA10/IOCB13/RB13	92	SEG58/AN22/OCM1F/PMA17/IOCA7/RA7
43	SEG8/AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/IOCB14/RB14	93	COM3/PMD0/IOCE0/RE0
44	SEG9/AN15/**RP29**/CTED6/PMA0/PMALL/IOCB15/RB15	94	COM2/PMD1/IOCE1/RE1
45	VSS	95	SEG59/CTED11/PMA16/IOCG14/RG14
46	VDD	96	SEG60/IOCG12/RG12
47	SEG38/**RPI43**/IOCD14/RD14	97	SEG61/CTED10/IOCG13/RG13
48	SEG39/**RP5**/IOCD15/RD15	98	COM1/PMD2/IOCE2/RE2
49	SEG10/**RP10**/PMA9/IOCF4/RF4	99	COM0/CTED9/PMD3/IOCE3/RE3
50	SEG11/**RP17**/PMA8/IOCF5/RF5	100	SEG62/LVDIN/CTED8/PMD4/IOCE4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

© 2015-2016 Microchip Technology Inc.

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
AN0	16	25	K2	I	ANA	A/D Analog Inputs
AN1	15	24	K1	I	ANA	
AN1-	15	24	K1	I	ANA	
AN2	14	23	J2	I	ANA	
AN3	13	22	J1	I	ANA	
AN4	12	21	H2	I	ANA	
AN5	11	20	H1	I	ANA	
AN6	17	26	L1	I	ANA	
AN7	18	27	J3	I	ANA	
AN8	21	32	K4	I	ANA	
AN9	22	33	L4	I	ANA	
AN10	23	34	H5	I	ANA	
AN11	24	35	K5	I	ANA	
AN12	27	41	J7	I	ANA	
AN13	28	42	L7	I	ANA	
AN14	29	43	K7	I	ANA	
AN15	30	44	L8	I	ANA	
AN16	—	9	E1	I	ANA	
AN17	—	10	E3	I	ANA	
AN18	—	11	F4	I	ANA	
AN19	—	12	F2	I	ANA	
AN20	—	14	F3	I	ANA	
AN21	—	19	G2	I	ANA	
AN22	—	92	E11	I	ANA	
AN23	—	91	E10	I	ANA	
AVDD	19	30	J4	P	—	Positive Supply for Analog modules
AVSS	20	31	L3	P	—	Ground Reference for Analog modules
C1INA	11	20	H1	I	ANA	Comparator 1 Input A
C1INB	12	21	H2	I	ANA	Comparator 1 Input B
C1INC	5,8	11,14	F4,F3	I	ANA	Comparator 1 Input C
C1IND	4	10	E3	I	ANA	Comparator 1 Input D
C2INA	13	22	J1	I	ANA	Comparator 2 Input A
C2INB	14	23	J2	I	ANA	Comparator 2 Input B
C2INC	8	14	F3	I	ANA	Comparator 2 Input C
C2IND	6	12	F2	I	ANA	Comparator 2 Input D
C3INA	55	84	C7	I	ANA	Comparator 3 Input A
C3INB	54	83	D7	I	ANA	Comparator 3 Input B
C3INC	8,45	14,71	F3,C11	I	ANA	Comparator 3 Input C
C3IND	44	70	D11	I	ANA	Comparator 3 Input D
CLC3OUT	46	72	D9	O	DIG	CLC3 Output
CLC4OUT	42	68	E9	O	DIG	CLC4 Output

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
RPI32	—	40	K6	I	ST	Remappable Peripherals (Input only)
RPI33	—	18	G1	I	ST	
RPI34	—	19	G2	I	ST	
RPI35	—	67	E8	I	ST	
RPI36	—	66	E11	I	ST	
RPI37	48	74	B11	I	ST	
RPI38	—	6	D1	I	ST	
RPI39	—	7	E4	I	ST	
RPI40	—	8	E2	I	ST	
RPI41	—	9	E1	I	ST	
RPI42	—	79	A9	I	ST	
RPI43	—	47	L9	I	ST	
RTCC	42	68	E9	O	DIGMV	Real-Time Clock Alarm/Seconds Pulse Output
SCK4	59	88	A6	I/O	DIG/ST	SPI4 Clock
SCL1	37	57	H10	I/O	DIG/I^2C/SMB	I2C1 Synchronous Serial Clock Input/Output
SCL2	32	58	H11	I/O	DIG/I^2C/SMB	I2C2 Synchronous Serial Clock Input/Output
SCL3	2	4	C1	I/O	DIG/I^2C/SMB	I2C3 Synchronous Serial Clock Input/Output
SDA1	36	56	J11	I/O	DIG/I^2C/SMB	I2C1 Data Input/Output
SDA2	31	59	G10	I/O	DIG/I^2C/SMB	I2C2 Data Input/Output
SDA3	3	5	D2	I/O	DIG/I^2C/SMB	I2C3 Data Input/Output
SDI4	28	42	L7	I	ST	SPI4 Data Input
SDO4	23	34	H5	O	DIG	SPI4 Data Output

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

© 2015-2016 Microchip Technology Inc.

TABLE 1-5: PIC24FJ256GB412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
IOCC1	—	6	D1	I	ST	PORTC Interrupt-on-Change
IOCC2	—	7	E4	I	ST	
IOCC3	—	8	E2	I	ST	
IOCC4	—	9	E!	I	ST	
IOCC12	39	63	F9	I	ST	
IOCC13	47	73	C10	I	ST	
IOCC14	48	74	B11	I	ST	
IOCC15	40	64	F11	I	ST	
IOCD0	46	72	D9	I	ST	PORTD Interrupt-on-Change
IOCD1	49	76	A11	I	ST	
IOCD2	50	77	A10	I	ST	
IOCD3	51	78	B9	I	ST	
IOCD4	52	81	C8	I	ST	
IOCD5	53	82	B8	I	ST	
IOCD6	54	83	D7	I	ST	
IOCD7	55	84	C7	I	ST	
IOCD8	42	68	E9	I	ST	
IOCD9	43	69	E10	I	ST	
IOCD10	44	70	D11	I	ST	
IOCD11	45	71	C11	I	ST	
IOCD12	—	79	A9	I	ST	
IOCD13	—	80	D8	I	ST	
IOCD14	—	47	L9	I	ST	
IOCD15	—	48	K9	I	ST	
IOCE0	60	93	A4	I	ST	PORTE Interrupt-on-Change
IOCE1	61	94	B4	I	ST	
IOCE2	62	98	B3	I	ST	
IOCE3	63	99	A2	I	ST	
IOCE4	64	100	A1	I	ST	
IOCE5	1	3	D3	I	ST	
IOCE6	2	4	C1	I	ST	
IOCE7	3	5	D2	I	ST	
IOCE8	—	18	G1	I	ST	
IOCE9	—	19	G2	I	ST	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

2.6 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency Primary Oscillator and a low-frequency Secondary Oscillator (refer to **Section 9.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

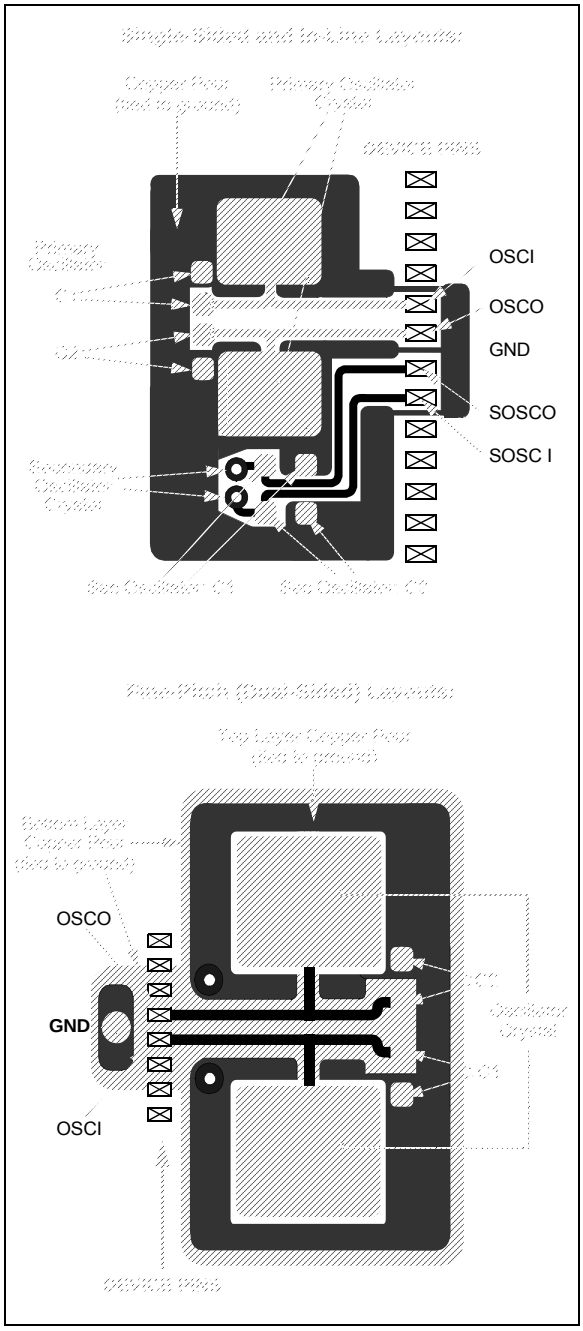
Layout suggestions are shown in Figure 2-5. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

In planning the application's routing and I/O assignments, ensure that adjacent port pins, and other signals in close proximity to the oscillator, are benign (i.e., free of high frequencies, short rise and fall times, and other similar noise).

For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate web site (www.microchip.com):

- *AN943, "Practical PICmicro® Oscillator Analysis and Design"*
- *AN949, "Making Your Oscillator Work"*
- *AN1798, "Crystal Selection for Low-Power Secondary Oscillator"*

FIGURE 2-5: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



REGISTER 8-15: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U2TXIE	U2RXIE	INT2IE(1)	T5IE	T4IE	OC4IE	OC3IE	DMA2IE
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CCP6IE	CCP5IE	—	INT1IE(1)	CNIE	CMIE	MI2C1IE	SI2C1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **U2TXIE:** UART2 Transmitter Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 14 **U2RXIE:** UART2 Receiver Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13 **INT2IE:** External Interrupt 2 Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12 **T5IE:** Timer5 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 11 **T4IE:** Timer4 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 10 **OC4IE:** Output Compare Channel 4 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 9 **OC3IE:** Output Compare Channel 3 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 8 **DMA2IE:** DMA Channel 2 Interrupt Flag Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 7 **CCP6IE:** SCCP6 Capture/Compare Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 6 **CCP5IE:** SCCP5 Capture/Compare Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **INT1IE:** External Interrupt 1 Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

Note 1: If an external interrupt is enabled, the interrupt input must also be configured to an available RPn or RPIn pin. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

REGISTER 8-50: IPC28: INTERRUPT PRIORITY CONTROL REGISTER 28

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U6TXIP2	U6TXIP1	U6TXIP0	—	U6RXIP2	U6RXIP1	U6RXIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U5ERIP2	U5ERIP1	U5ERIP0	—	U5TXIP2	U5TXIP1	U5TXIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **U6TXIP<2:0>:** UART6 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **U6RXIP<2:0>:** UART6 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **U5ERIP<2:0>:** UART5 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **U5TXIP<2:0>:** UART5 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

© 2015-2016 Microchip Technology Inc.

REGISTER 10-8: PMD5: PERIPHERAL MODULE DISABLE REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CCP7MD	CCP6MD	CCP5MD	CCP4MD	CCP3MD	CCP2MD	CCP1MD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **CCP7MD:** SCCP7 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 5 **CCP6MD:** SCCP6 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 4 **CCP5MD:** SCCP5 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 3 **CCP4MD:** SCCP4 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 2 **CCP3MD:** SCCP3 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 1 **CCP2MD:** SCCP2 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 0 **CCP1MD:** MCCP1 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

© 2015-2016 Microchip Technology Inc.

11.3 I/O Ports Register Maps

TABLE 11-2: PORTA REGISTER MAP(1)

Register Name	Bit Range	Bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANSA	15:0	ANSA<15:14>		—	—	—	ANSA<10:9>		—	ANSA<7:5>			—	ANSA<3:2>		—	ANSA0
TRISA	15:0	TRISA<15:0>															
PORTA	15:0	PORTA<15:0>															
LATA	15:0	LATA<15:0>															
ODCA	15:0	ODCA<15:0>															
IOCPA	15:0	IOCPA<15:14>		—	—	—	IOCPA<10:9>		—	IOCPA<7:0>							
IOCNA	15:0	IOCNA<15:14>		—	—	—	IOCNA<10:9>		—	IOCNA<7:0>							
IOCFA	15:0	IOCFA<15:14>		—	—	—	IOCFA<10:9>		—	IOCFA<7:0>							
IOCPUA	15:0	IOCPUA<15:14>		—	—	—	IOCPUA<10:9>		—	IOCPUA<7:0>							
IOCPDA	15:0	IOCPDA<15:14>		—	—	—	IOCPDA<10:9>		—	IOCPDA<7:0>							

Legend: — = unimplemented, read as '0'.

Note 1: PORT register maps show full pin count devices. Please refer to Table 1-4 and Table 1-5 for pin count-specific PORT I/O implementation.

TABLE 11-3: PORTB REGISTER MAP(1)

Register Name	Bit Range	Bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANSB	15:0	ANSB<15:0>															
TRISB	15:0	TRISB<15:0>															
PORTB	15:0	PORTB<15:0>															
LATB	15:0	LATB<15:0>															
ODCB	15:0	ODCB<15:0>															
IOCPB	15:0	IOCPB<15:0>															
IOCNB	15:0	IOCNB<15:0>															
IOCFB	15:0	IOCFB<15:0>															
IOCPUB	15:0	IOCPUB<15:0>															
IOCPDB	15:0	IOCPDB<15:0>															

Legend: — = unimplemented, read as '0'.

Note 1: PORT register maps show full pin count devices. Please refer to Table 1-4 and Table 1-5 for pin count-specific PORT I/O implementation.

© 2015-2016 Microchip Technology Inc.

REGISTER 11-17: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SCK2R5	SCK2R4	SCK2R3	SCK2R2	SCK2R1	SCK2R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SDI2R5	SDI2R4	SDI2R3	SDI2R2	SDI2R1	SDI2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **SCK2R<5:0>:** Assign SPI2 Clock Input (SCK2IN) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **SDI2R<5:0>:** Assign SPI2 Data Input (SDI2) to Corresponding RPn or RPIn Pin bits

REGISTER 11-18: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	TXCKR5	TXCKR4	TXCKR3	TXCKR2	TXCKR1	TXCKR0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SS2R5	SS2R4	SS2R3	SS2R2	SS2R1	SS2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **TXCKR<5:0>:** Assign General Timer External Input (TMRCK) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **SS2R<5:0>:** Assign SPI2 Slave Select Input (SS2IN) to Corresponding RPn or RPIn Pin bits

NOTES:

© 2015-2016 Microchip Technology Inc.

REGISTER 14-5: CCPxCON3L: CCPx CONTROL 3 LOW REGISTERS(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DT<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **DT<5:0>:** CCPx Dead-Time Select bits

111111 = Inserts 63 dead-time delay periods between complementary output signals
111110 = Inserts 62 dead-time delay periods between complementary output signals
. . .
000010 = Inserts 2 dead-time delay periods between complementary output signals
000001 = Inserts 1 dead-time delay period between complementary output signals
000000 = Dead-time logic is disabled

Note 1: This register is implemented in MCCPx modules only.

REGISTER 16-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Trigger/Synchronization Source Selection bits
11111 = This OC module(1)
11110 = OCTRIG1 external input
11101 = OCTRIG2 external input
11100 = CTMU(2)
11011 = A/D(2)
11010 = Comparator 3(2)
11001 = Comparator 2(2)
11000 = Comparator 1(2)
10111 = SCCP5 capture/compare
10110 = SCCP4 capture/compare
10101 = SCCP3 capture/compare
10100 = SCCP2 capture/compare
10011 = MCCP1 capture/compare
10010 = Input Capture 3(2)
10001 = Input Capture 2(2)
10000 = Input Capture 1(2)
01111 = SCCP7 capture/compare
01110 = SCCP6 capture/compare
01101 = Timer3
01100 = Timer2
01011 = Timer1
01010 = SCCP7 sync/trigger
01001 = SCCP6 sync/trigger
01000 = SCCP5 sync/trigger
00111 = SCCP4 sync/trigger
00110 = SCCP3 sync/trigger
00101 = SCCP2 sync/trigger
00100 = MCCP1 sync/trigger
00011 = Output Compare 5(1)
00010 = Output Compare 3(1)
00001 = Output Compare 1(1)
00000 = Not synchronized to any other module

Note 1: Never use an OCx module as its own trigger source, either by selecting this mode or another equivalent SYNCSELx setting.
2: Use these inputs as trigger sources only and never as sync sources.
3: The DCB<1:0> bits are double-buffered in PWM modes only (OCM<2:0> (OCxCON1<2:0>) = 111, 110).

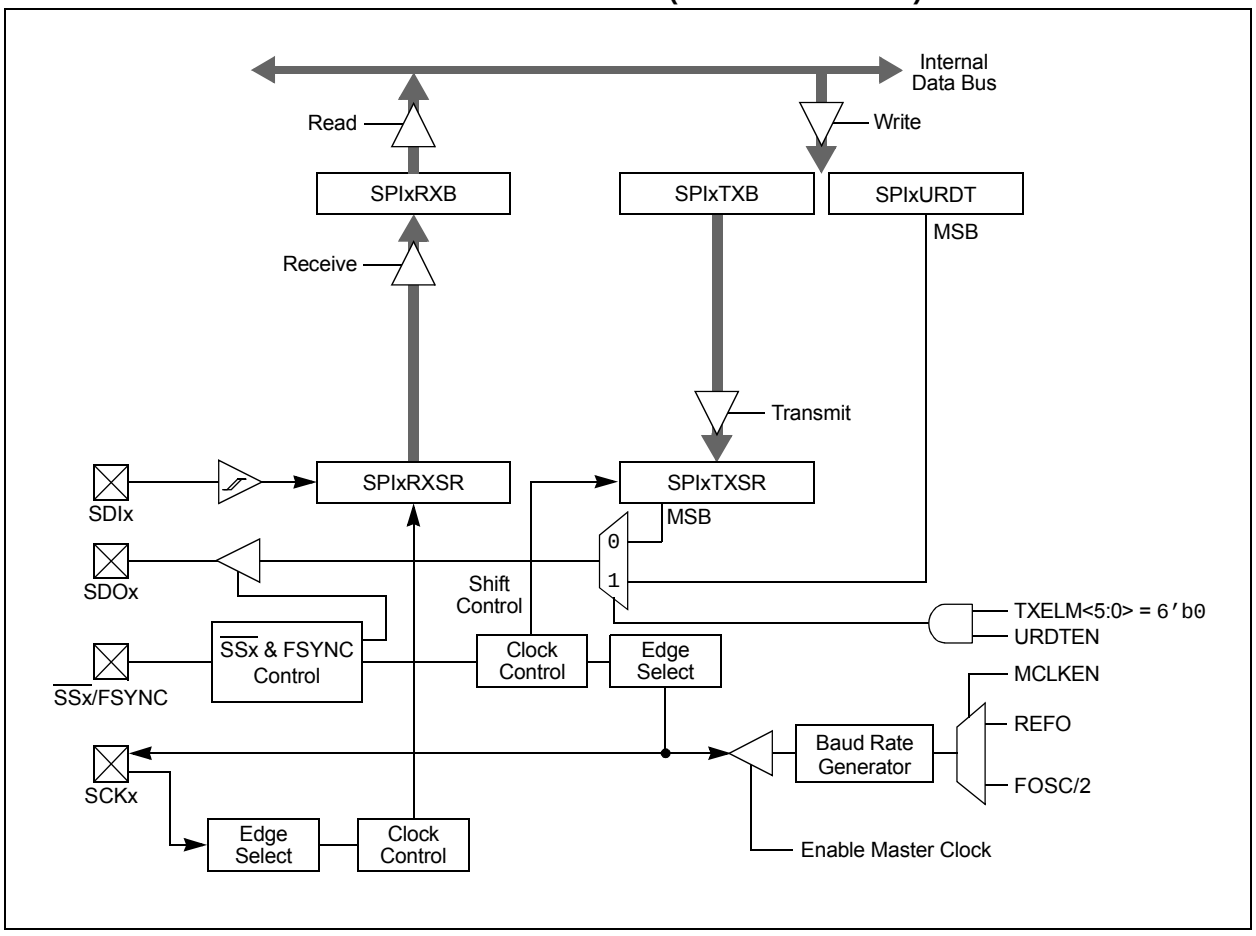
To set up the SPIx module for the Standard Master mode of operation:

1. If using interrupts:
   a) Clear the interrupt flag bits in the respective IFSx register.
   b) Set the interrupt enable bits in the respective IECx register.
   c) Write the SPIxIP bits in the respective IPCx register to set the interrupt priority.
2. Write the desired settings to the SPIxCON1L and SPIxCON1H registers with the MSTEN bit (SPIxCON1L<5>) = 1.
3. Clear the SPIROV bit (SPIxSTATL<6>).
4. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).
5. Write the data to be transmitted to the SPIxBUFL and SPIxBUFH registers. Transmission (and reception) will start as soon as data is written to the SPIxBUFL and SPIxBUFH registers.

To set up the SPIx module for the Standard Slave mode of operation:

1. Clear the SPIxBUF registers.
2. If using interrupts:
   a) Clear the SPIxBUFL and SPIxBUFH registers.
   b) Set the interrupt enable bits in the respective IECx register.
   c) Write the SPIxIP bits in the respective IPCx register to set the interrupt priority.
3. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with the MSTEN bit (SPIxCON1L<5>) = 0.
4. Clear the SMP bit.
5. If the CKE bit (SPIxCON1L<8>) is set, then the SSEN bit (SPIxCON1L<7>) must be set to enable the $\overline{SSx}$ pin.
6. Clear the SPIROV bit (SPIxSTATL<6>).
7. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).

FIGURE 17-1: SPIx MODULE BLOCK DIAGRAM (STANDARD MODE)



© 2015-2016 Microchip Technology Inc.

REGISTER 20-8: U1CON: USB CONTROL REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-x, HSC	R-x, HSC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
JSTATE	SE0	TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST	SOFEN
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **JSTATE:** Live Differential Receiver J-State Flag bit
- 1 = J-state (differential '0' in low speed, differential '1' in full speed) is detected on the USB
- 0 = No J-state is detected

bit 6 **SE0:** Live Single-Ended Zero Flag bit
- 1 = Single-ended zero is active on the USB bus
- 0 = No single-ended zero is detected

bit 5 **TOKBUSY:** Token Busy Status bit
- 1 = Token is being executed by the USB module in On-The-Go state
- 0 = No token is being executed

bit 4 **USBRST:** USB Module Reset bit
- 1 = USB Reset has been generated for a software Reset; application must set this bit for 50 ms, then clear it
- 0 = USB Reset is terminated

bit 3 **HOSTEN:** Host Mode Enable bit
- 1 = USB host capability is enabled; pull-downs on D+ and D- are activated in hardware
- 0 = USB host capability is disabled

bit 2 **RESUME:** Resume Signaling Enable bit
- 1 = Resume signaling is activated; software must set bit for 10 ms and then clear to enable remote wake-up
- 0 = Resume signaling is disabled

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
- 1 = Resets all Ping-Pong Buffer Pointers to the even BD banks
- 0 = Ping-Pong Buffer Pointers are not reset

bit 0 **SOFEN:** Start-of-Frame Enable bit
- 1 = Start-of-Frame token is sent every one 1 ms
- 0 = Start-of-Frame token is disabled

TABLE 21-2: ENHANCED PARALLEL MASTER PORT PIN DESCRIPTIONS

Pin Name (Alternate Function)	Type	Description
PMA<22:16>	O	Address Bus bits<22:16>
PMA15	O	Address Bus bit 15
	I/O	Data Bus bit 15 (16-bit port with Multiplexed Addressing)
(APMCS2)	O	Chip Select 2 (alternate location)
PMA14	O	Address Bus bit 14
	I/O	Data Bus bit 14 (16-bit port with Multiplexed Addressing)
(APMCS1)	O	Chip Select 1 (alternate location)
PMA<13:8>	O	Address Bus bits<13:8>
	I/O	Data Bus bits<13:8> (16-bit port with Multiplexed Addressing)
PMA<7:3>	O	Address Bus bits<7:3>
PMA2	O	Address Bus bit 2
(PMALU)	O	Address Latch Upper Strobe for Multiplexed Address
PMA1	I/O	Address Bus bit 1
(PMALH)	O	Address Latch High Strobe for Multiplexed Address
PMA0	I/O	Address Bus bit 0
(PMALL)	O	Address Latch Low Strobe for Multiplexed Address
PMD<15:8>	I/O	Data Bus bits<15:8> (Demultiplexed Addressing)
PMD<7:4>	I/O	Data Bus bits<7:4>
	O	Address Bus bits<7:4> (4-bit port with 1-Phase Multiplexed Addressing)
PMD<3:0>	I/O	Data Bus bits<3:0>
(1)	I/O	Chip Select 1
(1)	O	Chip Select 2
PMWR	I/O	Write Strobe**(2)**
(PMENB)	I/O	Enable Signal**(2)**
PMRD	I/O	Read Strobe**(2)**
(PMRD/$\overline{\text{PMWR}}$)	I/O	Read/$\overline{\text{Write}}$ Signal**(2)**
PMBE1	O	Byte Indicator
PMBE0	O	Nibble or Byte Indicator
PMACK1	I	Acknowledgment Signal 1
PMACK2	I	Acknowledgment Signal 2

2: Signal function depends on the setting of the MODE<1:0> and SM bits (PMCON1<9:8> and PMCSxCF<8>).

© 2015-2016 Microchip Technology Inc.

REGISTER 33-10: FDEVOPT1: DEVICE OPTIONS CONFIGURATION WORD

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 15							bit 8

U-1	U-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	U-1
—	—	—	ALTVREF(1)	TMPRWIPE	TMPRPIN	ALTCMPI(2)	—
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-5 **Unimplemented:** Read as '1'

bit 4 **ALTVREF:** Alternate External Voltage Reference Location Select bit(1)
1 = VREF+/CVREF+/DVREF+ and VREF-/CVREF- are mapped to RA10 and RA9, respectively
0 = VREF+/CVREF+/DVREF+ and VREF-/CVREF- are mapped to RB0 and RB1, respectively

bit 3 **TMPRWIPE:** Erase Key RAM on Tamper Event Enable Pin bit
1 = Cryptographic Engine Key RAM is not erased on $\overline{\text{TMPR}}$ pin events
0 = Cryptographic Engine Key RAM is erased when a $\overline{\text{TMPR}}$ pin event is detected

bit 2 **TMPRPIN:** Tamper Pin Disable bit
1 = $\overline{\text{TMPR}}$ pin is disabled
0 = $\overline{\text{TMPR}}$ pin is enabled

bit 1 **ALTCMPI:** Alternate Comparator Input Location Select bit(2)
1 = C1INC, C2INC and C3INC are mapped to their default pin locations
0 = C1INC, C2INC and C3INC are all mapped to RG9

bit 0 **Unimplemented:** Read as '1'

Note 1: Unimplemented on 64-pin devices; maintain this bit as '0' in those devices.
2: Unimplemented in PIC24FJXXXGAXXX devices.

TABLE 36-25: RESET AND BROWN-OUT RESET REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
SY10	TMCL	$\overline{\text{MCLR}}$ Pulse Width (Low)	2	—	—	μs	
SY12	TPOR	Power-on Reset Delay	—	2	—	μs	
SY13	TIOZ	I/O High-Impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	Lesser of: (3 TCY + 2) or 700	—	(3 TCY + 2)	μs	
SY25	TBOR	Brown-out Reset Pulse Width	1	—	—	μs	VDD ≤ VBOR
SY45	TRST	Internal State Reset Time	—	50	—	μs	
SY70	TDSWU	Deep Sleep Wake-up Time	—	200	—	μs	VCAP fully discharged before wake-up
SY71	TPM	Program Memory Wake-up Time	—	20	—	μs	Sleep wake-up with PMSLP = 0
			—	1	—	μs	Sleep wake-up with PMSLP = 1
SY72	TLVR	Low-Voltage Regulator Wake-up Time	—	90	—	μs	Sleep wake-up with PMSLP = 0
			—	70	—	μs	Sleep wake-up with PMSLP = 1

© 2015-2016 Microchip Technology Inc.

TABLE 36-39: A/D MODULE SPECIFICATIONS

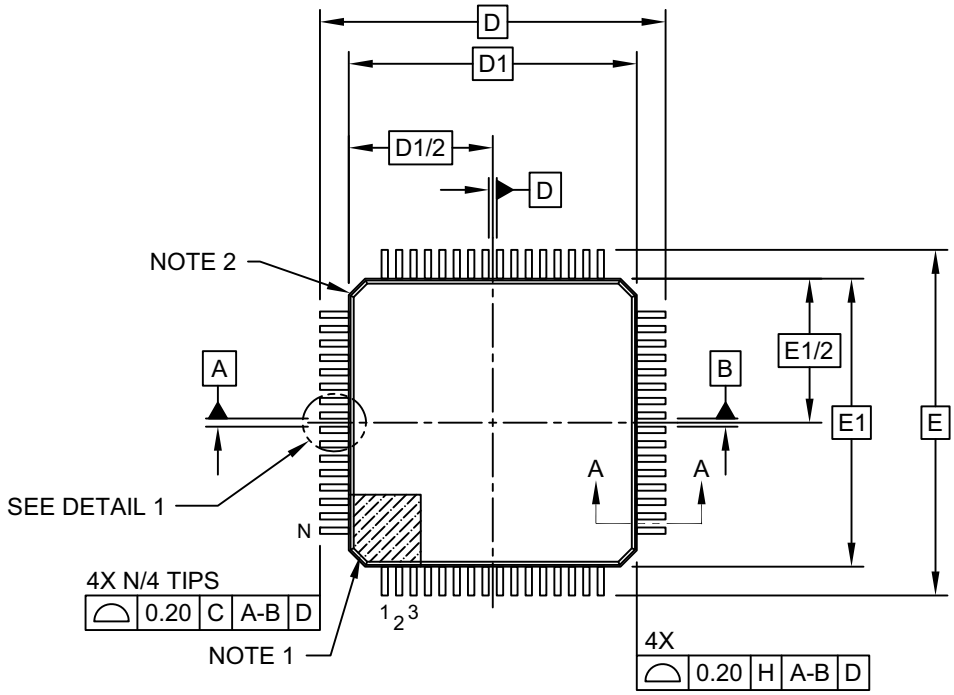
AC CHARACTERISTICS			Standard Operating Conditions: 2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of: VDD – 0.3 or 2.2	—	Lesser of: VDD + 0.3 or 3.6	V	
AD02	AVSS	Module VSS Supply	VSS – 0.3	—	VSS + 0.3	V	
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 1.7	—	AVDD	V	
AD06	VREFL	Reference Voltage Low	AVSS	—	AVDD – 1.7	V	
AD07	VREF	Absolute Reference Voltage	AVSS – 0.3	—	AVDD + 0.3	V	
Analog Input							
AD10	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	**(Note 2)**
AD11	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	
AD12	VINL	Absolute VINL Input Voltage	AVSS – 0.3	—	AVDD/3	V	
AD13		Leakage Current	—	±1.0	±610	nA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V, Source Impedance = 2.5 kΩ
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	2.5K	Ω	10-bit
Accuracy							
AD20B	Nr	Resolution	—	12	—	bits	
AD21B	INL	Integral Nonlinearity	—	±1	<±2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V
AD22B	DNL	Differential Nonlinearity	—	—	<±1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V
AD23B	GERR	Gain Error	—	±1	±3	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V
AD24B	EOFF	Offset Error	—	±1	±2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V
AD25B		Monotonicity(1)	—	—	—	—	Guaranteed

Note 1: The conversion result never decreases with an increase in the input voltage and has no missing codes.

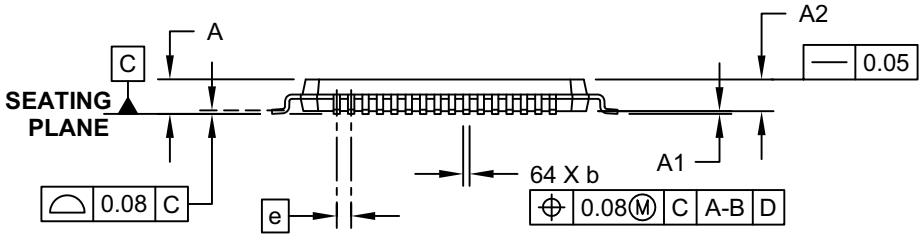
2: Measurements are taken with the external VREF+ and VREF- used as the voltage reference.

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

Microchip Technology Drawing C04-085C Sheet 1 of 2

© 2015-2016 Microchip Technology Inc.