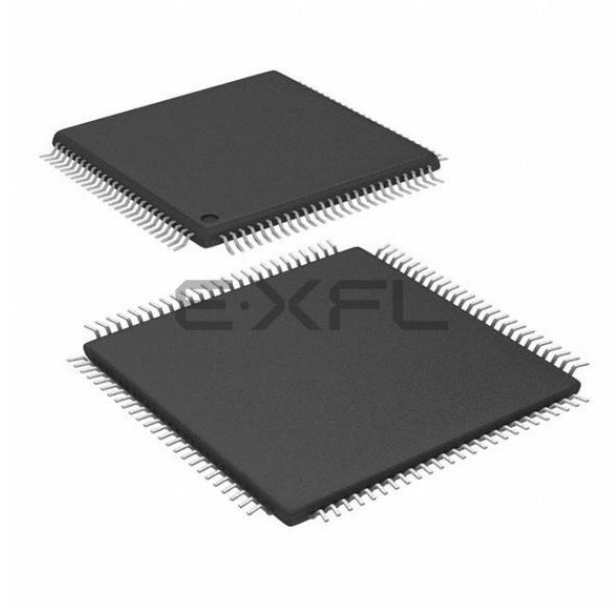

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128ga410t-i-pt

TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS FOR PIC24FJXXXGA410 DEVICES

Pin	Function	Pin	Function
1	SEG50/OCM1C/CTED3/IOCG15/RG15	51	SEG12/**RP16**/IOCF3/RF3
2	VDD	52	SEG40/**RP30**/IOCF2/RF2
3	LCDBIAS2/IC4/CTED4/PMD5/IOCE5/RE5	53	SEG41/**RP15**/IOCF8/RF8
4	LCDBIAS1/SCL3/IC5/PMD6/IOCE6/RE6	54	IOCF7/RF7
5	LCDBIAS0/SDA3/IC6/PMD7/IOCE7/RE7	55	IOCF6/RF6
6	SEG32/**RPI38**/OCM1D/IOCC1/RC1	56	SDA1/IOCG3/RG3
7	SEG51/**RPI39**/IOCC2/RC2	57	SCL1/IOCG2/RG2
8	SEG33/**RPI40**/IOCC3/RC3	58	SEG55/SCL2/IOCA2/RA2
9	SEG52/AN16/**RPI41**/PMCS2/IOCC4/RC4	59	SEG56/SDA2/PMA20/IOCA3/RA3
10	SEG0/AN17/C1IND/**RP21**/ICM1/OCM1A/PMA5/IOCG6/RG6	60	TDI/PMA21/IOCA4/RA4
11	VLCAP1/AN18/C1INC/**RP26**/OCM1B/PMA4/IOCG7/RG7	61	TDO/SEG28/IOCA5/RA5
12	VLCAP2/AN19/C2IND/**RP19**/ICM2/OCM2/PMA3/IOCG8/RG8	62	VDD
13	$\overline{\text{MCLR}}$	63	OSCI/CLKI/IOCC12/RC12
14	SEG1/AN20/C1INC/C2INC/C3INC/**RP27**/DAC1/PMA2/PMALU/IOCG9/RG9	64	OSCO/CLKO/IOCC15/RC15
15	VSS	65	VSS
16	VDD	66	SEG42/**RPI36**/SCL1/PMA22/IOCA14/RA14
17	TMS/SEG48/CTED14/IOCA0/RA0	67	SEG43/**RPI35**/SDA1/PMBE1/IOCA15/RA15
18	SEG34/**RPI33**/PMCS1/IOCE8/RE8	68	SEG13/CLC4OUT/**RP2**/RTCC/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/IOCD8/RD8
19	SEG35/AN21/**RPI34**/PMA19/IOCE9/RE9	69	SEG14/**RP4**/PMACK2/IOCD9/RD9
20	PGEC3/SEG2/AN5/C1INA/**RP18**/ICM3/OCM3/IOCB5/RB5	70	SEG15/C3IND/**RP3**/PMA15/APMCS2/IOCD10/RD10
21	PGED3/SEG3/AN4/C1INB/**RP28**/IOCB4/RB4	71	SEG16/C3INC/**RP12**/PMA14/PMCS/APMCS1/IOCD11/RD11
22	SEG4/AN3/C2INA/IOCB3/RB3	72	SEG17/CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/IOCD0/RD0
23	SEG5/AN2/CTCMP/C2INB/**RP13**/CTED13/IOCB2/RB2	73	SOSCI/IOCC13/RC13
24	PGEC1/SEG6/VREF-/CVREF-/AN1/AN1-/**RP1**/CTED12/IOCB1/RB1	74	SOSCO/SCLKI/**RPI37**/PWRLCLK/IOCC14/RC14
25	PGED1/SEG7/VREF+/CVREF+/DVREF+/AN0/**RP0**/IOCB0/RB0	75	VSS
26	PGEC2/LCDBIAS3/AN6/**RP6**/IOCB6/RB6	76	SEG20/**RP24**/U5TX/ICM4/IOCD1/RD1
27	PGED2/SEG63/AN7/**RP7**/U6TX/IOCB7/RB7	77	SEG21/**RP23**/PMACK1/IOCD2/RD2
28	SEG36/VREF-/CVREF-/PMA7/IOCA9/RA9	78	SEG22/**RP22**/ICM7/PMBE0/IOCD3/RD3
29	SEG37/VREF+/CVREF+/DVREF+/PMA6/IOCA10/RA10	79	SEG44/**RPI42**/PMD12/IOCD12/RD12
30	AVDD	80	SEG45/PMD13/IOCD13/RD13
31	AVSS	81	SEG23/**RP25**/PMWR/PMENB/IOCD4/RD4
32	COM7/SEG31/AN8/**RP8**/PWRGT/IOCB8/RB8	82	SEG24/**RP20**/PMRD/$\overline{\text{PMWR}}$/IOCD5/RD5
33	COM6/SEG30/AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/IOCB9/RB9	83	SEG25/C3INB/U5RX/OC4/PMD14/IOCD6/RD6
34	COM5/SEG29/CVREF/AN10/SDO4/PMA13/IOCB10/RB10	84	SEG26/C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/PMD15/IOCD7/RD7
35	AN11/REFI1/$\overline{\text{SS4}}$/FSYNC4/PMA12/IOCB11/RB11	85	VCAP
36	VSS	86	VBAT
37	VDD	87	SEG27/$\overline{\text{U5CTS}}$/OC6/PMD11/IOCF0/RF0
38	TCK/IOCA1/RA1	88	COM4/SEG47/SCK4/PMD10/IOCF1/RF1
39	SEG53/**RP31**/IOCF13/RF13	89	SEG46/PMD9/IOCG1/RG1
40	SEG54/**RPI32**/CTED7/PMA18/IOCF12/RF12	90	SEG49/PMD8/IOCG0/RG0
41	SEG18/AN12/U6RX/CTED2/PMA11/IOCB12/RB12	91	SEG57/AN23/OCM1E/IOCA6/RA6
42	SEG19/AN13/SDI4/CTED1/PMA10/IOCB13/RB13	92	SEG58/AN22/OCM1F/PMA17/IOCA7/RA7
43	SEG8/AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/IOCB14/RB14	93	COM3/PMD0/IOCE0/RE0
44	SEG9/AN15/**RP29**/CTED6/PMA0/PMALL/IOCB15/RB15	94	COM2/PMD1/IOCE1/RE1
45	VSS	95	SEG59/CTED11/PMA16/IOCG14/RG14
46	VDD	96	SEG60/IOCG12/RG12
47	SEG38/**RPI43**/IOCD14/RD14	97	SEG61/CTED10/IOCG13/RG13
48	SEG39/**RP5**/IOCD15/RD15	98	COM1/PMD2/IOCE2/RE2
49	SEG10/**RP10**/PMA9/IOCF4/RF4	99	COM0/CTED9/PMD3/IOCE3/RE3
50	SEG11/**RP17**/PMA8/IOCF5/RF5	100	SEG62/LVDIN/CTED8/PMD4/IOCE4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

TABLE 1-3: DEVICE FEATURES FOR THE PIC24FJ256GA412/GB412 FAMILY: 121-PIN

Features	PIC24FJXXXGA/GB412					
	64GA	128GA	256GA	64GB	128GB	256GB
Operating Frequency	DC – 32 MHz					
Program Memory (bytes)	64K	128K	256K	64K	128K	256K
Program Memory (instructions)	22,016	44,032	88,064	22,016	44,032	88,064
Data Memory (bytes)	8K	16K		8K	16K	
Interrupt Sources (soft vectors/ NMI traps)	113 (107/6)					
I/O Ports	Ports A, B, C, D, E, F, G, H, J					
Total I/O Pins	102			101		
Remappable Pins	44 (32 I/O, 12 input only)					
Timers:						
Total Number (16-bit)	19(1,2)					
32-Bit (from paired 16-bit timers)	9					
Input Capture w/Timer Channels	6(2)					
Output Compare/PWM Channels	6(2)					
Single Output CCP (SCCP)	6					
Multiple Output CCP (MCCP)	1					
Serial Communications:						
UART	6(2)					
SPI (3-wire/4-wire)	4(2)					
I^2C	3					
USB On-The-Go	No			Yes		
Cryptographic Engine	Yes					
Parallel Communications (EPMP/PSP)	Yes					
10/12-Bit Analog-to-Digital Converter (A/D) (input channels)	24					
Digital-to-Analog Converter (DAC)	1					
Analog Comparators	3					
CTMU Interface	Yes					
LCD Controller (available pixels)	512 (64 SEG x 8 COM)					
JTAG Boundary Scan	Yes					
Resets (and delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)					
Instruction Set	77 Base Instructions, Multiple Addressing Mode Variations					
Packages	121-Pin TFBGA					

Note 1: Includes the Timer modes of SCCP and MCCP modules.

2: Some instantiations of these modules are only available through remappable pins.

TABLE 1-5: PIC24FJ256GB412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
LCDBIAS0	3	5	D2	O	ANA	Bias Inputs for LCD Driver Charge Pump
LCDBIAS1	2	4	C1	O	ANA	
LCDBIAS2	1	3	D3	O	ANA	
LCDBIAS3	17	26	L1	O	ANA	
LVDIN	64	100	A1	I	ANA	Low-Voltage Detect Input
$\overline{MCLR}$	7	13	F1	I	ST/STMV	Master Clear (device Reset) Input. This line is brought low to cause a Reset.
OC4	54	83	D7	O	DIG	Output Compare 4 Output
OC5	55	84	C7	O	DIG	Output Compare 5 Output
OC6	58	87	B6	O	DIG	Output Compare 6 Output
OCM1A	4	10	E3	O	DIG	MCCP1 Outputs
OCM1B	5	11	F4	O	DIG	
OCM1C	—	1	B2	O	DIG	
OCM1D	—	6	D1	O	DIG	
OCM1E	—	91	C5	O	DIG	
OCM1F	—	92	B5	O	DIG	
OCM2	6	12	F2	O	DIG	SCCP2 Output
OCM3	11	20	H1	O	DIG	SCCP3 Output
OSCI	39	63	F9	I	ANA/ST	Main Oscillator Input Connection
OSCO	40	64	F11	O	—	Main Oscillator Output Connection
PGEC1	15	24	K1	I	ST	ICSP™ Programming Clock
PGEC2	17	26	L1	I	ST	
PGEC3	11	20	H1	I	ST	
PGED1	16	25	K2	I/O	DIG/ST	ICSP Programming Data
PGED2	18	27	J3	I/O	DIG/ST	
PGED3	12	21	H2	I/O	DIG/ST	
PMA0/PMALL	30	44	L8	I/O	DIG/ST/TTL	Parallel Master Port Address<0>/Address Latch Low
PMA1/PMALH	29	43	K7	I/O	DIG/ST/TTL	Parallel Master Port Address<1>/Address Latch High
PMA14/PMCS/ APMCS1	45	71	C11	I/O	DIG/ST/TTL	Parallel Master Port Address<14>/Slave Chip Select/Alternate Chip Select 1 Strobe
PMA15/APMCS2	44	70	D11	I/O	DIG/ST/TTL	Parallel Master Port Address<15>/Alternate Chip Select 2 Strobe
PMA6	16	29	K3	O	DIG	Parallel Master Port Address
PMA7	22	28	L2	O	DIG	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

TABLE 8-2: IMPLEMENTED INTERRUPT VECTORS (CONTINUED)

Interrupt Source	Vector Number	IRQ #	IVT Address	Interrupt Bit Locations		
				Flag	Enable	Priority
MCCP1 Capture/Compare	71	63	000092h	IFS3<15>	IEC3<15>	IPC15<14:12>
MCCP1 Timer	109	101	0000DEh	IFS6<5>	IEC6<5>	IPC25<6:4>
SCCP2 Capture/Compare	72	64	000094h	IFS4<0>	IEC4<0>	IPC16<2:0>
SCCP2 Timer	110	102	0000E0h	IFS6<6>	IEC6<6>	IPC25<10:8>
SCCP3 Capture/Compare	102	94	0000D0h	IFS5<14>	IEC5<14>	IPC23<10:8>
SCCP3 Timer	51	43	00006Ah	IFS2<11>	IEC2<11>	IPC10<14:12>
SCCP4 Capture/Compare	103	95	0000D2h	IFS5<15>	IEC5<15>	IPC23<14:12>
SCCP4 Timer	52	44	00006Ch	IFS2<12>	IEC2<12>	IPC11<2:0>
Output Compare 1	10	2	000018h	IFS0<2>	IEC0<2>	IPC0<10:8>
Output Compare 2	14	6	000020h	IFS0<6>	IEC0<6>	IPC1<10:8>
Output Compare 3	33	25	000046h	IFS1<9>	IEC1<9>	IPC6<6:4>
Output Compare 4	34	26	000048h	IFS1<10>	IEC1<10>	IPC6<10:8>
Output Compare 5	49	41	000066h	IFS2<9>	IEC2<9>	IPC10<6:4>
Output Compare 6	50	42	000068h	IFS2<10>	IEC2<10>	IPC10<10:8>
Real-Time Clock and Calendar (RTCC)	70	62	000090h	IFS3<14>	IEC3<14>	IPC15<10:8>
RTCC Timestamp	118	110	0000F0h	IFS6<14>	IEC6<14>	IPC27<10:8>
SCCP5 Capture/Compare	30	22	000040h	IFS1<6>	IEC1<6>	IPC5<10:8>
SCCP6 Capture/Compare	31	23	000042h	IFS1<7>	IEC1<7>	IPC5<14:12>
SCCP7 Capture/Compare	81	73	0000A6h	IFS4<9>	IEC4<9>	IPC18<6:4>
SCCP5 Timer	55	47	000072h	IFS2<15>	IEC2<15>	IPC11<14:12>
SCCP6 Timer	56	48	000074h	IFS3<0>	IEC3<0>	IPC12<2:0>
SCCP7 Timer	59	51	00007Ah	IFS3<3>	IEC3<3>	IPC12<14:12>
SPI1 General	17	9	000026h	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 Receive	66	58	000088h	IFS3<10>	IEC3<10>	IPC14<10:8>
SPI1 Transmit	18	10	000028h	IFS0<10>	IEC0<10>	IPC2<10:8>
SPI2 General	40	32	000054h	IFS2<0>	IEC2<0>	IPC8<2:0>
SPI2 Receive	67	59	00008Ah	IFS3<11>	IEC3<11>	IPC14<14:12>
SPI2 Transmit	41	33	000056h	IFS2<1>	IEC2<1>	IPC8<6:4>
SPI3 General	98	90	0000C8h	IFS5<10>	IEC5<10>	IPC22<10:8>
SPI3 Receive	68	60	00008Ch	IFS3<12>	IEC3<12>	IPC15<2:0>
SPI3 Transmit	99	91	0000CAh	IFS5<11>	IEC5<11>	IPC22<14:12>
SPI3 Transmit	101	93	0000CEh	IFS5<13>	IEC5<13>	IPC23<6:4>
SPI4 General	100	92	0000CCh	IFS5<12>	IEC5<12>	IPC23<2:0>
SPI4 Receive	65	57	000086h	IFS3<9>	IEC3<9>	IPC14<6:4>
Timer1	11	3	00001Ah	IFS0<3>	IEC0<3>	IPC0<14:12>
Timer2	15	7	000022h	IFS0<7>	IEC0<7>	IPC1<14:12>
Timer3	16	8	000024h	IFS0<8>	IEC0<8>	IPC2<2:0>
Timer4	35	27	00004Ah	IFS1<11>	IEC1<11>	IPC6<14:12>
Timer5	36	28	00004Ch	IFS1<12>	IEC1<12>	IPC7<2:0>
UART1 Error	73	65	000096h	IFS4<1>	IEC4<1>	IPC16<6:4>
UART1 Receiver	19	11	00002Ah	IFS0<11>	IEC0<11>	IPC2<14:12>
UART1 Transmitter	20	12	00002Ch	IFS0<12>	IEC0<12>	IPC3<2:0>
UART2 Error	74	66	000098h	IFS4<2>	IEC4<2>	IPC16<10:8>
UART2 Receiver	38	30	000050h	IFS1<14>	IEC1<14>	IPC7<10:8>
UART2 Transmitter	39	31	000052h	IFS1<15>	IEC1<15>	IPC7<14:12>

TABLE 8-2: IMPLEMENTED INTERRUPT VECTORS (CONTINUED)

Interrupt Source	Vector Number	IRQ #	IVT Address	Interrupt Bit Locations		
				Flag	Enable	Priority
UART3 Error	89	81	0000B6h	IFS5<1>	IEC5<1>	IPC20<6:4>
UART3 Receiver	90	82	0000B8h	IFS5<2>	IEC5<2>	IPC20<10:8>
UART3 Transmitter	91	83	0000BAh	IFS5<3>	IEC5<3>	IPC20<14:12>
UART4 Error	95	87	0000C2h	IFS5<7>	IEC5<7>	IPC21<14:12>
UART4 Receiver	96	88	0000C4h	IFS5<8>	IEC5<8>	IPC22<2:0>
UART4 Transmitter	97	89	0000C6h	IFS5<9>	IEC5<9>	IPC22<6:4>
UART5 Error	121	113	0000F6h	IFS7<1>	IEC7<1>	IPC28<6:4>
UART5 Receive	119	111	0000F2h	IFS6<15>	IEC6<15>	IPC27<14:12>
UART5 Transmit	120	112	0000F4h	IFS7<0>	IEC7<0>	IPC28<2:0>
UART6 Error	124	116	0000FCh	IFS7<4>	IEC7<4>	IPC29<2:0>
UART6 Receive	122	114	0000F8h	IFS7<2>	IEC7<2>	IPC28<10:8>
UART6 Transmit	123	113	0000FAh	IFS7<3>	IEC7<3>	IPC28<14:12>
USB	94	86	0000C0h	IFS5<6>	IEC5<6>	IPC21<10:8>

REGISTER 8-18: IEC4: INTERRUPT ENABLE CONTROL REGISTER 4

U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
—	DAC1IE	CTMUIE	—	—	—	CCP7IE	HLVDIE
bit 15							bit 8

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
MI2C3IE	SI2C3IE	—	—	CRCIE	U2ERIE	U1ERIE	CCP2IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **DAC1IE:** DAC Converter Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13 **CTMUIE:** CTMU Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CCP7IE:** SCCP7 Capture/Compare Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 8 **HLVDIE:** High/Low-Voltage Detect Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 7 **MI2C3IE:** Master I2C3 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 6 **SI2C3IE:** Slave I2C3 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **CRCIE:** CRC Generator Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **U2ERIE:** UART2 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **U1ERIE:** UART1 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **CCP2IE:** SCCP2 Capture/Compare Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

REGISTER 8-34: IPC12: INTERRUPT PRIORITY CONTROL REGISTER 12

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CCT7IP2	CCT7IP1	CCT7IP0	—	MI2C2IP2	MI2C2IP1	MI2C2IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SI2C2IP2	SI2C2IP1	SI2C2IP0	—	CCT6IP2	CCT6IP1	CCT6IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **CCT7IP<2:0>:** SCCP7 Timer Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **MI2C2IP<2:0>:** Master I2C2 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SI2C2IP<2:0>:** Slave I2C2 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **CCT6IP<2:0>:** SCCP6 Timer Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-35: IPC13: INTERRUPT PRIORITY CONTROL REGISTER 13

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CRYDNIP2	CRYDNIP21	CRYDNIP0	—	INT4IP2	INT4IP1	INT4IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	INT3IP2	INT3IP1	INT3IP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **CRYDNIP<2:0>:** Cryptographic Operation Done Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **INT4IP<2:0>:** External Interrupt 4 Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **INT3IP<2:0>:** External Interrupt 3 Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

REGISTER 8-45: IPC23: INTERRUPT PRIORITY CONTROL REGISTER 23

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CCP4IP2	CCP4IP1	CCP4IP0	—	CCP3IP2	CCP3IP1	CCP3IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPI4TXIP2	SPI4TXIP1	SPI4TXIP0	—	SPI4IP2	SPI4IP1	SPI4IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **CCP4IP<2:0>:** SCCP4 Capture/Compare Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **CCP3IP<2:0>:** SCCP3 Capture/Compare Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **SPI4TXIP<2:0>:** SPI4 Transmit Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **SPI4IP<2:0>:** SPI4 General Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit
If FSCM is enabled (FCKSM1 = 1):
1 = Clock and PLL selections are locked
0 = Clock and PLL selections are not locked and may be modified by setting the OSWEN bit
If FSCM is disabled (FCKSM1 = 0):
Clock and PLL selections are never locked and may be modified by setting the OSWEN bit.

bit 6 **IOLOCK:** I/O Lock Enable bit(2)
1 = I/O lock is active
0 = I/O lock is not active

bit 5 **LOCK:** PLL Lock Status bit(3)
1 = PLL module is in lock or PLL module start-up timer is satisfied
0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled

bit 4 **Unimplemented:** Read as '0'

bit 3 **CF:** Clock Fail Detect bit
1 = FSCM has detected a clock failure
0 = No clock failure has been detected

bit 2 **POSCEN:** Primary Oscillator Sleep Enable bit
1 = Primary Oscillator continues to operate during Sleep mode
0 = Primary Oscillator is disabled during Sleep mode

bit 1 **SOSCEN:** 32 kHz Secondary Oscillator (SOSC) Enable bit
1 = Enables Secondary Oscillator
0 = Disables Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit
1 = Initiates an oscillator switch to a clock source specified by the NOSC<2:0> bits
0 = Oscillator switch is complete

Note 1: Reset values for these bits are determined by the FNOSCx Configuration bits.
2: The state of the IOLOCK bit can only be changed once an unlocking sequence has been executed. In addition, if the IOL1WAY Configuration bit is '1' once the IOLOCK bit is set, it cannot be cleared.
3: This bit also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.
4: The default divisor of the postscaler is 2, which will generate a 4 MHz clock to the PLL module.

REGISTER 9-5: REFOCONH: REFERENCE CLOCK CONTROL HIGH REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RODIV<14:8>						
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RODIV<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-0 **RODIV<14:0>:** Reference Clock Integer Divisor Select bits
Divisor for the selected input clock source is two times the selected value.
111 1111 1111 1111 = Base clock value divided by 65,534 (2 * 7FFFh)
111 1111 1111 1110 = Base clock value divided by 65,532 (2 * 7FFEh)
111 1111 1111 1101 = Base clock value divided by 65,530 (2 * 7FFDh)
• • •
000 0000 0000 0010 = Base clock value divided by 4 (2 * 2)
000 0000 0000 0001 = Base clock value divided by 2 (2 * 1)
000 0000 0000 0000 = Base clock value

REGISTER 9-6: REFOTRIML: REFERENCE CLOCK TRIM REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROTRIM<8:1>							
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
ROTRIM0	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **ROTRIM<8:0>:** Reference Clock Fractional Divisor Select bits
Added fractional portion of the divisor for the selected input clock source is the value, divided by 512.
111111111 = 1 (512/512)
111111110 = 0.998947 (511/512)
111111101 = 0.996094 (510/512)
• • •
000000010 = 0.003906 (2/512)
000000001 = 0.001953 (1/512)
000000000 = No fractional portion (0/512)

bit 6-0 **Unimplemented:** Read as '0'

REGISTER 11-31: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP17R5	RP17R4	RP17R3	RP17R2	RP17R1	RP17R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP16R5	RP16R4	RP16R3	RP16R2	RP16R1	RP16R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP17R<5:0>:** RP17 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP17 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP16R<5:0>:** RP16 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP16 (see Table 11-12 for peripheral function numbers).

REGISTER 11-32: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP19R5	RP19R4	RP19R3	RP19R2	RP19R1	RP19R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP18R5	RP18R4	RP18R3	RP18R2	RP18R1	RP18R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

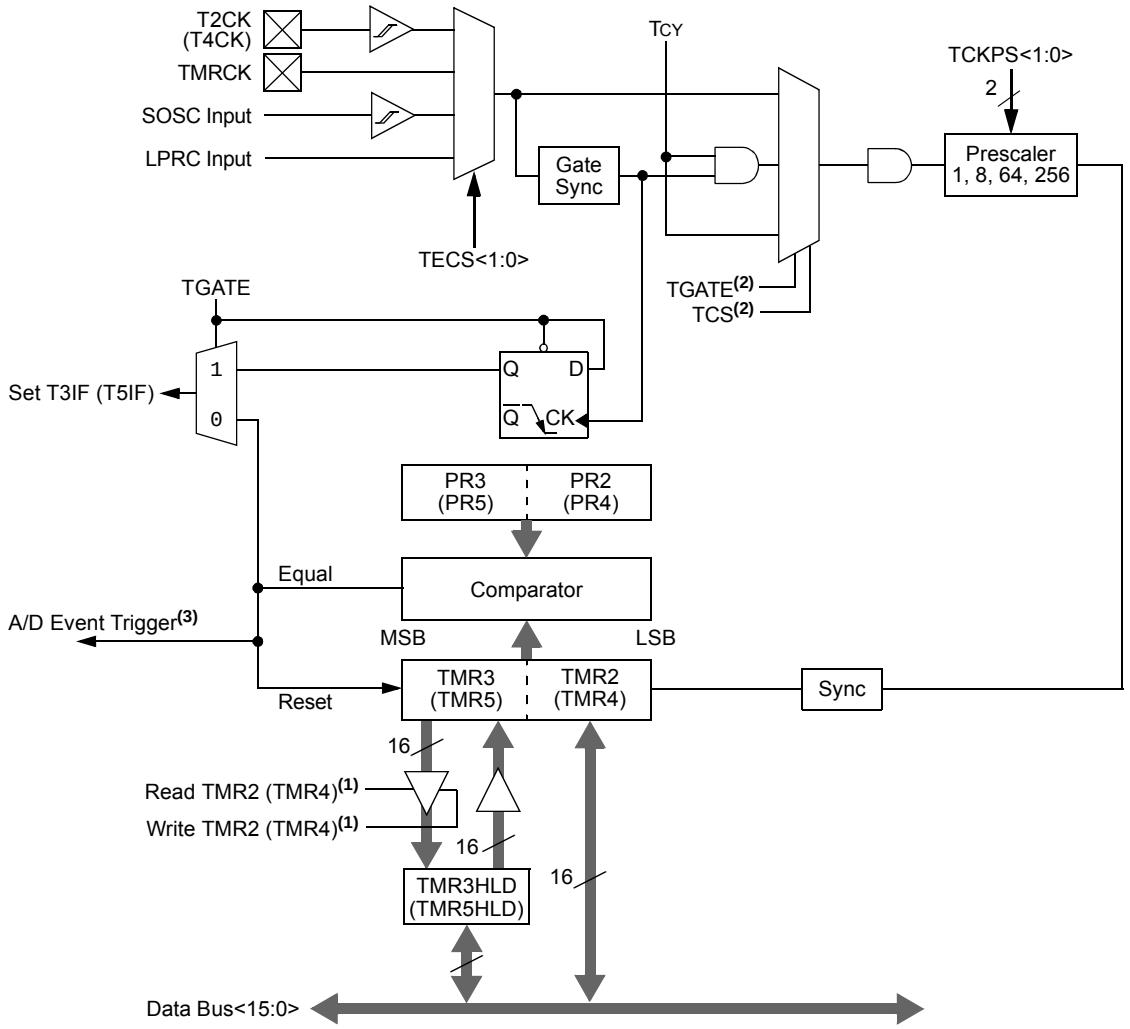
bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP19R<5:0>:** RP19 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP19 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP18R<5:0>:** RP18 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP18 (see Table 11-12 for peripheral function numbers).

FIGURE 13-1: TIMER2/3 AND TIMER4/5 (32-BIT) BLOCK DIAGRAM



Note 1: The 32-Bit Timer Configuration bit, T32, must be set for 32-bit timer/counter operation. All control bits are respective to the T2CON and T4CON registers.

2: The timer clock input must be assigned to an available RPn/RPIn pin before use. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

3: The A/D Event Trigger is available only on Timer2/3 in 32-bit mode and Timer3 in 16-bit mode.

18.2 Setting Baud Rate When Operating as a Bus Master

To compute the Baud Rate Generator reload value, use Equation 18-1.

EQUATION 18-1: COMPUTING BAUD RATE RELOAD VALUE(1,2)

$$F_{SCL} = \frac{F_{CY}}{2 \cdot (BRG + 2)}$$

or

$$BRG = \left(\frac{F_{CY}}{2 \cdot F_{SCL}}\right) - 2$$

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

2: These clock rate values are for guidance only. The actual clock rate can be affected by various system-level parameters. The actual clock rate should be measured in its intended application.

18.3 Slave Address Masking

The I2CxMSK register (Register 18-4) designates address bit positions as “don’t care” for both 7-Bit and 10-Bit Addressing modes. Setting a particular bit location (= 1) in the I2CxMSK register causes the slave module to respond, whether the corresponding address bit value is a ‘0’ or a ‘1’. For example, when I2CxMSK is set to ‘0010000000’, the slave module will detect both addresses, ‘0000000000’ and ‘0010000000’.

To enable address masking, the Intelligent Peripheral Management Interface (IPMI) must be disabled by clearing the STRICT bit (I2CxCONH<11>).

Note: As a result of changes in the I^2C protocol, the addresses in Table 18-2 are reserved and will not be Acknowledged in Slave mode. This includes any address mask settings that include any of these addresses.

TABLE 18-1: I2Cx CLOCK RATES(1,2)

Required System FSCL	FCY	I2CxBRG Value		Actual FSCL
		(Decimal)	(Hexadecimal)	
100 kHz	16 MHz	157	9D	100 kHz
100 kHz	8 MHz	78	4E	100 kHz
100 kHz	4 MHz	39	27	99 kHz
400 kHz	16 MHz	37	25	404 kHz
400 kHz	8 MHz	18	12	404 kHz
400 kHz	4 MHz	9	9	385 kHz
400 kHz	2 MHz	4	4	385 kHz
1 MHz	16 MHz	13	D	1.026 MHz
1 MHz	8 MHz	6	6	1.026 MHz
1 MHz	4 MHz	3	3	0.909 MHz

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

2: These clock rate values are for guidance only. The actual clock rate can be affected by various system-level parameters. The actual clock rate should be measured in its intended application.

TABLE 18-2: I2Cx RESERVED ADDRESSES(1)

Slave Address	R/$\overline{W}$ Bit	Description
0000 000	0	General Call Address(2)
0000 000	1	Start Byte
0000 001	x	CBus Address
0000 01x	x	Reserved
0000 1xx	x	HS Mode Master Code
1111 0xx	x	10-Bit Slave Upper Byte(3)
1111 1xx	x	Reserved

Note 1: The address bits listed here will never cause an address match independent of address mask settings.

2: This address will be Acknowledged only if GCEN = 1.

3: A match on this address can only occur on the upper byte in 10-Bit Addressing mode.

20.0 UNIVERSAL SERIAL BUS WITH ON-THE-GO SUPPORT (USB OTG)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"USB On-The-Go (OTG)"** (DS39721). The information in this data sheet supersedes the information in the FRM.

PIC24FJ256GB412 family devices contain a full-speed and low-speed compatible, On-The-Go (OTG) USB Serial Interface Engine (SIE). The OTG capability allows the device to act as either a USB peripheral device or as a USB embedded host with limited host capabilities. The OTG capability allows the device to dynamically switch from device to host operation using OTG's Host Negotiation Protocol (HNP).

For more details on OTG operation, refer to the *"On-The-Go Supplement"* to the *"USB 2.0 Specification"*, published by the USB-IF. For more details on USB operation, refer to the *"Universal Serial Bus Specification"*, v2.0.

Note: USB functionality is not available on PIC24FJ256GA412 family devices.

The USB OTG module offers these features:

- USB Functionality in Device and Host Modes, and OTG Capabilities for Application-Controlled Mode Switching
- Software-Selectable Module Speeds of Full Speed (12 Mbps) or Low Speed (1.5 Mbps, available in Host mode only)
- Support for All Four USB Transfer Types: Control, Interrupt, Bulk and Isochronous
- 16 Bidirectional Endpoints for a Total of 32 Unique Endpoints
- DMA Interface for Data RAM Access
- Queues up to Sixteen Unique Endpoint Transfers without Servicing
- Integrated, On-Chip USB Transceiver with Support for Off-Chip Transceivers via a Digital Interface
- Integrated VBUS Generation with On-Chip Comparators and Boost Generation, and Support of External VBUS Comparators and Regulators through a Digital Interface
- Configurations for On-chip Bus Pull-up and Pull-Down Resistors

A simplified block diagram of the USB OTG module is shown in Figure 20-1.

The USB OTG module can function as a USB peripheral device or as a USB host, and may dynamically switch between Device and Host modes under software control. In either mode, the same data paths and Buffer Descriptors (BDs) are used for the transmission and reception of data.

In discussing USB operation, this section will use a controller-centric nomenclature for describing the direction of the data transfer between the microcontroller and the USB. RX (Receive) will be used to describe transfers that move data from the USB to the microcontroller and TX (Transmit) will be used to describe transfers that move data from the microcontroller to the USB. Table 20-1 shows the relationship between data direction in this nomenclature and the USB tokens exchanged.

TABLE 20-1: CONTROLLER-CENTRIC DATA DIRECTION FOR USB HOST OR TARGET

USB Mode	Direction	
	RX	TX
Device	OUT or SETUP	IN
Host	IN	OUT or SETUP

This chapter presents the most basic operations needed to implement USB OTG functionality in an application. A complete and detailed discussion of the USB protocol and its OTG supplement are beyond the scope of this data sheet. It is assumed that the user already has a basic understanding of USB architecture and the latest version of the protocol.

Not all steps for proper USB operation (such as device enumeration) are presented here. It is recommended that application developers use an appropriate device driver to implement all of the necessary features. Microchip provides a number of application-specific resources, such as USB firmware and driver support. Refer to www.microchip.com/usb for the latest firmware and driver support.

20.5.2 COMPLETE A CONTROL TRANSACTION TO A CONNECTED DEVICE

1. Follow the procedure described in **Section 20.5.1 "Enable Host Mode and Discover a Connected Device"** to discover a device.
2. Set up the Endpoint Control register for bidirectional control transfers by writing 0Dh to U1EP0 (this sets the EPCONDIS, EPTXEN and EPHSHK bits).
3. Place a copy of the device framework setup command in a memory buffer. See Chapter 9 of the *"USB 2.0 Specification"* for information on the device framework command set.
4. Initialize the Buffer Descriptor (BD) for the current (even or odd) TX EP0 to transfer the eight bytes of command data for a device framework command (i.e., `GET DEVICE DESCRIPTOR`):
   a) Set the BD Data Buffer Address (BD0ADR) to the starting address of the 8-byte memory buffer containing the command.
   b) Write 8008h to BD0STAT (this sets the UOWN bit and sets a byte count of 8).
5. Set the USB device address of the target device in the address register (U1ADDR<6:0>). After a USB bus Reset, the device USB address will be zero. After enumeration, it will be set to another value between 1 and 127.
6. Write D0h to U1TOK; this is a SETUP token to Endpoint 0, the target device's default control pipe. This initiates a SETUP token on the bus, followed by a data packet. The device handshake is returned in the PID field of BD0STAT after the packets are complete. When the USB module updates BD0STAT, a Token Complete Interrupt Flag is asserted (the TRNIF flag is set). This completes the setup phase of the setup transaction, as referenced in Chapter 9 of the *"USB 2.0 Specification"*.
7. To initiate the data phase of the setup transaction (i.e., get the data for the `GET DEVICE DESCRIPTOR` command), set up a buffer in memory to store the received data.
8. Initialize the current (even or odd) RX or TX (RX for IN, TX for OUT) EP0 BD to transfer the data.
   a) Write C040h to BD0STAT. This sets the UOWN, configures Data Toggle (DTS) to DATA1 and sets the byte count to the length of the data buffer (64 or 40h in this case).
   b) Set BD0ADR to the starting address of the data buffer.
9. Write the Token register with the appropriate IN or OUT token to Endpoint 0, the target device's default control pipe (e.g., write 90h to U1TOK for an IN token for a `GET DEVICE DESCRIPTOR` command). This initiates an IN token on the bus, followed by a data packet from the device to the host. When the data packet completes, the BD0STAT is written and a Token Complete Interrupt Flag is asserted (the TRNIF flag is set). For control transfers with a single packet data phase, this completes the data phase of the setup transaction, as referenced in Chapter 9 of the *"USB 2.0 Specification"*. If more data needs to be transferred, return to Step 8.
10. To initiate the status phase of the setup transaction, set up a buffer in memory to receive or send the zero length status phase data packet.
11. Initialize the current (even or odd) TX EP0 BD to transfer the status data:
    a) Set the BDT buffer address field to the start address of the data buffer.
    b) Write 8000h to BD0STAT (set UOWN bit, configure DTS to DATA0 and set byte count to 0).
12. Write the Token register with the appropriate IN or OUT token to Endpoint 0, the target device's default control pipe (e.g., write 01h to U1TOK for an OUT token for a `GET DEVICE DESCRIPTOR` command). This initiates an OUT token on the bus, followed by a zero length data packet from the host to the device. When the data packet completes, the BD is updated with the handshake from the device and a Token Complete Interrupt Flag is asserted (the TRNIF flag is set). This completes the status phase of the setup transaction, as described in Chapter 9 of the *"USB 2.0 Specification"*.

Note:	Only one control transaction can be performed per frame.

REGISTER 20-6: U1STAT: USB STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	U-0	U-0
ENDPT3	ENDPT2	ENDPT1	ENDPT0	DIR	PPBI(1)	—	—
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-4 **ENDPT<3:0>:** Number of the Last Endpoint Activity bits
(Represents the number of the BDT updated by the last USB transfer.)
1111 = Endpoint 15
1110 = Endpoint 14
•
•
•
0001 = Endpoint 1
0000 = Endpoint 0

bit 3 **DIR:** Last BD Direction Indicator bit
1 = The last transaction was a transmit transfer (TX)
0 = The last transaction was a receive transfer (RX)

bit 2 **PPBI:** Ping-Pong BD Pointer Indicator bit(1)
1 = The last transaction was to the odd BD bank
0 = The last transaction was to the even BD bank

bit 1-0 **Unimplemented:** Read as '0'

Note 1: This bit is only valid for endpoints with available even and odd BD registers.

REGISTER 21-7: PMCSxMD: EPMP CHIP SELECT x MODE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
ACKM1	ACKM0	AMWAIT2	AMWAIT1	AMWAIT0	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DWAITB1	DWAITB0	DWAITM3	DWAITM2	DWAITM1	DWAITM0	DWAITE1	DWAITE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **ACKM<1:0>:** Chip Select x Acknowledge Mode bits
11 = Reserved
10 = PMACKx is used to determine when a read/write operation is complete
01 = PMACKx is used to determine when a read/write operation is complete with time-out
(If DWAITM<3:0> = 0000, the maximum time-out is 255 TCY or else it is DWAITM<3:0> cycles.)
00 = PMACKx is not used

bit 13-11 **AMWAIT<2:0>:** Chip Select x Alternate Master Wait States bits
111 = Wait of 10 alternate master cycles
...
001 = Wait of 4 alternate master cycles
000 = Wait of 3 alternate master cycles

bit 10-8 **Unimplemented:** Read as '0'

bit 7-6 **DWAITB<1:0>:** Chip Select x Data Setup Before Read/Write Strobe Wait States bits
11 = Wait of 3¼ TCY
10 = Wait of 2¼ TCY
01 = Wait of 1¼ TCY
00 = Wait of ¼ TCY

bit 5-2 **DWAITM<3:0>:** Chip Select x Data Read/Write Strobe Wait States bits
For Write Operations:
1111 = Wait of 15½ TCY
...
0001 = Wait of 1½ TCY
0000 = Wait of ½ TCY
For Read Operations:
1111 = Wait of 15¾ TCY
...
0001 = Wait of 1¾ TCY
0000 = Wait of ¾ TCY

bit 1-0 **DWAITE<1:0>:** Chip Select x Data Hold After Read/Write Strobe Wait States bits
For Write Operations:
11 = Wait of 3¼ TCY
10 = Wait of 2¼ TCY
01 = Wait of 1¼ TCY
00 = Wait of ¼ TCY
For Read Operations:
11 = Wait of 3 TCY
10 = Wait of 2 TCY
01 = Wait of 1 TCY
00 = Wait of 0 TCY

REGISTER 24-3: RTCCON2L: RTCC CONTROL REGISTER 2 (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
FDIV4	FDIV3	FDIV2	FDIV1	FDIV0	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
PWCPS1	PWCPS0	PS1	PS0	—	—	CLKSEL1	CLKSEL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **FDIV<4:0>:** Fractional Clock Divide bits

11111 = Clock period increases by 31 RTCC input clock cycles every 16 seconds
11101 = Clock period increases by 30 RTCC input clock cycles every 16 seconds
• • •
00010 = Clock period increases by 2 RTCC input clock cycles every 16 seconds
00001 = Clock period increases by 1 RTCC input clock cycle every 16 seconds
00000 = No fractional clock division

bit 10-8 **Unimplemented:** Read as '0'

bit 7-6 **PWCPS<1:0>:** Power Control Prescale Select bits

11 = 1:256
10 = 1:64
01 = 1:16
00 = 1:1

bit 5-4 **PS<1:0>:** Prescale Select bits

11 = 1:256
10 = 1:64
01 = 1:16
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CLKSEL<1:0>:** Clock Select bits

11 = Peripheral clock (FCY)
10 = PWRLCLK input pin
01 = LPRC
00 = SOSC

TABLE 36-11: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
DVR10	VBG	Internal Band Gap Reference	—	1.2	—	V	
DVR11	TBG	Band Gap Reference Start-up Time	—	1	—	ms	
DVR20	VRGOUT	Regulator Output Voltage	—	1.8	—	V	VDD > 2.0V
DVR21	CEFC	External Filter Capacitor Value	4.7	10	—	μF	Series Resistance < 3Ω recommended; < 5Ω required.
DVR	TVREG	Start-up Time	—	10	—	μs	PMSLP = 1 with any POR or BOR
DVR30	VLVR	Low-Voltage Regulator Output Voltage	—	1.2	—	V	RETEN = 1, $\overline{\text{LPCFG}}$ = 0

TABLE 36-12: VBAT OPERATING VOLTAGE SPECIFICATIONS

Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
DVB01	VBT	Operating Voltage	1.6	—	3.6	V	Battery connected to the VBAT pin, VBTBOR = 0
DVB02			VBATBOR	—	3.6	V	Battery connected to the VBAT pin, VBTBOR = 1
DVB10	VBTADC	VBAT A/D Monitoring Voltage Specification(1)	1.6	—	3.6	V	A/D is monitoring the VBAT pin using the internal A/D channel

Note 1: Measuring the A/D value using the A/D is represented by the equation: Measured Voltage = ((VBAT/2)/VDD) * 4096) for 12-bit A/D.

TABLE 36-13: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			**Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial					
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Comments**	**Conditions**
DCT10	IOUT1	CTMU Current Source, Base Range	—	550	—	nA	CTMUCON1L<1:0> = 00	2.5V < VDD < VDDMAX
DCT11	IOUT2	CTMU Current Source, 10x Range	—	5.5	—	μA	CTMUCON1L<1:0> = 01	
DCT12	IOUT3	CTMU Current Source, 100x Range	—	55	—	μA	CTMUCON1L<1:0> = 10	
DCT13	IOUT4	CTMU Current Source, 1000x Range	—	550	—	μA	CTMUCON1L<1:0> = 11(2)	
DCT21	VΔ	Temperature Diode Voltage Change per Degree Celsius	—	-3	—	mV/°C		

Note 1: Nominal value at center point of current trim range (CTMUCON1L<7:2> = 000000).

2: Do not use this current range with temperature sensing diode.