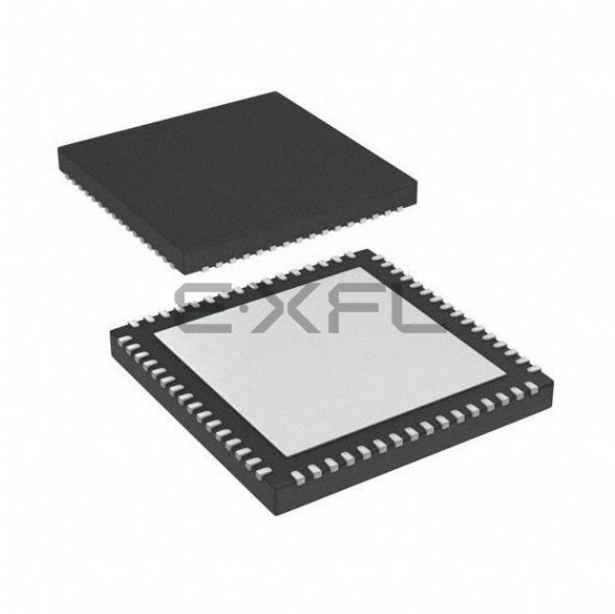

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Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128gb406-i-mr

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
INT0	46	72	D9	I	ST/STMV	External Interrupt Input 0
IOCA0	—	17	G3	I	ST	PORTA Interrupt-on-Change
IOCA1	—	38	J6	I	ST	
IOCA2	—	58	H11	I	ST	
IOCA3	—	59	G10	I	ST	
IOCA4	—	60	G11	I	ST	
IOCA5	—	61	G9	I	ST	
IOCA6	—	91	E10	I	ST	
IOCA7	—	92	E11	I	ST	
IOCA9	—	28	L2	I	ST	
IOCA10	—	29	K3	I	ST	
IOCA14	—	66	E11	I	ST	
IOCA15	—	67	E8	I	ST	
IOCB0	16	25	K2	I	ST	PORTB Interrupt-on-Change
IOCB1	15	24	K1	I	ST	
IOCB2	14	23	J2	I	ST	
IOCB3	13	22	J1	I	ST	
IOCB4	12	21	H2	I	ST	
IOCB5	11	20	H1	I	ST	
IOCB6	17	26	L1	I	ST	
IOCB7	18	27	J3	I	ST	
IOCB8	21	32	K4	I	ST	
IOCB9	22	33	L4	I	ST	
IOCB10	23	34	H5	I	ST	
IOCB11	24	35	K5	I	ST	
IOCB12	27	41	J7	I	ST	
IOCB13	28	42	L7	I	ST	
IOCB14	29	43	K7	I	ST	
IOCB15	30	44	L8	I	ST	
IOCC1	—	6	D1	I	ST	PORTC Interrupt-on-Change
IOCC2	—	7	E4	I	ST	
IOCC3	—	8	E2	I	ST	
IOCC4	—	9	E1	I	ST	
IOCC12	39	63	F9	I	ST	
IOCC13	47	73	C10	I	ST	
IOCC14	48	74	B11	I	ST	
IOCC15	40	64	F11	I	ST	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
RPI32	—	40	K6	I	ST	Remappable Peripherals (Input only)
RPI33	—	18	G1	I	ST	
RPI34	—	19	G2	I	ST	
RPI35	—	67	E8	I	ST	
RPI36	—	66	E11	I	ST	
RPI37	48	74	B11	I	ST	
RPI38	—	6	D1	I	ST	
RPI39	—	7	E4	I	ST	
RPI40	—	8	E2	I	ST	
RPI41	—	9	E1	I	ST	
RPI42	—	79	A9	I	ST	
RPI43	—	47	L9	I	ST	
RTCC	42	68	E9	O	DIGMV	Real-Time Clock Alarm/Seconds Pulse Output
SCK4	59	88	A6	I/O	DIG/ST	SPI4 Clock
SCL1	37	57	H10	I/O	DIG/I^2C/SMB	I2C1 Synchronous Serial Clock Input/Output
SCL2	32	58	H11	I/O	DIG/I^2C/SMB	I2C2 Synchronous Serial Clock Input/Output
SCL3	2	4	C1	I/O	DIG/I^2C/SMB	I2C3 Synchronous Serial Clock Input/Output
SDA1	36	56	J11	I/O	DIG/I^2C/SMB	I2C1 Data Input/Output
SDA2	31	59	G10	I/O	DIG/I^2C/SMB	I2C2 Data Input/Output
SDA3	3	5	D2	I/O	DIG/I^2C/SMB	I2C3 Data Input/Output
SDI4	28	42	L7	I	ST	SPI4 Data Input
SDO4	23	34	H5	O	DIG	SPI4 Data Output

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

4.1.4 FLASH CONFIGURATION WORDS

In PIC24FJ256GA412/GB412 family devices, the top nine words of on-chip program memory are reserved for configuration information. On device Reset, the configuration information is copied into the actual Configuration registers, located in configuration space.

The address range of the Flash Configuration Words for devices in the PIC24FJ256GA412/GB412 family are shown in Table 4-2. Their location in the memory map is shown with the other memory vectors in Figure 4-1. Additional details on the device Configuration Words are provided in **Section 33.0 "Special Features"**.

4.1.4.1 Dual Partition Configuration Words

In Dual Partition Flash modes, each partition has its own set of Flash Configuration Words. The full set of Configuration registers in the Active Partition is used to determine the device's configuration; the Configuration Words in the Inactive Partition are used to determine the device's configuration when that partition becomes active. However, some of the Configuration registers in the Inactive Partition (FSEC, FBSLIM and FSIGN) may be used to determine how the Active Partition is able or allowed to access the Inactive Partition.

4.1.5 ONE-TIME-PROGRAMMABLE (OTP) MEMORY

PIC24FJ256GA412/GB412 family devices provide 384 bytes of One-Time-Programmable (OTP) memory, located at addresses, 801380h through 8013FEh. This memory can be used for persistent storage of application-specific information that will not be erased by reprogramming the device. This includes many types of information, such as (but not limited to):

- Application checksums
- Code revision information
- Product information
- Serial numbers
- System manufacturing dates
- Manufacturing lot numbers

OTP memory may be programmed in any mode, including user RTSP mode, but it cannot be erased. Data is not cleared by a Chip Erase. Once programmed, it cannot be rewritten.

Do not perform repeated write operations on the OTP.

TABLE 4-2: FLASH CONFIGURATION WORDS FOR PIC24FJ256GA412/GB412 FAMILY DEVICES

Device Family	Program Memory (Words)	Configuration Word Address Range	
		Single Partition	Dual Partition(1)
PIC24FJ64GA4XX/GB4XX	22,016	00AF80h:00AFB0h	005780h:0057FCh
PIC24FJ128GA4XX/GB4XX	44,032	015780h:0157B0h	00AB80h:00ABFCh
PIC24FJ256GA4XX/GB4XX	88,065	02AF80h:02AFB0h	015780h:0157FCh

Note 1: Addresses for the Active Partition are shown. For the Inactive Partitions, add 400000h.

TABLE 4-8: SFR BLOCK 300h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
CCP/Timer (SCCP)			CCP7CON1L	36C	0000000000000000	U4TXREG	3D4	x000000xxxxxxxxx
CCP4CON1L	300	0000000000000000	CCP7CON1H	36E	0000000000000000	U4RXREG	3D6	0000000000000000
CCP4CON1H	302	0000000000000000	CCP7CON2L	370	0000000000000000	U4BRG	3D8	0000000000000000
CCP4CON2L	304	0000000000000000	CCP7CON2H	372	0000000100000000	U4ADMD	3DA	0000000000000000
CCP4CON2H	306	0000000100000000	CCP7CON3H	376	0000000000000000	U5MODE	3DC	0000000000000000
CCP4CON3H	30A	0000000000000000	CCP7STATL	378	00000000000xx0000	U5STA	3DE	0000000100010000
CCP4STATL	30C	00000000000xx0000	CCP7STATH	37A	0000000000000000	U5TXREG	3E0	x000000xxxxxxxxx
CCP4STATH	30E	0000000000000000	CCP7TMRL	37C	0000000000000000	U5RXREG	3E2	0000000000000000
CCP4TMRL	310	0000000000000000	CCP7TMRH	37E	0000000000000000	U5BRG	3E4	0000000000000000
CCP4TMRH	312	0000000000000000	CCP7PRL	380	1111111111111111	U5ADMD	3E6	0000000000000000
CCP4PRL	314	1111111111111111	CCP7PRH	382	1111111111111111	U6MODE	3E8	0000000000000000
CCP4PRH	316	1111111111111111	CCP7RAL	384	0000000000000000	U6STAL	3EA	0000000100010000
CCP4RAL	318	0000000000000000	CCP7RBL	388	0000000000000000	U6TXREG	3EC	x000000xxxxxxxxx
CCP4RBL	31C	0000000000000000	CCP7BUFL	38C	0000000000000000	U6RXREG	3EE	0000000000000000
CCP4BUFL	320	0000000000000000	CCP7BUFH	38E	0000000000000000	U6BRG	3F0	0000000000000000
CCP4BUFH	322	0000000000000000	**UART**			U6ADMD	3F2	0000000000000000
CCP5CON1L	324	0000000000000000	U1MODE	398	0000000000000000	**SPI**		
CCP5CON1H	326	0000000000000000	U1STA	39A	0000000100010000	SPI1CON1L	3F4	0000000000000000
CCP5CON2L	328	0000000000000000	U1TXREG	39C	x000000xxxxxxxxx	SPI1CON1H	3F6	0000000000000000
CCP5CON2H	32A	0000000100000000	U1RXREG	39E	0000000000000000	SPI1CON2L	3F8	0000000000000000
CCP5CON3H	32E	0000000000000000	U1BRG	3A0	0000000000000000	SPI1STATL	3FC	0000000000101000
CCP5STATL	330	00000000000xx0000	U1ADMD	3A2	0000000000000000	SPI1STATH	3FE	0000000000000000
CCP5STATH	332	0000000000000000	U1SCCON	3A4	0000000000000000			
CCP5TMRL	334	0000000000000000	U1SCINT	3A6	0000000000000000			
CCP5TMRH	336	0000000000000000	U1GTC	3A8	0000000000000000			
CCP5PRL	338	1111111111111111	U1WTCH	3AA	0000000000000000			
CCP5PRH	33A	1111111111111111	U1WTCL	3AC	0000000000000000			
CCP5RAL	33C	0000000000000000	U2MODE	3AE	0000000000000000			
CCP5RBL	340	0000000000000000	U2STA	3B0	0000000100010000			
CCP5BUFL	344	0000000000000000	U2TXREG	3B2	x000000xxxxxxxxx			
CCP5BUFH	346	0000000000000000	U2RXREG	3B4	0000000000000000			
CCP6CON1L	348	0000000000000000	U2BRG	3B6	0000000000000000			
CCP6CON1H	34A	0000000000000000	U2ADMD	3B8	0000000000000000			
CCP6CON2L	34C	0000000000000000	U2SCCON	3BA	0000000000000000			
CCP6CON2H	34E	0000000100000000	U2SCINT	3BC	0000000000000000			
CCP6CON3H	352	0000000000000000	U2GTC	3BE	0000000000000000			
CCP6STATL	354	00000000000xx0000	U2WTCH	3C0	0000000000000000			
CCP6STATH	356	0000000000000000	U2WTCL	3C2	0000000000000000			
CCP6TMRL	358	0000000000000000	U3MODE	3C4	0000000000000000			
CCP6TMRH	35A	0000000000000000	U3STA	3C6	0000000100010000			
CCP6PRL	35C	1111111111111111	U3TXREG	3C8	x000000xxxxxxxxx			
CCP6PRH	35E	1111111111111111	U3RXREG	3CA	0000000000000000			
CCP6RAL	360	0000000000000000	U3BRG	3CC	0000000000000000			
CCP6RBL	364	0000000000000000	U3ADMD	3CE	0000000000000000			
CCP6BUFL	368	0000000000000000	U4MODE	3D0	0000000000000000			
CCP6BUFH	36A	0000000000000000	U4STA	3D2	0000000100010000			

Legend: x = unknown or indeterminate value. Reset and address values are in hexadecimal.

REGISTER 8-4: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-0	R-0, HSC	R/W-0	U-0	U-0	U-0	U-0	R/W-0
GIE	DISI	SWTRAP	—	—	—	—	ALTIVT
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **GIE:** Global Interrupt Enable bit
1 = Interrupt and associated interrupt enable bits are enabled
0 = Interrupts are disabled; traps remain enabled

bit 14 **DISI:** DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active

bit 13 **SWTRAP:** Software Trap Status bit
1 = Generates a software trap
0 = Software trap is not requested

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **ALTIVT:** Enable Alternate Interrupt Vector Table bit
1 = Uses Alternate Interrupt Vector Table
0 = Uses standard (default) Interrupt Vector Table

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 3 **INT3EP:** External Interrupt 3 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

REGISTER 8-16: IEC2: INTERRUPT ENABLE CONTROL REGISTER 2 (CONTINUED)

bit 3 **CRYROLLIE:** Cryptographic Rollover Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **CRYFREEIE:** Cryptographic Buffer Free Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **SPI2TXIE:** SPI2 Transmit Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **SPI2IE:** SPI2 General Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

REGISTER 8-47: IPC25: INTERRUPT PRIORITY CONTROL REGISTER 25

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	CCT2IP2	CCT2IP1	CCT2IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CCT1IP2	CCT1IP1	CCT1IP0	—	LCDIP2	LCDIP1	LCDIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-8 **CCT2IP<2:0>:** SCCP2 Timer Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **CCT1IP<2:0>:** MCCP1 Timer Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **LCDIP<2:0>:** LCD Controller Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

10.6 Clock Frequency and Clock Switching

In Run and Idle modes, all PIC24FJ devices allow for a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits. The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

10.7 Doze Mode

Generally, changing clock speed and invoking one of the power-saving modes are the preferred strategies for reducing power consumption. There may be circumstances, however, where this is not practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed may introduce communication errors, while using a power-saving mode may stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:8 being the default.

It is also possible to use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU Idles, waiting for something to invoke an interrupt routine. Enabling the automatic return to full-speed CPU operation on interrupts is enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

10.8 Selective Peripheral Module Control

Idle and Doze modes allow users to substantially reduce power consumption by slowing or stopping the CPU clock. Even so, peripheral modules still remain clocked, and thus, consume power. There may be cases where the application needs what these modes do not provide: the allocation of power resources to the CPU processing with minimal power consumption from the peripherals.

PIC24F devices address this requirement by allowing peripheral modules to be selectively disabled, reducing or eliminating their power consumption. This can be done with two control bits:

- The Peripheral Enable bit, generically named, "XXXEN", located in the module's main control SFR.
- The Peripheral Module Disable (PMD) bit, located in one of the PMDx registers (Register 10-4 through Register 10-11).

Both bits have similar functions in enabling or disabling its associated module. Setting the PMDx bit for a module disables all clock sources to that module, reducing its power consumption to an absolute minimum. In this state, the control and status registers associated with the peripheral will also be disabled, so writes to those registers will have no effect and read values will be invalid. Many peripheral modules have a corresponding PMDx bit.

In contrast, disabling a module by clearing its XXXEN bit disables its functionality, but leaves its registers available to be read and written to. Power consumption is reduced, but not by as much as when the PMDx bits are used. Most peripheral modules have an enable bit; exceptions include capture, compare and RTCC.

To achieve more selective power savings, peripheral modules can also be selectively disabled when the device enters Idle mode. This is done through the control bit of the generic name format, "XXXIDL". By default, all modules that can operate during Idle mode will do so. Using the disable on Idle feature disables the module while in Idle mode, allowing further reduction of power consumption during Idle mode, enhancing power savings for extremely critical power applications.

TABLE 11-10: PORTJ REGISTER MAP(1)

Register Name	Bit Range	Bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRISJ	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRISJ<1:0>	
PORTJ	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PORTJ<1:0>	
LATJ	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LATJ<1:0>	
ODCJ	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ODCJ<1:0>	
IOCPJ	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCPJ<1:0>	
IOCNJ	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCNJ<1:0>	
IOCFJ	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCFJ<1:0>	
IOCPUJ	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCPUJ<1:0>	
IOCPDJ	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCPDJ<1:0>	

Legend: — = unimplemented, read as '0'.

Note 1: PORT register maps show full pin count devices. Please refer to Table 1-4 and Table 1-5 for pin count-specific PORT I/O implementation.

REGISTER 11-7: RPINR4: PERIPHERAL PIN SELECT INPUT REGISTER 4

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	T5CKR5	T5CKR4	T5CKR3	T5CKR2	T5CKR1	T5CKR0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	T4CKR5	T4CKR4	T4CKR3	T4CKR2	T4CKR1	T4CKR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **T5CKR<5:0>:** Assign Timer5 Clock Input (T5CK) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **T4CKR<5:0>:** Assign Timer4 Clock Input (T4CK) to Corresponding RPn or RPIn Pin bits

REGISTER 11-8: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	IC2R5	IC2R4	IC2R3	IC2R2	IC2R1	IC2R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	IC1R5	IC1R4	IC1R3	IC1R2	IC1R1	IC1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **IC2R<5:0>:** Assign Input Capture 2 (IC2) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IC1R<5:0>:** Assign Input Capture 1 (IC1) to Corresponding RPn or RPIn Pin bits

REGISTER 13-1: TxCON: TIMER2 AND TIMER4 CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
TON	—	TSIDL	—	—	—	TECS1(2)	TECS0(2)
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS0	T32(3)	—	TCS(2)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timerx On bit
When TxCON<3> = 1:
1 = Starts 32-bit Timerx/y
0 = Stops 32-bit Timerx/y
When TxCON<3> = 0:
1 = Starts 16-bit Timerx
0 = Stops 16-bit Timerx

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timerx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9-8 **TECS<1:0>:** Timerx Extended Clock Source Select bits (selected when TCS = 1)(2)
When TCS = 1:
11 = Generic Timer (TMRCK) external input
10 = LPRC Oscillator
01 = TxCK external clock input
00 = SOSC
When TCS = 0:
These bits are ignored; the Timer is clocked from the internal system clock (FOSC/2).

bit 7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timerx Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

Note 1: Changing the value of TxCON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

2: If TCS = 1 and TECS<1:0> = x1, the selected external timer input (TMRCK or TxCK) must be configured to an available RPn/RPIn pin. For more information, see **Section 11.5 "Peripheral Pin Select (PPS)"**.

3: In T4CON, the T45 bit is implemented instead of T32 to select 32-bit mode. In 32-bit mode, the T3CON or T5CON control bits do not affect 32-bit timer operation.

REGISTER 17-7: SPIxIMSKH: SPIx INTERRUPT MASK REGISTER HIGH

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RXWIEN	—	RXMSK5(1)	RXMSK4(1,4)	RXMSK3(1,3)	RXMSK2(1,2)	RXMSK1(1)	RXMSK0(1)
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TXWIEN	—	TXMSK5(1)	TXMSK4(1,4)	TXMSK3(1,3)	TXMSK2(1,2)	TXMSK1(1)	TXMSK0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **RXWIEN:** Receive Watermark Interrupt Enable bit
1 = Triggers receive buffer element watermark interrupt when RXMSK<5:0> ≤ RXELM<5:0>
0 = Disables receive buffer element watermark interrupt

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **RXMSK<5:0>:** RX Buffer Mask bits(1,2,3,4)
RX mask bits; used in conjunction with the RXWIEN bit.

bit 7 **TXWIEN:** Transmit Watermark Interrupt Enable bit
1 = Triggers transmit buffer element watermark interrupt when TXMSK<5:0> = TXELM<5:0>
0 = Disables transmit buffer element watermark interrupt

bit 6 **Unimplemented:** Read as '0'

bit 5-0 **TXMSK<5:0>:** TX Buffer Mask bits(1,2,3,4)
TX mask bits; used in conjunction with the TXWIEN bit.

Note 1: Mask values higher than FIFODEPTH are not valid. The module will not trigger a match for any value in this case.
2: RXMSK2 and TXMSK2 bits are only present when FIFODEPTH = 8 or higher.
3: RXMSK3 and TXMSK3 bits are only present when FIFODEPTH = 16 or higher.
4: RXMSK4 and TXMSK4 bits are only present when FIFODEPTH = 32.

21.0 ENHANCED PARALLEL MASTER PORT (EPMP)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Enhanced Parallel Master Port (EPMP)"** (DS39730). The information in this data sheet supersedes the information in the FRM.

The Enhanced Parallel Master Port (EPMP) module provides a parallel, 4-bit (Master mode only), 8-bit (Master and Slave modes) or 16-bit (Master mode only) data bus interface to communicate with off-chip modules, such as memories, FIFOs, LCD controllers and other microcontrollers. This module can serve as either the master or the slave on the communication bus.

For EPMP Master modes, all external addresses are mapped into the internal Extended Data Space (EDS). This is done by allocating a region of the EDS for each Chip Select (CS), and then assigning each Chip Select to a particular external resource, such as a memory or external controller. This region should not be assigned to another device resource, such as RAM or SFRs. To perform a write or read on an external resource, the CPU simply performs a write or read within the address range assigned for the EPMP.

Key features of the EPMP module are:

- Extended Data Space (EDS) Interface allows Direct Access from the CPU
- Up to 23 Programmable Address Lines
- Up to 2 Chip Select Lines
- Up to 2 Acknowledgment Lines (one per Chip Select)
- 4-Bit, 8-Bit or 16-Bit Wide Data Bus
- Programmable Strobe Options (per Chip Select):
  - Individual Read and Write Strobes or;
  - Read/$\overline{\text{Write}}$ Strobe with Enable Strobe
- Programmable Address/Data Multiplexing
- Programmable Address Wait States
- Programmable Data Wait States (per Chip Select)
- Programmable Polarity on Control Signals (per Chip Select)
- Legacy Parallel Slave Port Support
- Enhanced Parallel Slave Support:
  - Address Support
  - 4-Byte Deep Auto-Incrementing Buffer

21.1 Specific Package Variations

While all PIC24FJ256GA412/GB412 family devices implement the EPMP, I/O pin constraints place some limits on 16-Bit Master mode operations in some package types. This is reflected in the number of dedicated Chip Select pins implemented and the number of dedicated address lines that are available. The differences are summarized in Table 21-1. All available EPMP pin functions are summarized in Table 21-2.

For 64-pin devices, the dedicated Chip Select pins (PMCS1 and PMS2) are not implemented. In addition, only 16 address lines (PMA<15:0>) are available. If required, PMA14 and PMA15 can be remapped to function as APMCS1 and APMCS2 (Alternate Chip Select 1/2), respectively.

The memory space addressable by the device depends on the number of address lines available, as well as the number of Chip Select signals required for the application. Devices with lower pin counts are more affected by Chip Select requirements, as these take away address lines. Table 21-1 shows the maximum addressable range for each pin count.

TABLE 21-1: EPMP FEATURE DIFFERENCES BY DEVICE PIN COUNT

Device	Dedicated Chip Select		Address Lines	Address Range (bytes)		
	CS1	CS2		No CS	1 CS	2 CS
PIC24FJXXXGX406 (64-pin)(1)	—	—	16	64K	32K	16K
PIC24FJXXXGX410 (100-pin)	X	X	23	16M		
PIC24FJXXXGX412 (121-pin)	X	X	23	16M		

Note 1: The 64-pin devices can use the Alternate Chip Select pins, APMCS1 and APMCS2.

REGISTER 22-4: LCDSEx: LCD SEGMENT x ENABLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SE(n+15)(1,2)	SE(n+14)	SE(n+13)	SE(n+12)	SE(n+11)	SE(n+10)	SE(n+9)	SE(n+8)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SE(n+7)	SE(n+6)	SE(n+5)	SE(n+4)	SE(n+3)	SE(n+2)	SE(n+1)	SE(n)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **SE(n+15):SE(n)**: Segment Enable bits
For LCDSE0: n = 0
For LCDSE1: n = 16
For LCDSE2: n = 32
For LCDSE3: n = 48(1,2)
1 = Segment function of the pin is enabled, digital I/O is disabled
0 = Segment function of the pin is disabled, digital I/O is enabled

Note 1: SE63 (LCDSE3<15>) is not implemented.
2: For the SEG49 to work correctly, the JTAG needs to be disabled.

REGISTER 22-5: LCDDATAx: LCD DATA x REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
S(n+15)Cy	S(n+14)Cy	S(n+13)Cy	S(n+12)Cy	S(n+11)Cy	S(n+10)Cy	S(n+9)Cy	S(n+8)Cy
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
S(n+7)Cy	S(n+6)Cy	S(n+5)Cy	S(n+4)Cy	S(n+3)Cy	S(n+2)Cy	S(n+1)Cy	S(n)Cy
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **S(n+15)Cy:S(n)Cy**: Pixel On bits
For Registers, LCDDATA0 through LCDDATA3: n = (16x), y = 0
For Registers, LCDDATA4 through LCDDATA7: n = (16(x – 4)), y = 1
For Registers, LCDDATA8 through LCDDATA11: n = (16(x – 8)), y = 2
For Registers, LCDDATA12 through LCDDATA15: n = (16(x – 12)), y = 3
For Registers, LCDDATA16 through LCDDATA19: n = (16(x – 16)), y = 4
For Registers, LCDDATA20 through LCDDATA23: n = (16(x – 20)), y = 5
For Registers, LCDDATA24 through LCDDATA27: n = (16(x – 24)), y = 6
For Registers, LCDDATA28 through LCDDATA31: n = (16(x – 28)), y = 7
1 = Pixel is on
0 = Pixel is off

REGISTER 24-6: RTCSTATL: RTCC STATUS REGISTER (LOW)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/C-0, HSC	R/W-0, HSC	R/W-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
—	—	ALMEVT	TSBEVT(1)	TSAEVT(1)	SYNC	ALMSYNC	HALFSEC(2)
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5 **ALMEVT:** Alarm Event bit
1 = An alarm event has occurred
0 = An alarm event has not occurred

bit 4 **TSBEVT:** Timestamp B Event bit(1)
1 = A Timestamp B event has occurred
0 = A Timestamp B event has not occurred

bit 3 **TSAEVT:** Timestamp A Event bit(1)
1 = A Timestamp A event has occurred
0 = A Timestamp A event has not occurred

bit 2 **SYNC:** Synchronization Status bit
1 = Time registers may change during software read
0 = Time registers may be read safely

bit 1 **ALMSYNC:** Alarm Synchronization Status bit
1 = Alarm registers (ALMTIME, ALMDATE) and AMASKx bits should not be modified and Alarm Control registers (ALRMEN, ALMRPT<7:0>) may change during software read
0 = Alarm registers and Alarm Control registers may be written/modified safely

bit 0 **HALFSEC:** Half Second Status bit(2)
1 = Second half of 1-second period
0 = First half of 1-second period

Note 1: User software may write a '1' to this location to initiate a Timestamp A event; timestamp capture is not valid until TSAEVT reads as '1'.

2: This bit is read-only; it is cleared to '0' on a write to the SECONE<3:0> bits in Register 24-7.

25.8 Generating a Pseudorandom Number (PRN)

For operations that require a Pseudorandom Number (PRN), the method outlined in NIST SP800-90 can be adapted for efficient use with the Cryptographic Engine. This method uses the AES algorithm in CTR mode to create PRNs with minimal CPU overhead. PRNs generated in this manner can be used for cryptographic purposes or any other purpose that the host application may require.

The random numbers used as initial seeds can be taken from any source convenient to the user's application. If possible, a non-deterministic random number source should be used.

Note:	PRN generation is not available when software keys are disabled (SWKYDIS = 1).

To perform the initial reseeding operation, and subsequent reseedings after the reseeding interval has expired:

1. Store a random number (128 bits) in CRYTXTA.
2. For the initial generation ONLY, use a key value of 0h (128 bits) and a counter value of 0h.
3. Configure the engine for AES encryption, CTR mode (OPMOD<3:0> = 0000, CPHRSEL = 1, CPHRMOD<2:0> = 100).
4. Perform an encrypt operation by setting CRYGO.
5. Move the results in CRYTXTC to RAM. This is the New Key Value (NEW_KEY).
6. Store another random number (128 bits) in CRYTXTA.
7. Configure the module for encryption as in Step 3.
8. Perform an encrypt operation by setting CRYGO.
9. Store this value in RAM. This is the New Counter Value (NEW_CTR).
10. For subsequent reseeding operations, use NEW_KEY and NEW_CTR for the starting key and counter values.

To generate the Pseudorandom Number:

1. Load NEW_KEY value from RAM into CRYKEY.
2. Load NEW_CTR value from RAM into CRYTXTB.
3. Load CRYTXTA with 0h (128 bits).
4. Configure the engine for AES encryption, CTR mode (OPMOD<3:0> = 0000, CPHRSEL = 1, CPHRMOD<2:0> = 100).
5. Perform an encrypt operation by setting CRYGO.
6. Copy the generated PRN in CRYTXTC (PRNG_VALUE) to RAM.
7. Repeat the encrypt operation.
8. Store the value of CRYTXTC from this round as the new value of NEW_KEY.
9. Repeat the encrypt operation.
10. Store the value of CRYTXTC from this round as the new value of NEW_CTR.

Subsequent PRNs can be generated by repeating this procedure until the reseeding interval has expired. At that point, the reseeding operation is performed using the stored values of NEW_KEY and NEW_CTR.

25.9 Generating a True Random Number

1. Enable the Cryptographic mode (CRYON (CRYCONL<15>) = 1).
2. Set the OPMOD<3:0> bits to '1010'.
3. Start the request by setting the CRYGO bit (CRYCONL<8>) to '1'.
4. Wait for the CRYGO bit to be cleared to '0' by the hardware.
5. Read the random number from the CRYTXTA register.

25.10 Testing the Key Source Configuration

The validity of the key source configuration can always be tested by writing the appropriate register bits and then reading the KEYFAIL register bit. No operation needs to be started to perform this check; the module does not even need to be enabled.

REGISTER 25-5: CFGPAGE: SECURE ARRAY CONFIGURATION BITS (OTP PAGE 0) REGISTER (CONTINUED)

bit 21-20 **KEY1TYPE<1:0>:** Key Type for OTP Pages 1 and 2 bits
11 = Keys in these pages are for 192-bit/256-bit AES operations only
10 = Keys in these pages are for 128-bit AES operations only
01 = Keys in these pages are for 3DES operations only
00 = Keys in these pages are for DES/2DES operations only

bit 19 **SKEYEN:** Session Key Enable bit
1 = Stored Key #1 may be used only as a Key Encryption Key
0 = Stored Key #1 may be used for any operation

bit 18-11 **LKYSRC<7:0>:** Locked Key Source Configuration bits
If SRCLCK = 1:
1xxxxxxx = Key source is as if KEYSRC<3:0> = 1111
01xxxxxx = Key source is as if KEYSRC<3:0> = 0111
001xxxxx = Key source is as if KEYSRC<3:0> = 0110
0001xxxx = Key source is as if KEYSRC<3:0> = 0101
00001xxx = Key source is as if KEYSRC<3:0> = 0100
000001xx = Key source is as if KEYSRC<3:0> = 0011
0000001x = Key source is as if KEYSRC<3:0> = 0010
00000001 = Key source is as if KEYSRC<3:0> = 0001
00000000 = Key source is as if KEYSRC<3:0> = 0000
If SRCLCK = 0:
These bits are ignored.

bit 10 **SRCLCK:** Key Source Lock bit
1 = The key source is determined by the LKYSRC<7:0> bits (software key selection is disabled)
0 = The key source is determined by the KEYSRC<3:0> (CRYCONH<3:0>) bits (locked key selection is disabled)

bit 9-1 **WRLOCK<8:0>:** Write Lock Page Enable bits
For OTP Pages 0 (CFGPAGE) through 8:
1 = OTP Page is permanently locked and may not be programmed
0 = OTP Page is unlocked and may be programmed

bit 0 **SWKYDIS:** Software Key Disable bit
1 = Software key (CRYKEY register) is disabled; when KEYSRC<3:0> = 0000, the KEYFAIL status bit will be set and no encryption/decryption/session key operations can be started until KEYSRC<3:0> bits are changed to a value other than '0000'
0 = Software key (CRYKEY register) can be used as a key source when KEYSRC<3:0> = 0000

Note 1: This bit's state is mirrored by the PGMTST bit (CRYOTP<7>).

REGISTER 27-7: ANCFG: A/D BAND GAP REFERENCE CONFIGURATION(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	VBG6USB	VBG2CMP	VBGDAC	VBGAN	VBGADC	VBGEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5 **VBG6USB:** USB OTG $V_{BG}/6$ Input Enable bit
1 = Band gap voltage, divided by six reference ($V_{BG}/6$), is enabled
0 = Band gap voltage, divided by six reference ($V_{BG}/6$), is disabled

bit 4 **VBG2CMP:** Comparator $V_{BG}/2$ Input Enable bit
1 = Band gap voltage, divided by two reference ($V_{BG}/2$), is enabled
0 = Band gap voltage, divided by two reference ($V_{BG}/2$), is disabled

bit 3 **VBGDAC:** DAC Input Band Gap Reference Enable bit
1 = Band gap voltage reference (V_{BG}) is enabled
0 = Band gap voltage reference (V_{BG}) is disabled

bit 2 **VBGAN:** Analog Module V_{BG} Input Enable bit
1 = Band gap voltage reference (V_{BG}) is enabled
0 = Band gap voltage reference (V_{BG}) is disabled

bit 1 **VBGADC:** A/D Input V_{BG} Enable bit
1 = Band gap voltage reference (V_{BG}) is enabled
0 = Band gap voltage reference (V_{BG}) is disabled

bit 0 **VBGEN:** General Resource V_{BG} Enable bit
1 = Band gap voltage reference (V_{BG}) is enabled
0 = Band gap voltage reference (V_{BG}) is disabled

Note 1: Band gap references are automatically enabled when their consumer modules request these resources, and disabled when the modules are disabled or do not require them. The individual control bits permit manual control of the band gap references.The state of the bits does not necessarily reflect the status of the associated reference and should not be used as a status flag.

REGISTER 31-3: CTMUCON2L: CTMU CONTROL 2 LOW REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	IRSTEN	—	DSCH2	DSCH1	DSCH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4 **IRSTEN:** Current Source Reset Enable bit
1 = Current source is reset by the IDISSEN bit or by a source selected by DSCH<2:0>
0 = Edge detect logic does not occur

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **DSCH<2:0>:** Discharge Trigger Source Select bits
111 = CLC2 output
110 = CLC1 output
101 = Unimplemented
100 = A/D end of conversion event
011 = SCCP5 auxiliary output
010 = SCCP2 auxiliary output
001 = MCCP1 auxiliary output
000 = Unimplemented

34.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

34.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

34.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

34.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

34.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.