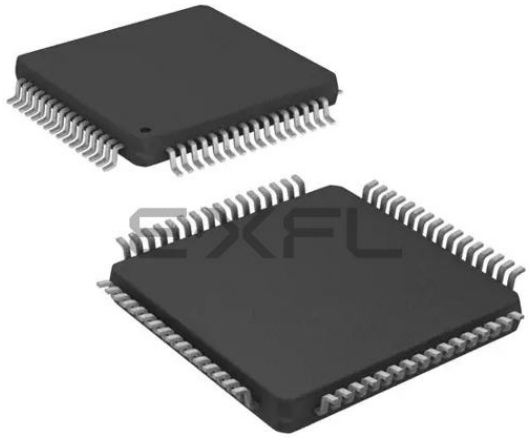

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Details	
Product Status	Active
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Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128gb406-i-pt

4.3.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® MCUs and improve Data Space memory usage efficiency, the PIC24F instruction set supports both word and byte operations. As a consequence of byte accessibility, all EA calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] will result in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

Data byte reads will read the complete word, which contains the byte, using the LSB of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode, but separate write lines. Data byte writes only write to the corresponding side of the array or register which matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap will be generated. If the error occurred on a read, the instruction underway is completed; if it occurred on a write, the instruction will be executed but the write will not occur. In either case, a trap is then executed, allowing the system and/or user to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB. The Most Significant Byte (MSB) is not modified.

A Sign-Extend (SE) instruction is provided to allow users to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, users can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

Although most instructions are capable of operating on word or byte data sizes, it should be noted that some instructions operate only on words.

4.3.3 NEAR DATA SPACE

The 8-Kbyte area between 0000h and 1FFFh is referred to as the Near Data Space. Locations in this space are directly addressable via a 13-bit absolute address field within all memory direct instructions. The remainder of the Data Space is addressable indirectly. Additionally, the whole Data Space is addressable using MOV instructions, which support Memory Direct Addressing with a 16-bit address field.

4.3.4 SPECIAL FUNCTION REGISTER (SFR) SPACE

The first 2 Kbytes of the Near Data Space, from 0000h to 07FFh, are primarily occupied with Special Function Registers (SFRs). These are used by the PIC24F core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by module. A diagram of the SFR space, showing where the SFRs are actually implemented, is shown in Table 4-4. Each implemented area indicates a 32-byte region where at least one address is implemented as an SFR. A complete list of implemented SFRs, including their addresses, is shown in Tables 4-5 through 4-12.

TABLE 4-4: IMPLEMENTED REGIONS OF SFR DATA SPACE

	SFR Space Address							
	xx00	**xx20**	**xx40**	**xx60**	**xx80**	**xxA0**	**xxC0**	**xxE0**
000h	Core		—		Interrupts			—
100h	System	EPMP	CRC(1)	PMD	Timers	—	CTM	RTCC
200h	Capture	Compare		MCCP				CMP/DAC
300h	SCCP				UART			UART/SPI
400h	SPI		CLC		I^2C		DMA	
500h	DMA	Crypto Engine		USB(2)			LCD	
600h	LCD	—	I/O					
700h	I/O	A/D	NVM	—	PPS			—

Legend: — = Block is largely or entirely unimplemented.

Note 1: This region includes system control registers (Reference Oscillator).

2: Implemented in PIC24FJXXXGBXXX devices only.

TABLE 4-7: SFR BLOCK 200h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
Input Capture			OC4CON2	250	0000000000001100	CCP2PRH	2A6	1111111111111111
IC1CON1	200	0000000000000000	OC4RS	252	xxxxxxxxxxxxxxxx	CCP2RAL	2A8	0000000000000000
IC1CON2	202	0000000000001101	OC4R	254	xxxxxxxxxxxxxxxx	CCP2RBL	2AC	0000000000000000
IC1BUF	204	0000000000000000	OC4TMR	256	xxxxxxxxxxxxxxxx	CCP2BUFL	2B0	0000000000000000
IC1TMR	206	0000000000000000	OC5CON1	258	0000000000000000	CCP2BUFH	2B2	0000000000000000
IC2CON1	208	0000000000000000	OC5CON2	25A	0000000000001100	CCP3CON1L	2B4	0000000000000000
IC2CON2	20A	0000000000001101	OC5RS	25C	xxxxxxxxxxxxxxxx	CCP3CON1H	2B6	0000000000000000
IC2BUF	20C	0000000000000000	OC5R	25E	xxxxxxxxxxxxxxxx	CCP3CON2L	2B8	0000000000000000
IC2TMR	20E	0000000000000000	OC5TMR	260	xxxxxxxxxxxxxxxx	CCP3CON2H	2BA	0000000100000000
IC3CON1	210	0000000000000000	OC6CON1	262	0000000000000000	CCP3CON3H	2BE	0000000000000000
IC3CON2	212	0000000000001101	OC6CON2	264	0000000000001100	CCP3STATL	2C0	0000000000xx0000
IC3BUF	214	0000000000000000	OC6RS	266	xxxxxxxxxxxxxxxx	CCP3STATH	2C2	0000000000000000
IC3TMR	216	0000000000000000	OC6R	268	xxxxxxxxxxxxxxxx	CCP3TMRL	2C4	0000000000000000
IC4CON1	218	0000000000000000	OC6TMR	26A	xxxxxxxxxxxxxxxx	CCP3TMRH	2C6	0000000000000000
IC4CON2	21A	0000000000001101	**CCP/Timer (MCCP)**			CCP3PRL	2C8	1111111111111111
IC4BUF	21C	0000000000000000	CCP1CON1L	26C	0000000000000000	CCP3PRH	2CA	1111111111111111
IC4TMR	21E	0000000000000000	CCP1CON1H	26E	0000000000000000	CCP3RAL	2CC	0000000000000000
IC5CON1	220	0000000000000000	CCP1CON2L	270	0000000000000000	CCP3RBL	2D0	0000000000000000
IC5CON2	222	0000000000001101	CCP1CON2H	272	0000000100000000	CCP3BUFL	2D4	0000000000000000
IC5BUF	224	0000000000000000	CCP1CON3L	274	0000000000000000	CCP3BUFH	2D6	0000000000000000
IC5TMR	226	0000000000000000	CCP1CON3H	276	0000000000000000	**Comparator/DAC/Analog Pin Control**		
IC6CON1	228	0000000000000000	CCP1STATL	278	0000000000xx0000	CMSTAT	2E6	0000000000000000
IC6CON2	22A	0000000000001101	CCP1STATH	27A	0000000000000000	CVRCON	2E8	0000000000000000
IC6BUF	22C	0000000000000000	CCP1TMRL	27C	0000000000000000	CM1CON	2EA	0000000000000000
IC6TMR	22E	0000000000000000	CCP1TMRH	27E	0000000000000000	CM2CON	2EC	0000000000000000
Output Compare/PWM			CCP1PRL	280	1111111111111111	CM3CON	2EE	0000000000000000
OC1CON1	230	0000000000000000	CCP1PRH	282	1111111111111111	ANCFG	2F4	0000000000000000
OC1CON2	232	0000000000001100	CCP1RAL	284	0000000000000000	DAC1CON	2F8	0000000000000000
OC1RS	234	xxxxxxxxxxxxxxxx	CCP1RBL	288	0000000000000000	DAC1DAT	2FA	0000000000000000
OC1R	236	xxxxxxxxxxxxxxxx	CCP1BUFL	28C	0000000000000000			
OC1TMR	238	xxxxxxxxxxxxxxxx	CCP1BUFH	28E	0000000000000000			
OC2CON1	23A	0000000000000000	**CCP/Timer (SCCP)**					
OC2CON2	23C	0000000000001100	CCP2CON1L	290	0000000000000000			
OC2RS	23E	xxxxxxxxxxxxxxxx	CCP2CON1H	292	0000000000000000			
OC2R	240	xxxxxxxxxxxxxxxx	CCP2CON2L	294	0000000000000000			
OC2TMR	242	xxxxxxxxxxxxxxxx	CCP2CON2H	296	0000000100000000			
OC3CON1	244	0000000000000000	CCP2CON3H	29A	0000000000000000			
OC3CON2	246	0000000000001100	CCP2STATL	29C	0000000000xx0000			
OC3RS	248	xxxxxxxxxxxxxxxx	CCP2STATH	29E	0000000000000000			
OC3R	24A	xxxxxxxxxxxxxxxx	CCP2TMRL	2A0	0000000000000000			
OC3TMR	2AC	xxxxxxxxxxxxxxxx	CCP2TMRH	2A2	0000000000000000			
OC4CON1	24E	0000000000000000	CCP2PRL	2A4	1111111111111111			

Legend: x = unknown or indeterminate value. Reset and address values are in hexadecimal.

TABLE 4-9: SFR BLOCK 400h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
SPI (Continued)			**CLC**			I2C3ADD	4C0	0000000000000000
SPI1BUFL	400	0000000000000000	CLC1CONL	464	0000000000000000	I2C3MSK	4C2	0000000000000000
SPI1BUFH	402	0000000000000000	CLC1CONH	466	0000000000000000	**DMA**		
SPI1BRGL	404	000xxxxxxxxxxxx	CLC1SEL	468	0000000000000000	DMACON	4C4	0000000000000000
SPI1IMSKL	408	0000000000000000	CLC1GLSL	46C	0000000000000000	DMABUF	4C6	0000000000000000
SPI1IMSKH	40A	0000000000000000	CLC1GLSH	46E	0000000000000000	DMAL	4C8	0000000000000000
SPI1URDTL	40C	0000000000000000	CLC2CONL	470	0000000000000000	DMAH	4CA	0000000000000000
SPI1URDTH	40E	0000000000000000	CLC2CONH	472	0000000000000000	DMACH0	4CC	0000000000000000
SPI2CON1L	410	0000000000000000	CLC2SEL	474	0000000000000000	DMAINT0	4CE	0000000000000000
SPI2CON1H	412	0000000000000000	CLC2GLSL	478	0000000000000000	DMASRC0	4D0	0000000000000000
SPI2CON2L	414	0000000000000000	CLC2GLSH	47A	0000000000000000	DMADST0	4D2	0000000000000000
SPI2STATL	418	0000000000101000	CLC3CONL	47C	0101001100011000	DMACNT0	4D4	0000000000000001
SPI2STATH	41A	0000000000000000	CLC3CONH	47E	0000000000000000	DMACH1	4D6	0000000000000000
SPI2BUFL	41C	0000000000000000	CLC3SEL	480	0000000000000000	DMAINT1	4D8	0000000000000000
SPI2BUFH	41E	0000000000000000	CLC3GLSL	484	0000000000000000	DMASRC1	4DA	0000000000000000
SPI2BRGL	420	000xxxxxxxxxxxx	CLC3GLSH	486	0000000000000000	DMADST1	4DC	0000000000000000
SPI2IMSKL	424	0000000000000000	CLC4CONL	488	0000000000000000	DMACNT1	4DE	0000000000000001
SPI2IMSKH	426	0000000000000000	CLC4CONH	48A	0000000000000000	DMACH2	4E0	0000000000000000
SPI2URDTL	428	0000000000000000	CLC4SEL	48C	0000000000000000	DMAINT2	4E2	0000000000000000
SPI2URDTH	42A	0000000000000000	CLC4GLSL	490	0000000000000000	DMASRC2	4E4	0000000000000000
SPI3CON1L	42C	0000000000000000	CLC4GLSH	492	0000000000000000	DMADST2	4E6	0000000000000000
SPI3CON1H	42E	0000000000000000	**I²C**			DMACNT2	4E8	0000000000000001
SPI3CON2L	430	0000000000000000	I2C1RCV	494	0000000000000000	DMACH3	4EA	0000000000000000
SPI3STATL	434	0000000000101000	I2C1TRN	496	0000000011111111	DMAINT3	4EC	0000000000000000
SPI3STATH	436	0000000000000000	I2C1BRG	498	0000000000000000	DMASRC3	4EE	0000000000000000
SPI3BUFL	438	0000000000000000	I2C1CONL	49A	0001000000000000	DMADST3	4F0	0000000000000000
SPI3BUFH	43A	0000000000000000	I2C1CONH	49C	0000000000000000	DMACNT3	4F2	0000000000000001
SPI3BRGL	43C	000xxxxxxxxxxxx	I2C1STAT	49E	0000000000000000	DMACH4	4F4	0000000000000000
SPI3IMSKL	440	0000000000000000	I2C1ADD	4A0	0000000000000000	DMAINT4	4F6	0000000000000000
SPI3IMSKH	442	0000000000000000	I2C1MSK	4A2	0000000000000000	DMASRC4	4F8	0000000000000000
SPI3URDTL	444	0000000000000000	I2C2RCV	4A4	0000000000000000	DMADST4	4FA	0000000000000000
SPI3URDTH	446	0000000000000000	I2C2TRN	4A6	0000000011111111	DMACNT4	4FC	0000000000000001
SPI4CON1L	448	0000000000000000	I2C2BRG	4A8	0000000000000000	DMACH5	4FE	0000000000000000
SPI4CON1H	44A	0000000000000000	I2C2CONL	4AA	0001000000000000			
SPI4CON2L	44C	0000000000000000	I2C2CONH	4AC	0000000000000000			
SPI4STATL	450	0000000000101000	I2C2STAT	4AE	0000000000000000			
SPI4STATH	452	0000000000000000	I2C2ADD	4B0	0000000000000000			
SPI4BUFL	454	0000000000000000	I2C2MSK	4B2	0000000000000000			
SPI4BUFH	456	0000000000000000	I2C3RCV	4B4	0000000000000000			
SPI4BRGL	458	000xxxxxxxxxxxx	I2C3TRN	4B6	0000000011111111			
SPI4IMSKL	45C	0000000000000000	I2C3BRG	4B8	0000000000000000			
SPI4IMSKH	45E	0000000000000000	I2C3CONL	4BA	0001000000000000			
SPI4URDTL	460	0000000000000000	I2C3CONH	4BC	0000000000000000			
SPI4URDTH	462	0000000000000000	I2C3STAT	4BE	0000000000000000			

Legend: x = unknown or indeterminate value. Reset and address values are in hexadecimal.

REGISTER 8-2: CORCON: CPU CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/C-0	r-1	U-0	U-0
—	—	—	—	IPL3(1)	—	—	—
bit 7							bit 0

Legend:	r = Reserved bit	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit(1)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

bit 2 **Reserved:** Read as '1'

bit 1-0 **Unimplemented:** Read as '0'

Note 1: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level; see Register 3-2 for bit description.

REGISTER 8-19: IEC5: INTERRUPT ENABLE CONTROL REGISTER 5 (CONTINUED)

bit 3 **U3TXIE:** UART3 Transmitter Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **U3RXIE:** UART3 Receiver Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **U3ERIE:** UART3 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **Unimplemented:** Read as '0'

REGISTER 8-26: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CNIP2	CNIP1	CNIP0	—	CMIP2	CMIP1	CMIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **CNIP<2:0>:** Input Change Notification Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **CMIP<2:0>:** Comparator Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **MI2C1IP<2:0>:** Master I2C1 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **SI2C1IP<2:0>:** Slave I2C1 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-50: IPC28: INTERRUPT PRIORITY CONTROL REGISTER 28

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U6TXIP2	U6TXIP1	U6TXIP0	—	U6RXIP2	U6RXIP1	U6RXIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U5ERIP2	U5ERIP1	U5ERIP0	—	U5TXIP2	U5TXIP1	U5TXIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **U6TXIP<2:0>:** UART6 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **U6RXIP<2:0>:** UART6 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **U5ERIP<2:0>:** UART5 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **U5TXIP<2:0>:** UART5 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

9.3 Control Registers

The operation of the oscillator is controlled by three Special Function Registers:

- OSCCON
- CLKDIV
- OSCTUN

The OSCCON register (Register 9-1) is the main control register for the oscillator. It controls clock source switching and allows the monitoring of clock sources. OSCCON is protected by a write lock to prevent inadvertent clock switches. See **Section 9.4 "Clock Switching Operation"** for more information.

The CLKDIV register (Register 9-2) controls the features associated with Doze mode, as well as the postscaler for the FRC Oscillator.

The OSCTUN register (Register 9-3) allows the user to fine-tune the FRC Oscillator over a range of approximately ±1.5%. It also controls the FRC self-tuning features, described in **Section 9.5 "FRC Active Clock Tuning"**.

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER

U-0	R-0	R-0	R-0	U-0	R/W-x(1)	R/W-x(1)	R/W-x(1)
—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0
bit 15							bit 8

R/SO-0	R/W-0	R-0(3)	U-0	R/CO-0	R/W-0	R/W-0	R/W-0
CLKLOCK	IOLOCK(2)	LOCK	—	CF	POSCEN	SOSCEN	OSWEN
bit 7							bit 0

Legend:	CO = Clearable Only bit	SO = Settable Only bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits
111 = Fast RC Oscillator with Postscaler (FRCDIV)
110 = Reserved
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator with Postscaler and PLL module (FRCPLL)(4)
000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits(1)
111 = Fast RC Oscillator with Postscaler (FRCDIV)
110 = Reserved
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator with Postscaler and PLL module (FRCPLL)(4)
000 = Fast RC Oscillator (FRC)

Note 1: Reset values for these bits are determined by the FNOSCx Configuration bits.

2: The state of the IOLOCK bit can only be changed once an unlocking sequence has been executed. In addition, if the IOL1WAY Configuration bit is '1' once the IOLOCK bit is set, it cannot be cleared.

3: This bit also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.

4: The default divisor of the postscaler is 2, which will generate a 4 MHz clock to the PLL module.

REGISTER 9-5: REFOCONH: REFERENCE CLOCK CONTROL HIGH REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RODIV<14:8>						
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RODIV<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-0 **RODIV<14:0>:** Reference Clock Integer Divisor Select bits
Divisor for the selected input clock source is two times the selected value.
111 1111 1111 1111 = Base clock value divided by 65,534 (2 * 7FFFh)
111 1111 1111 1110 = Base clock value divided by 65,532 (2 * 7FFEh)
111 1111 1111 1101 = Base clock value divided by 65,530 (2 * 7FFDh)
• • •
000 0000 0000 0010 = Base clock value divided by 4 (2 * 2)
000 0000 0000 0001 = Base clock value divided by 2 (2 * 1)
000 0000 0000 0000 = Base clock value

REGISTER 9-6: REFOTRIML: REFERENCE CLOCK TRIM REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROTRIM<8:1>							
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
ROTRIM0	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **ROTRIM<8:0>:** Reference Clock Fractional Divisor Select bits
Added fractional portion of the divisor for the selected input clock source is the value, divided by 512.
111111111 = 1 (512/512)
111111110 = 0.998947 (511/512)
111111101 = 0.996094 (510/512)
• • •
000000010 = 0.003906 (2/512)
000000001 = 0.001953 (1/512)
000000000 = No fractional portion (0/512)

bit 6-0 **Unimplemented:** Read as '0'

TABLE 11-4: PORTC REGISTER MAP(1)

Register Name	Bit Range	Bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANSC	15:0	—	—	—	—	—	—	—	—	—	—	—	ANSC<4:1>				—
TRISC	15:0	TRISC15	—	—	TRISC12	—	—	—	—	—	—	—	TRISC<4:1>				—
PORTC	15:0	PORTC<15:12>				—	—	—	—	—	—	—	PORTC<4:1>				—
LATC	15:0	LATC15	—	—	LATC12	—	—	—	—	—	—	—	LATC<4:1>				—
ODCC	15:0	ODCC15	—	—	ODCC12	—	—	—	—	—	—	—	ODCC<4:1>				—
IOCPC	15:0	IOCPC<15:12>				—	—	—	—	—	—	—	IOCPC<4:1>				—
IOCNC	15:0	IOCNC<15:12>				—	—	—	—	—	—	—	IOCNC<4:1>				—
IOCFC	15:0	IOCFC<15:12>				—	—	—	—	—	—	—	IOCFC<4:1>				—
IOCPUC	15:0	IOCPUC<15:12>				—	—	—	—	—	—	—	IOCPUC<4:1>				—
IOCPDC	15:0	IOCPDC<15:12>				—	—	—	—	—	—	—	IOCPDC<4:1>				—

Legend: — = unimplemented, read as '0'.

Note 1: PORT register maps show full pin count devices. Please refer to Table 1-4 and Table 1-5 for pin count-specific PORT I/O implementation.

TABLE 11-5: PORTD REGISTER MAP(1)

Register Name	Bit Range	Bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANSD	15:0	ANSD<15:0>															
TRISD	15:0	TRISD<15:0>															
PORTD	15:0	PORTD<15:0>															
LATD	15:0	LATD<15:0>															
ODCD	15:0	ODCD<15:0>															
IOCPD	15:0	IOCPD<15:0>															
IOCND	15:0	IOCND<15:0>															
IOCFD	15:0	IOCFD<15:0>															
IOCPUD	15:0	IOCPUD<15:0>															
IOCPDD	15:0	IOCPDD<15:0>															

Legend: — = unimplemented, read as '0'.

Note 1: PORT register maps show full pin count devices. Please refer to Table 1-4 and Table 1-5 for pin count-specific PORT I/O implementation.

TABLE 11-6: PORTE REGISTER MAP(1)

Register Name	Bit Range	Bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANSE	15:0	—	—	—	—	—	—	ANSE<9:0>									
TRISE	15:0	—	—	—	—	—	—	TRISE<9:0>									
PORTE	15:0	—	—	—	—	—	—	PORTE<9:0>									
LATE	15:0	—	—	—	—	—	—	LATE<9:0>									
ODCE	15:0	—	—	—	—	—	—	ODCE<9:0>									
IOCPE	15:0	—	—	—	—	—	—	IOCPE<9:0>									
IOCNE	15:0	—	—	—	—	—	—	IOCNE<9:0>									
IOCFE	15:0	—	—	—	—	—	—	IOCFE<9:0>									
IOCPUE	15:0	—	—	—	—	—	—	IOCPUE<9:0>									
IOCPDE	15:0	—	—	—	—	—	—	IOCPDE<9:0>									

Legend: — = unimplemented, read as '0'.

Note 1: PORT register maps show full pin count devices. Please refer to Table 1-4 and Table 1-5 for pin count-specific PORT I/O implementation.

TABLE 11-7: PORTF REGISTER MAP(1)

Register Name	Bit Range	Bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANSF	15:0	—	—	ANSF<13:12>		—	—	—	ANSF8	—	—	ANSF<5:0>					
TRISF	15:0	—	—	TRISF<13:12>		—	—	—	TRISF<8:0>(2)								
PORTF	15:0	—	—	PORTF<13:12>		—	—	—	PORTF<8:0>								
LATF	15:0	—	—	LATF<13:12>		—	—	—	LATF<8:0>								
ODCF	15:0	—	—	ODCF<13:12>		—	—	—	ODCF<8:0>								
IOCPF	15:0	—	—	IOCPF<13:12>		—	—	—	IOCPF<8:7>		—	IOCPF<5:0>					
IOCNF	15:0	—	—	IOCNF<13:12>		—	—	—	IOCNF<8:7>		—	IOCNF<5:0>					
IOCFF	15:0	—	—	IOCFF<13:12>		—	—	—	IOCFF<8:7>		—	IOCFF<5:0>					
IOCPUF	15:0	—	—	IOCPUF<13:12>		—	—	—	IOCPUF<8:7>		—	IOCPUF<5:0>					
IOCPDF	15:0	—	—	IOCPDF<13:12>		—	—	—	IOCPDF<8:7>		—	IOCPDF<5:0>					

Legend: — = unimplemented, read as '0'.

Note 1: PORT register maps show full pin count devices. Please refer to Table 1-4 and Table 1-5 for pin count-specific PORT I/O implementation.

2: TRISF6 is only available on PIC24FJXXXGB4XX devices.

14.0 CAPTURE/COMPARE/PWM/ TIMER MODULES (MCCP AND SCCP)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the MCCP/SCCP modules, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Capture/Compare/PWM/Timer (MCCP and SCCP)"** (DS33035). The information in this data sheet supersedes the information in the FRM.

PIC24FJ256GA412/GB412 family devices include several Capture/Compare/PWM/Timer base modules, which provide the functionality of three different peripherals of earlier PIC24F devices. The module can operate in one of three major modes:

- General Purpose Timer
- Input Capture
- Output Compare/PWM

The module is provided in two different forms, distinguished by the number of PWM outputs that the module can generate. Single output modules (SCCPs) provide only one PWM output. Multiple output modules (MCCPs) can provide up to six outputs and an extended range of power control features, depending on the pin count of the particular device. All other features of the modules are identical.

The SCCP and MCCP modules can be operated only in one of the three major modes at any time. The other modes are not available unless the module is reconfigured for the new mode.

A conceptual block diagram for the module is shown in Figure 14-1. All three modes share a time base generator and a common Timer register pair (CCPxTMRH/L); other shared hardware components are added as a particular mode requires.

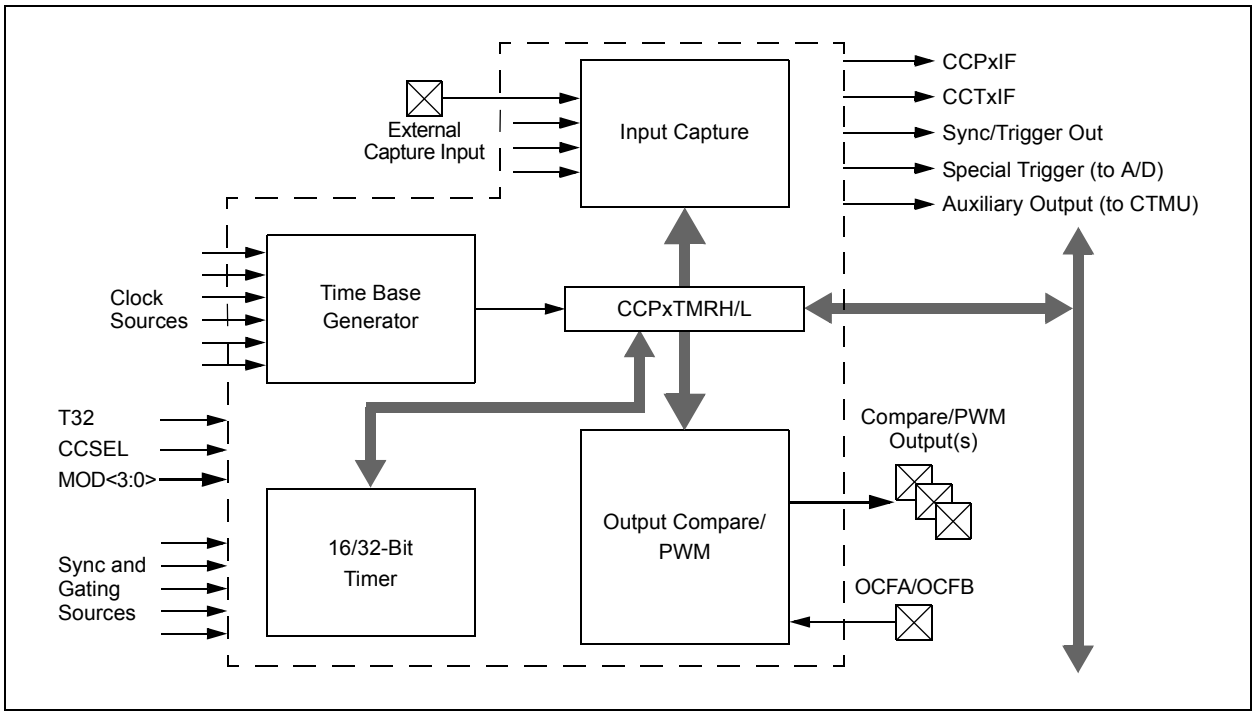
Each module has a total of seven control and status registers:

- CCPxCON1L (Register 14-1)
- CCPxCON1H (Register 14-2)
- CCPxCON2L (Register 14-3)
- CCPxCON2H (Register 14-4)
- CCPxCON3L (Register 14-5)
- CCPxCON3H (Register 14-6)
- CCPxSTATL (Register 14-7)

Each module also includes eight buffer/counter registers that serve as Timer Value registers or data holding buffers:

- CCPxTMRH/CCPxTMRL (CCPx Timer High/Low Counters)
- CCPxPRH/CCPxPRL (CCPx Timer Period High/Low)
- CCPxRAH/CCPxRAL (CCPx Primary Output Compare Data High/Low Buffers)
- CCPxRBH/CCPxRBL (CCPx Secondary Output Compare Data High/Low Buffers)

FIGURE 14-1: MCCPx/SCCPx CONCEPTUAL BLOCK DIAGRAM



REGISTER 20-13: U1CNFG2: USB CONFIGURATION REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	U-0	U-0	r-0	r-0
—	—	—	PUVBUS(1)	—	—	—	—
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4 **PUVBUS:** VBUS Pull-Up Enable bit(1)
1 = Pull-up on VBUS pin is enabled
0 = Pull-up on VBUS pin is disabled

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **Reserved:** Maintain as '0'

Note 1: Never change this bit while the USBPWR bit is set (U1PWRC<0> = 1).

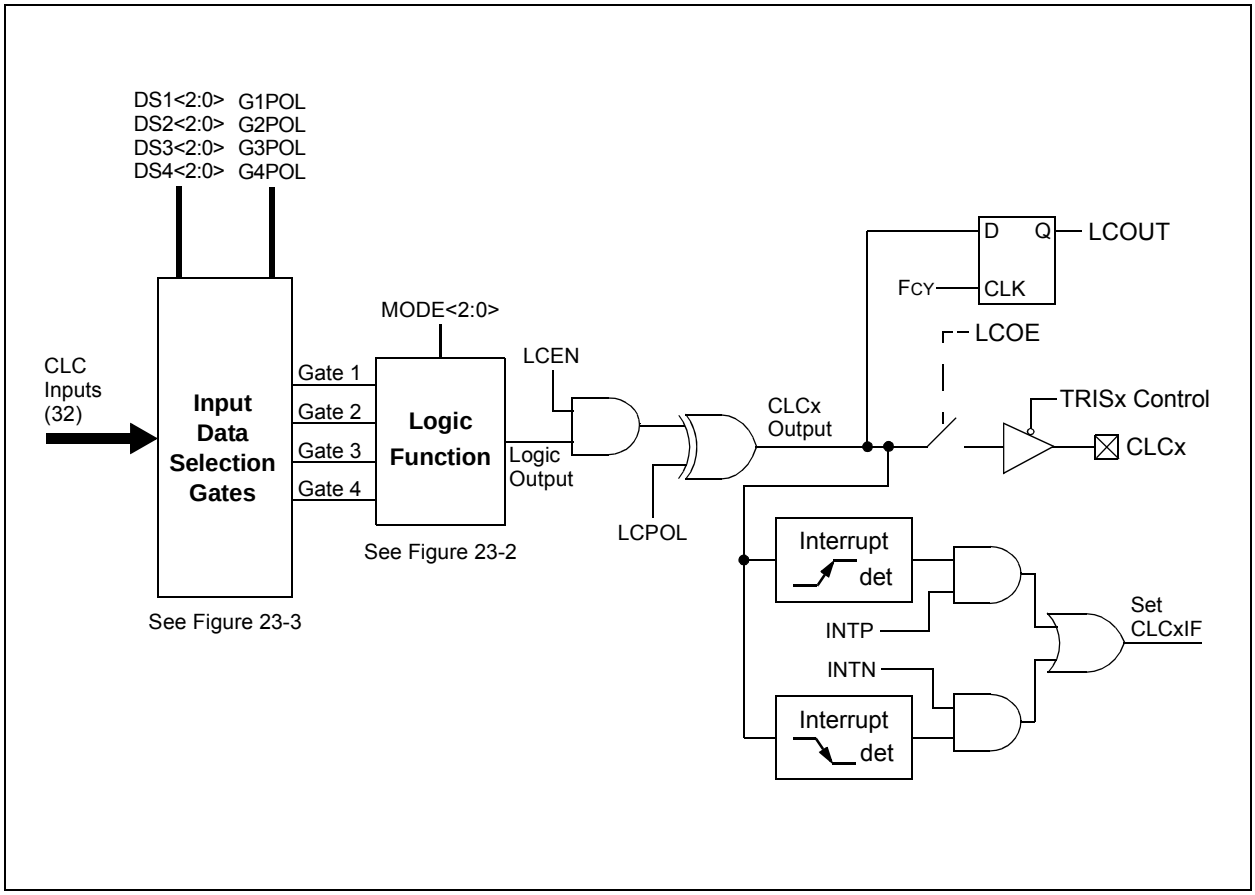
23.0 CONFIGURABLE LOGIC CELL (CLC)

Note: This data sheet summarizes the features of the PIC24FJ256GA412/GB412 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Configurable Logic Cell (CLC)"** (DS33949), which is available from the Microchip web site (www.microchip.com).

The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins. This provides greater flexibility and potential in embedded designs since the CLC module can operate outside the limitations of software execution and supports a vast amount of output designs.

There are four input gates to the selected logic function. These four input gates select from a pool of up to 32 signals that are selected using four data source selection multiplexers. Figure 23-1 shows an overview of the module. Figure 23-3 shows the details of the data source multiplexers and logic input gate connections.

FIGURE 23-1: CLCx MODULE



24.3 Power Control

The RTCC includes a power control feature that allows the device to periodically wake-up an external device, wait for the device to be stable before sampling wake-up events from that device and then shut down the external device. This can be done completely autonomously by the RTCC, without the need to wake from the current lower power mode.

To use this feature:

1. Enable the RTCC (RTCEN = 1).
2. Set the PWCEN bit (RTCCON1L<10>).
3. Configure the RTCC pin to drive the PWC control signal (RTCOE = 1 and OUTSEL<2:0> = 011).

The polarity of the PWC control signal is selected by the PWCPOL bit (RTCCON1L<9>). An active-low or active-high signal may be used with the appropriate external switch to turn on or off the power to one or more external devices. The active-low setting may also be used in conjunction with an open-drain setting on the RTCC pin, in order to drive the ground pin(s) of the external device directly (with the appropriate external VDD pull-up device), without the need for external switches. Finally, the CHIME bit should be set to enable the PWC periodicity.

Once the RTCC and PWC are enabled and running, the PWC logic will generate a control output and a sample gate output. The control output is driven out on the RTCC pin (when RTCOE = 1 and OUTSEL<2:0> = 011) and is used to power-up or power-down the device, as described above.

Once the control output is asserted, the Stability Window begins, in which the external device is given enough time to power-up and provide a stable output.

Once the output is stable, the RTCC provides a sample gate during the Sample Window. The use of this sample gate depends on the external device being used, but typically, it is used to mask out one or more wake-up signals from the external device.

Finally, both the Stability and the Sample Windows close after the expiration of the Sample Window, and the external device is powered down.

24.3.1 POWER CONTROL CLOCK SOURCE

The Stability and Sample Windows are controlled by the PWCSAMP<7:0> and PWCSTAB<7:0> bits field in the RTCCON3L register (RTCCON3L<15:8> and <7:0>, respectively). As both the Stability and Sample Windows are defined in terms of the RTCC clock, their absolute values vary by the value of the PWC clock base period. The 8-bit magnitude of PWCSTABx and PWCSAMPx allows for a window size of 0 to 255 clock periods.

The period of the PWC clock can also be adjusted with a 1:1, 1:16, 1:64 or 1:256 prescaler, determined by the PWCPS<1:0> bits (RTCCON2L<7:6>).

In addition, certain values for the PWCSTABx and PWCSAMPx fields have specific control meanings in determining power control operations. If either bit field is 00h, the corresponding window is inactive. In addition, if the PWCSTABx field is FFh, the Stability Window remains active continuously, even if power control is disabled.

24.4 Event Timestamping

The RTCC includes two sets of Timestamp registers that may be used for the capture of Time and Date register values when an external input signal is received. The RTCC triggers the timestamps for two events:

- For Timestamp A, a falling edge on the $\overline{\text{TMPR}}$ pin
- For Timestamp B, when the devices transition from VDD to VBAT power

A Timestamp A event can be triggered while running the device in VBAT mode if the $\overline{\text{TMPR}}$ pin is pulled up to VBAT.

24.4.1 TIMESTAMP OPERATION

The event input is enabled for timestamping using the TSAEN bit (RTCCON1L<0>). When the timestamp event occurs, the present time and date values are stored in the TSATIMEL/H and TSADATEL/H registers, the TSAEVT status bit (RTCSTATL<3>) becomes set and an RTCC interrupt occurs. A new timestamp capture event cannot occur until the user clears the TSAEVT status bit.

Note 1: The TSATIMEL/H and TSADATEL/H register pairs can be used for data storage when TSAEN = 0. The values of TSATIMEL/H and TSADATEL/H will be maintained throughout all types of non-power Resets ($\overline{\text{MCLR}}$, WDT, etc).

24.4.2 MANUAL TIMESTAMP

The current time and date may be captured in the TSATIMEL/H and TSADATEL/H registers by writing a '1' to the TSAEVT bit location while the timestamp functionality is enabled (TSAEN = 1). This write will not set the TSAEVT bit, but it will initiate a timestamp capture. The TSAEVT bit will be set when the capture operation is complete. The user must poll the TSAEVT bit to determine when the capture operation is complete.

After the Timestamp registers have been read, the TSAEVT bit should be cleared to allow further hardware or software timestamp capture events.

REGISTER 25-5: CFGPAGE: SECURE ARRAY CONFIGURATION BITS (OTP PAGE 0) REGISTER (CONTINUED)

bit 21-20 **KEY1TYPE<1:0>:** Key Type for OTP Pages 1 and 2 bits
11 = Keys in these pages are for 192-bit/256-bit AES operations only
10 = Keys in these pages are for 128-bit AES operations only
01 = Keys in these pages are for 3DES operations only
00 = Keys in these pages are for DES/2DES operations only

bit 19 **SKEYEN:** Session Key Enable bit
1 = Stored Key #1 may be used only as a Key Encryption Key
0 = Stored Key #1 may be used for any operation

bit 18-11 **LKYSRC<7:0>:** Locked Key Source Configuration bits
If SRCLCK = 1:
1xxxxxxx = Key source is as if KEYSRC<3:0> = 1111
01xxxxxx = Key source is as if KEYSRC<3:0> = 0111
001xxxxx = Key source is as if KEYSRC<3:0> = 0110
0001xxxx = Key source is as if KEYSRC<3:0> = 0101
00001xxx = Key source is as if KEYSRC<3:0> = 0100
000001xx = Key source is as if KEYSRC<3:0> = 0011
0000001x = Key source is as if KEYSRC<3:0> = 0010
00000001 = Key source is as if KEYSRC<3:0> = 0001
00000000 = Key source is as if KEYSRC<3:0> = 0000
If SRCLCK = 0:
These bits are ignored.

bit 10 **SRCLCK:** Key Source Lock bit
1 = The key source is determined by the LKYSRC<7:0> bits (software key selection is disabled)
0 = The key source is determined by the KEYSRC<3:0> (CRYCONH<3:0>) bits (locked key selection is disabled)

bit 9-1 **WRLOCK<8:0>:** Write Lock Page Enable bits
For OTP Pages 0 (CFGPAGE) through 8:
1 = OTP Page is permanently locked and may not be programmed
0 = OTP Page is unlocked and may be programmed

bit 0 **SWKYDIS:** Software Key Disable bit
1 = Software key (CRYKEY register) is disabled; when KEYSRC<3:0> = 0000, the KEYFAIL status bit will be set and no encryption/decryption/session key operations can be started until KEYSRC<3:0> bits are changed to a value other than '0000'
0 = Software key (CRYKEY register) can be used as a key source when KEYSRC<3:0> = 0000

Note 1: This bit's state is mirrored by the PGMTST bit (CRYOTP<7>).

REGISTER 27-6: AD1CHS: A/D SAMPLE SELECT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB2	CH0NB1	CH0NB0	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA2	CH0NA1	CH0NA0	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **CH0NB<2:0>:** Sample B Channel 0 Negative Input Select bits
1xx = Unimplemented
011 = Unimplemented
010 = AN1
001 = Unimplemented
000 = VREF-/AVSS

bit 12-8 **CH0SB<4:0>:** Sample B Channel 0 Positive Input Select bits
See Table 27-2 for available options.

bit 7-5 **CH0NA<2:0>:** Sample A Channel 0 Negative Input Select bits
Same definitions as for CHONB<2:0>.

bit 4-0 **CH0SA<4:0>:** Sample A Channel 0 Positive Input Select bits
Same definitions as for CHOSB<4:0>.

TABLE 27-2: POSITIVE CHANNEL SELECT OPTIONS (CHOSA<4:0> OR CHOSB<4:0>)

CH0SA<4:0> or CH0SB<4:0>	Analog Channel	CH0SA<4:0> or CH0SB<4:0>	Analog Channel
11111	VBAT/2(1)	01111	AN15
11110	AVDD(1)	01110	AN14
11101	AVSS(1)	01101	AN13
11100	VBG(1)	01100	AN12
11011	Reserved	01011	AN11
11010	Reserved	01010	AN10
11001	CTMU	01001	AN9
11000	CTMU Temperature Sensor(2)	01000	AN8
10111	AN23(3)	00111	AN7
10110	AN22(3)	00110	AN6
10101	AN21(3)	00101	AN5
10100	AN20(3)	00100	AN4
10011	AN19(3)	00011	AN3
10010	AN18(3)	00010	AN2
10001	AN17(3)	00001	AN1
10000	AN16(3)	00000	AN0

Note 1: These input channels do not have corresponding memory-mapped result buffers.
2: Temperature sensor does not require AD1CTMENL<13> to be set.
3: These channels are not implemented in 64-pin devices.

35.0 INSTRUCTION SET SUMMARY

Note: This chapter is a brief summary of the PIC24F Instruction Set Architecture (ISA) and is not intended to be a comprehensive reference source.

The PIC24F instruction set adds many enhancements to the previous PIC® MCU instruction sets, while maintaining an easy migration from previous PIC MCU instruction sets. Most instructions are a single program memory word. Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction. The instruction set is highly orthogonal and is grouped into four basic categories:

- Word or byte-oriented operations
- Bit-oriented operations
- Literal operations
- Control operations

Table 35-1 shows the general symbols used in describing the instructions. The PIC24F instruction set summary in Table 35-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register, ‘Wb’, without any address modifier
- The second source operand, which is typically a register, ‘Ws’, with or without an address modifier
- The destination of the result, which is typically a register, ‘Wd’, with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value, ‘f’
- The destination, which could either be the file register, ‘f’, or the W0 register, which is denoted as ‘WREG’

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of ‘Ws’ or ‘f’)
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register, ‘Wb’)

The literal instructions that involve data movement may use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by the value of ‘k’)
- The W register or file register where the literal value is to be loaded (specified by ‘Wb’ or ‘f’)

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register, ‘Wb’, without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register, ‘Wd’, with or without an address modifier

The control instructions may use some of the following operands:

- A program memory address
- The mode of the Table Read and Table Write instructions

All instructions are a single word, except for certain double-word instructions, which were made double-word instructions so that all the required information is available in these 48 bits. In the second word, the 8 MSbs are ‘0’s. If this second word is executed as an instruction (by itself), it will execute as a NOP.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the Program Counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles, with the additional instruction cycle(s) executed as a NOP. Notable exceptions are the BRA (unconditional/computed branch), indirect CALL/GOTO, all Table Reads and Writes, and RETURN/RETFIE instructions, which are single-word instructions but take two or three cycles.

Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles. The double-word instructions execute in two instruction cycles.

TABLE 36-4: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Operating Temperature**	**VDD**	**Conditions**
Operating Current (IDD)(2)						
DC19	0.17	0.4	mA	-40°C to +85°C	2.0V	0.5 MIPS, FOSC = 1 MHz
	0.19	0.4	mA	-40°C to +85°C	3.3V	
DC20	0.28	0.7	mA	-40°C to +85°C	2.0V	1 MIPS, FOSC = 2 MHz
	0.31	0.7	mA	-40°C to +85°C	3.3V	
DC23	0.90	2.5	mA	-40°C to +85°C	2.0V	4 MIPS, FOSC = 8 MHz
	1.00	2.5	mA	-40°C to +85°C	3.3V	
DC24	5.13	9	mA	-40°C to +85°C	2.0V	16 MIPS, FOSC = 32 MHz
	5.28	9	mA	-40°C to +85°C	3.3V	
DC31	24.4	100	μA	-40°C to +85°C	2.0V	LPRC (15.5 KIPS), FOSC = 31 kHz
	24.5	110	μA	-40°C to +85°C	3.3V	

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Typical parameters are for design guidance only and are not tested.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. No peripheral modules are operating and all of the Peripheral Module Disable x (PMDx) bits are set.

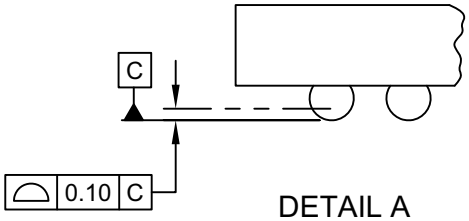
TABLE 36-5: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Operating Temperature**	**VDD**	**Conditions**
Idle Current (IIDLE)						
DC40	130	180	μA	-40°C to +85°C	2.0V	1 MIPS, FOSC = 2 MHz
	180	200	μA	-40°C to +85°C	3.3V	
DC43	0.33	0.7	mA	-40°C to +85°C	2.0V	4 MIPS, FOSC = 8 MHz
	0.44	0.8	mA	-40°C to +85°C	3.3V	
DC47	1.54	2.2	mA	-40°C to +85°C	2.0V	16 MIPS, FOSC = 32 MHz
	1.67	2.3	mA	-40°C to +85°C	3.3V	
DC50	0.56	0.8	mA	-40°C to +85°C	2.0V	4 MIPS (FRC), FOSC = 8 MHz
	0.56	0.9	mA	-40°C to +85°C	3.3V	
DC51	18.76	90	μA	-40°C to +85°C	2.0V	LPRC (15.5 KIPS), FOSC = 31 kHz
	19.30	100	μA	-40°C to +85°C	3.3V	

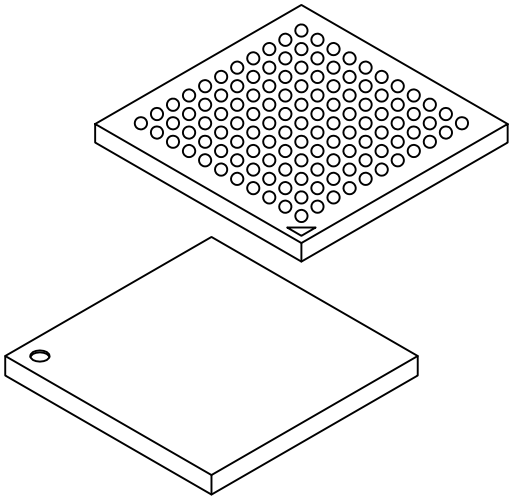
Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

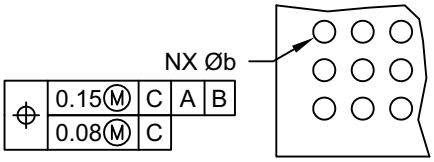
121-Ball Plastic Thin Profile Fine Pitch Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A





DETAIL B

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Contacts	N		121	
Contact Pitch	e		0.80 BSC	
Overall Height	A	1.00	1.10	1.20
Ball Height	A1	0.25	0.30	0.35
Overall Width	E		10.00 BSC	
Array Width	E1		8.00 BSC	
Overall Length	D		10.00 BSC	
Array Length	D1		8.00 BSC	
Contact Diameter	b	0.35	0.40	0.45

Notes:

1. Ball A1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
3. The outer rows and colums of balls are located with respect to datums A and B.
4. Ball interface to package body: 0.37mm nominal diameter.

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