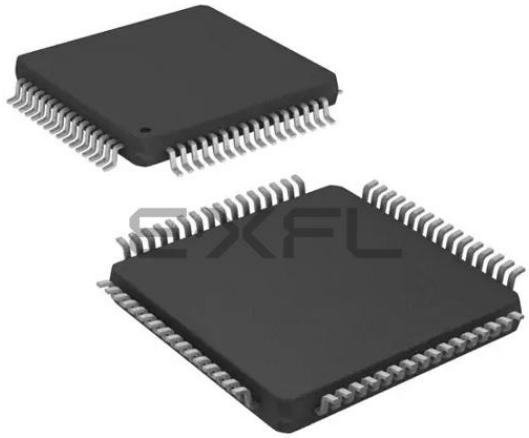

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128gb406t-i-pt

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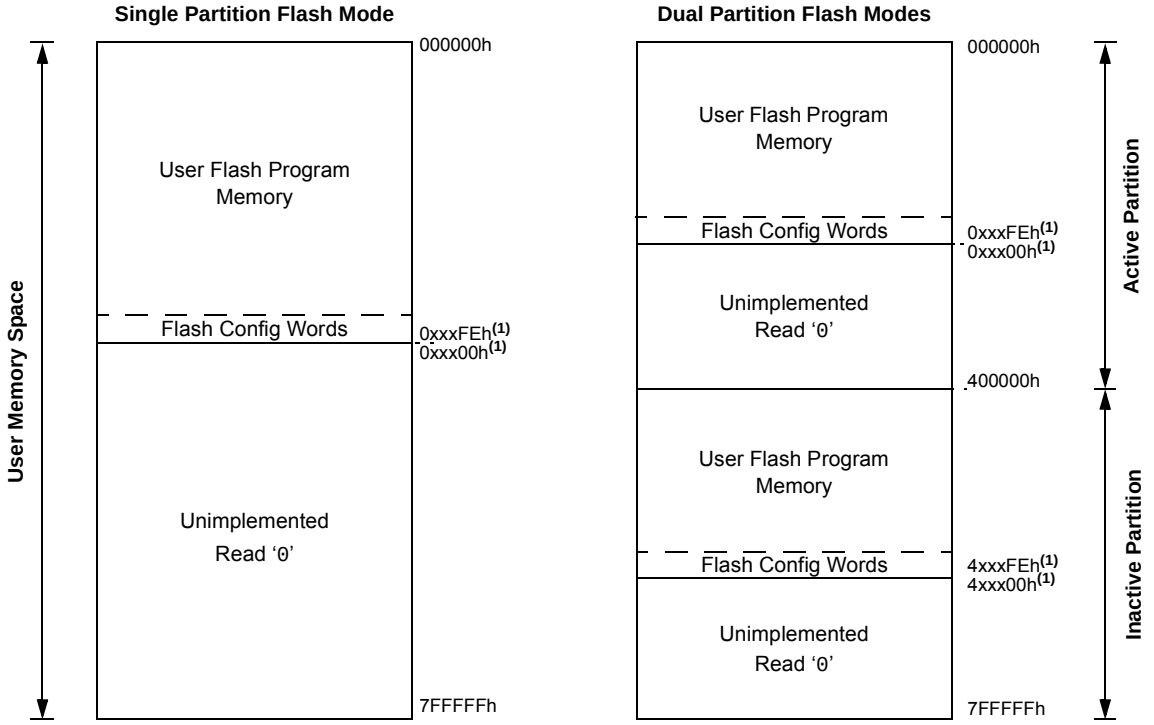
TABLE 1-2: DEVICE FEATURES FOR THE PIC24FJ256GA412/GB412 FAMILY: 100-PIN

Features	PIC24FJXXXGA/GB410					
	64GA	128GA	256GA	64GB	128GB	256GB
Operating Frequency	DC – 32 MHz					
Program Memory (bytes)	64K	128K	256K	64K	128K	256K
Program Memory (instructions)	22,016	44,032	88,064	22,016	44,032	88,064
Data Memory (bytes)	8K	16K		8K	16K	
Interrupt Sources (soft vectors/ NMI traps)	113 (107/6)					
I/O Ports	Ports A, B, C, D, E, F, G					
Total I/O Pins	85			84		
Remappable Pins	44 (32 I/Os, 12 input only)					
Timers:						
Total Number (16-bit)	19(1,2)					
32-Bit (from paired 16-bit timers)	9					
Input Capture w/Timer Channels	6(2)					
Output Compare/PWM Channels	6(2)					
Capture/Compare/PWM/Timer:						
Single Output (SCCP)	6(2)					
Multiple Output (MCCP)	1(2)					
Serial Communications:						
UART	6(2)					
SPI (3-wire/4-wire)	4(2)					
I^2C	3					
USB On-The-Go	No			Yes		
Cryptographic Engine	Yes					
Parallel Communications (EPMP/PSP)	Yes					
10/12-Bit Analog-to-Digital Converter (A/D) (input channels)	24					
Digital-to-Analog Converter (DAC)	1					
Analog Comparators	3					
CTMU Interface	Yes					
LCD Controller (available pixels)	512 (64 SEG x 8 COM)					
JTAG Boundary Scan	Yes					
Resets (and delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, $\overline{MCLR}$, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)					
Instruction Set	77 Base Instructions, Multiple Addressing Mode Variations					
Packages	100-Pin TQFP					

Note 1: Includes the Timer modes of the SCCP and MCCP modules.

2: Some instantiations of these modules are only available through remappable pins.

FIGURE 4-3: PROGRAM MEMORY MAPS FOR SINGLE AND DUAL PARTITION FLASH MODES



Legend: Memory areas are not shown to scale.
Note 1: Exact boundary addresses are determined by the size of the implemented program memory. See Table 4-1 for details.

TABLE 4-1: PROGRAM MEMORY SIZES AND BOUNDARIES

Device	Program Memory Upper Boundary (Instruction Words)			Write Blocks(1)	Erase Blocks(1)
	Single Partition Flash Mode	Dual Partition Flash Mode			
		Active Partition	Inactive Partition		
PIC24FJ256GX4XX	02AFFEh (88K)	0157FEh(44K)	0157FEh(44K)	1376	172
PIC24FJ128GX4XX	0157FEh(44K)	00ABFEh (22K)	00ABFEh (22K)	688	86
PIC24FJ64GX4XX	00AFFEh (22K)	0057FEh (11K)	0057FEh (11K)	352	44

Note 1: One Write Block = 64 Instruction Words; One Erase Block = 512 Instruction Words.

The Boot Sequence Configuration Words (FBTSEQ) determine whether Partition 1 or Partition 2 will be active after Reset. If the part is operating in Dual Partition mode, the partition with the lower boot sequence number will operate as the Active Panel (FBTSEQ is unused in Single Partition mode). The partitions can be switched between Active and Inactive by reprogramming their boot sequence numbers, but the Active Partition will not change until a device Reset is performed. If both boot sequence numbers are the same, or if both are corrupted, the part will use Partition 1 as the Active Partition. If only one boot sequence number is corrupted, the device will use the partition without a corrupted boot sequence number as the Active Partition.

The user can also change which partition is active at run time using the BOOTSWP instruction. Issuing a BOOTSWP instruction does not affect which partition will be the Active Partition after a Reset. Figure 4-4 demonstrates how the relationship between Partitions 1 and 2, shown in red and blue, respectively, and the Active and Inactive Partitions are affected by reprogramming the boot sequence number or issuing a BOOTSWP instruction.

The P2ACTIV bit (NVMCON<10>) can be used to determine which physical partition is the Active Partition. If P2ACTIV = 1, Partition 2 is active; if P2ACTIV = 0, Partition 1 is active.

4.4.2 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the program space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two, 16-bit word-wide address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space which contains the least significant data word, and TBLRDH and TBLWTH access the space which contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

1. TBLRDL (Table Read Low): In Word mode, it maps the lower word of the program space location (P<15:0>) to a data address (D<15:0>).

   In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when byte select is '1'; the lower byte is selected when it is '0'.

2. TBLRDH (Table Read High): In Word mode, it maps the entire upper word of a program address (P<23:16>) to a data address. Note that D<15:8>, the 'phantom' byte, will always be '0'.

   In Byte mode, it maps the upper or lower byte of the program word to D<7:0> of the data address, as above. Note that the data will always be '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address. The details of their operation are described in **Section 6.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Memory Page Address (TBLPAG) register. TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.

Note:	Only Table Read operations will execute in the configuration memory space where Device IDs are located. Table Write operations are not allowed.

FIGURE 4-11: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS

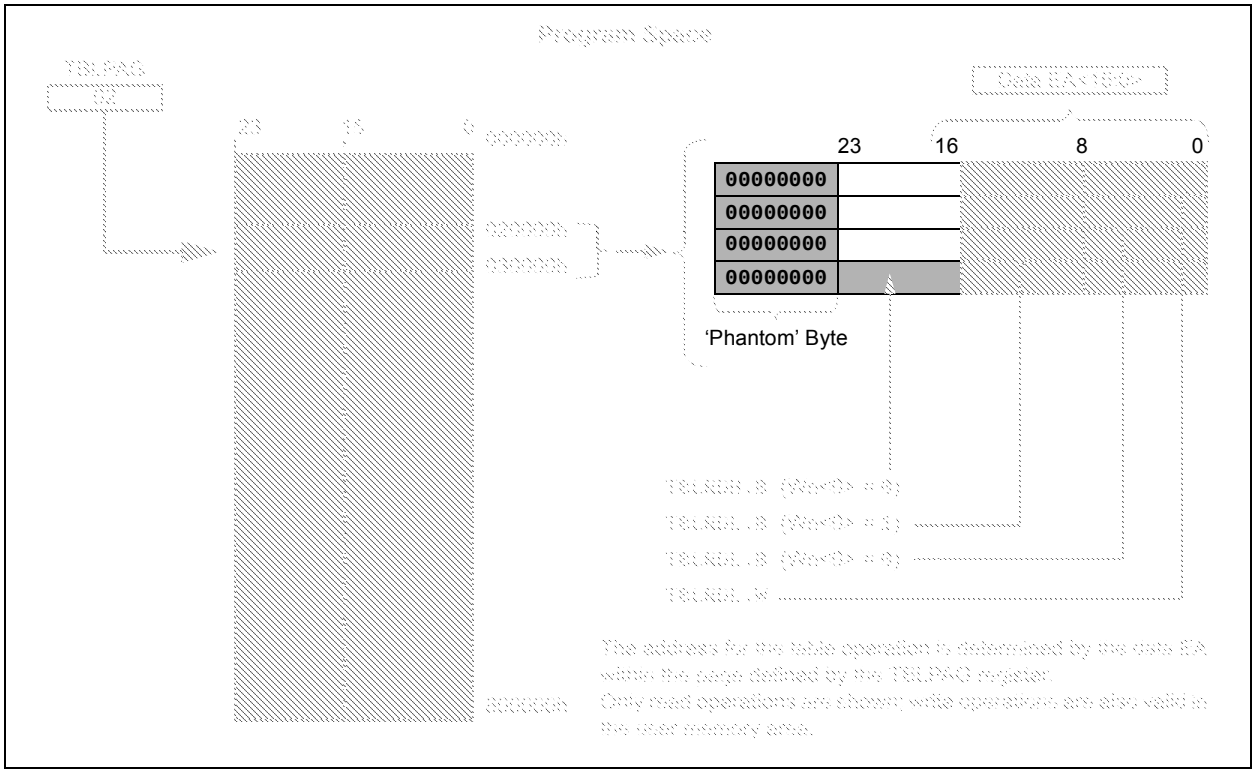


TABLE 5-1: DMA CHANNEL TRIGGER SOURCES

CHSEL<6:0>		Trigger (Interrupt)	CHSEL<6:0>		Trigger (Interrupt)	CHSEL<6:0>		Trigger (Interrupt)
0000000	00h	(Unimplemented)	0100110	26h	SPI1 Receive Event	1001100	4Ch	DMA Channel 4
0000001	01h	SCCP7 IC/OC Event	0100111	27h	SPI1 Transmit Event	1001101	4Dh	DMA Channel 3
0000010	02h	SCCP7 Timer	0101000	28h	SPI1 General Event	1001110	4Eh	DMA Channel 2
0000011	03h	SCCP6 IC/OC Event	0101001	29h	(Reserved, do not use)	1001111	4Fh	DMA Channel 1
0000100	04h	SCCP6 Timer	0101010	2Ah	(Reserved, do not use)	1010000	50h	DMA Channel 0
0000101	05h	SCCP5 IC/OC Event	0101011	2Bh	(Reserved, do not use)	1010001	51h	A/D Converter
0000110	06h	SCCP5 Timer	0101100	2Ch	I2C3 Slave Event	1010010	52h	USB
0000111	07h	SCCP4 IC/OC Event	0101101	2Dh	I2C3 Master Event	1010011	53h	EPMP
0001000	08h	SCCP4 Timer	0101110	2Eh	I2C3 Collision Event	1010100	54h	HLVD
0001001	09h	(Reserved, do not use)	0101111	2Fh	I2C2 Slave Event	1010101	55h	CRC Done
0001010	0Ah	(Reserved, do not use)	0110000	30h	I2C2 Master Event	1010110	56h	LCD
0001011	0Bh	SCCP3 IC/OC Event	0110001	31h	I2C2 Collision Event	1010111	57h	Crypto Done
0001100	0Ch	SCCP3 Timer	0110010	32h	I2C1 Slave Event	1011000	58h	Crypto OTP Done
0001101	0Dh	SCCP2 IC/OC Event	0110011	33h	I2C1 Master Event	1011001	59h	CLC4 Output
0001110	0Eh	SCCP2 Timer	0110100	34h	I2C1 Collision Event	1011010	5Ah	CLC3 Output
0001111	0Fh	MCCP1 IC/OC Event	0110101	35h	UART6 Transmit	1011011	5Bh	CLC2 Output
0010000	10h	MCCP1 Timer	0110110	36h	UART6 Receive	1011100	5Ch	CLC1 Output
0010001	11h	Output Compare 6	0110111	37h	UART6 Error	1011101	5Dh	(Reserved, do not use)
0010010	12h	Output Compare 5	0111000	38h	UART5 Transmit	1011110	5Eh	RTCC
0010011	13h	Output Compare 4	0111001	39h	UART5 Receive	1011111	5Fh	Timer5
0010100	14h	Output Compare 3	0111010	3Ah	UART5 Error	1100000	60h	Timer4
0010101	15h	Output Compare 2	0111011	3Bh	UART4 Transmit	1100001	61h	Timer3
0010110	16h	Output Compare 1	0111100	3Ch	UART4 Receive	1100010	62h	Timer2
0010111	17h	Input Capture 6	0111101	3Dh	UART4 Error	1100011	63h	Timer1
0011000	18h	Input Capture 5	0111110	3Eh	UART3 Transmit	1100100	64h	(Reserved, do not use)
0011001	19h	Input Capture 4	0111111	3Fh	UART3 Receive	1100101	65h	DAC
0011010	1Ah	Input Capture 3	1000000	40h	UART3 Error	1100110	66h	CTMU
0011011	1Bh	Input Capture 2	1000001	41h	UART2 Transmit	1100111	67h	Comparators Event
0011100	1Ch	Input Capture 1	1000010	42h	UART2 Receive	1101000	68h	External Interrupt 4
0011101	1Dh	SPI4 Receive Event	1000011	43h	UART2 Error	1101001	69h	External Interrupt 3
0011110	1Eh	SPI4 Transmit Event	1000100	44h	UART1 Transmit	1101010	6Ah	External Interrupt 2
0011111	1Fh	SPI4 General Event	1000101	45h	UART1 Receive	1101011	6Bh	External Interrupt 1
0100000	20h	SPI3 Receive Event	1000110	46h	UART1 Error	1101100	6Ch	External Interrupt 0
0100001	21h	SPI3 Transmit Event	1000111	47h	(Reserved, do not use)	1101101	6Dh	Interrupt-on-Change
0100010	22h	SPI3 General Event	1001000	48h	(Reserved, do not use)	1101110	6Eh	(Unimplemented)
0100011	23h	SPI2 Receive Event	1001001	49h	(Reserved, do not use)	•	•	
0100100	24h	SPI2 Transmit Event	1001010	4Ah	(Reserved, do not use)	•	•	
0100101	25h	SPI2 General Event	1001011	4Bh	DMA Channel 5	•	•	
						1111111	7Fh	

TABLE 7-3: RESET DELAY TIMES FOR VARIOUS DEVICE RESETS

Reset Type	Clock Source	$\overline{\text{SYSRST}}$ Delay	System Clock Delay	Notes
POR	EC	TPOR + TSTARTUP + TRST	—	**1, 2, 3**
	ECPLL	TPOR + TSTARTUP + TRST	TLOCK	**1, 2, 3, 5**
	XT, HS, SOSC	TPOR + TSTARTUP + TRST	TOST	**1, 2, 3, 4**
	XTPLL, HSPLL	TPOR + TSTARTUP + TRST	TOST + TLOCK	**1, 2, 3, 4, 5**
	FRC, FRCDIV	TPOR + TSTARTUP + TRST	TFRC	**1, 2, 3, 6, 7**
	FRCPLL	TPOR + TSTARTUP + TRST	TFRC + TLOCK	**1, 2, 3, 5, 6**
	LPRC	TPOR + TSTARTUP + TRST	TLPRC	**1, 2, 3, 6**
BOR	EC	TSTARTUP + TRST	—	**2, 3**
	ECPLL	TSTARTUP + TRST	TLOCK	**2, 3, 5**
	XT, HS, SOSC	TSTARTUP + TRST	TOST	**2, 3, 4**
	XTPLL, HSPLL	TSTARTUP + TRST	TOST + TLOCK	**2, 3, 4, 5**
	FRC, FRCDIV	TSTARTUP + TRST	TFRC	**2, 3, 6, 7**
	FRCPLL	TSTARTUP + TRST	TFRC + TLOCK	**2, 3, 5, 6**
	LPRC	TSTARTUP + TRST	TLPRC	**2, 3, 6**
$\overline{\text{MCLR}}$	Any Clock	TRST	—	**3**
WDT	Any Clock	TRST	—	**3**
Software	Any clock	TRST	—	**3**
Illegal Opcode	Any Clock	TRST	—	**3**
Uninitialized W	Any Clock	TRST	—	**3**
Trap Conflict	Any Clock	TRST	—	**3**

Note 1: TPOR = Power-on Reset Delay (10 μs nominal).

2: TSTARTUP = TVREG.

3: TRST = Internal State Reset Time (2 μs nominal).

4: TOST = Oscillator Start-up Timer (OST). A 10-bit counter counts 1024 oscillator periods before releasing the oscillator clock to the system.

5: TLOCK = PLL Lock Time.

6: TFRC and TLPRC = RC Oscillator Start-up Times.

7: If Two-Speed Start-up is enabled, regardless of the Primary Oscillator selected, the device starts with FRC so the system clock delay is just TFRC, and in such cases, FRC start-up time is valid; it switches to the Primary Oscillator after its respective clock delay.

7.4.1 POR AND LONG OSCILLATOR START-UP TIMES

The oscillator start-up circuitry and its associated delay timers are not linked to the device Reset delays that occur at power-up. Some crystal circuits (especially low-frequency crystals) will have a relatively long start-up time. Therefore, one or more of the following conditions is possible after $\overline{\text{SYSRST}}$ is released:

- The oscillator circuit has not begun to oscillate.
- The Oscillator Start-up Timer has not expired (if a crystal oscillator is used).
- The PLL has not achieved a lock (if PLL is used).

The device will not begin to execute code until a valid clock source has been released to the system. Therefore, the oscillator and PLL start-up delays must be considered when the Reset delay time must be known.

7.4.2 FAIL-SAFE CLOCK MONITOR (FSCM) AND DEVICE RESETS

If the FSCM is enabled, it will begin to monitor the system clock source when $\overline{\text{SYSRST}}$ is released. If a valid clock source is not available at this time, the device will automatically switch to the FRC Oscillator and the user can switch to the desired crystal oscillator in the Trap Service Routine (TSR).

TABLE 8-2: IMPLEMENTED INTERRUPT VECTORS

Interrupt Source	Vector Number	IRQ #	IVT Address	Interrupt Bit Locations		
				Flag	Enable	Priority
ADC1 Interrupt	21	13	00002Eh	IFS0<13>	IEC0<13>	IPC3<6:4>
CLC1	104	96	0000D4h	IFS6<0>	IEC6<0>	IPC24<2:0>
CLC2	105	97	0000D6h	IFS6<1>	IEC6<1>	IPC24<6:4>
CLC3	106	98	0000D8h	IFS6<2>	IEC6<2>	IPC24<10:8>
CLC4	107	99	0000DAh	IFS6<3>	IEC6<3>	IPC24<14:12>
Comparator Event	26	18	000038h	IFS1<2>	IEC1<2>	IPC4<10:8>
CRC Generator	75	67	00009Ah	IFS4<3>	IEC4<3>	IPC16<14:12>
Crypto Buffer Ready	42	34	000058h	IFS2<2>	IEC2<2>	IPC8<10:8>
Crypto Operation Done	63	55	000082h	IFS3<7>	IEC3<7>	IPC13<14:12>
Crypto Key Store Program Done	64	56	000084h	IFS3<8>	IEC3<8>	IPC14<2:0>
Crypto Rollover	43	35	00005Ah	IFS2<3>	IEC2<3>	IPC8<14:12>
CTMU Event	85	77	0000AEh	IFS4<13>	IEC4<13>	IPC19<6:4>
DAC	86	78	0000B0h	IFS4<14>	IEC4<14>	IPC19<10:8>
DMA Channel 0	12	4	00001Ch	IFS0<4>	IEC0<4>	IPC1<2:0>
DMA Channel 1	22	14	000030h	IFS0<14>	IEC0<14>	IPC3<10:8>
DMA Channel 2	32	24	000044h	IFS1<8>	IEC1<8>	IPC6<2:0>
DMA Channel 3	44	36	00005Ch	IFS2<4>	IEC2<4>	IPC9<2:0>
DMA Channel 4	54	46	000070h	IFS2<14>	IEC2<14>	IPC11<10:8>
DMA Channel 5	69	61	00008Eh	IFS3<13>	IEC3<13>	IPC15<6:4>
Enhanced Parallel Master Port (EPMP)	53	45	00006Eh	IFS2<13>	IEC2<13>	IPC11<6:4>
External Interrupt 0	8	0	000014h	IFS0<0>	IEC0<0>	IPC0<2:0>
External Interrupt 1	28	20	00003Ch	IFS1<4>	IEC1<4>	IPC5<2:0>
External Interrupt 2	37	29	00004Eh	IFS1<13>	IEC1<13>	IPC7<6:4>
External Interrupt 3	61	53	00007Eh	IFS3<5>	IEC3<5>	IPC13<6:4>
External Interrupt 4	62	54	000080h	IFS3<6>	IEC3<6>	IPC13<10:8>
Flash Write/Program Done	23	15	000032h	IFS0<15>	IEC0<15>	IPC3<14:12>
FRC Self-Tune	114	106	0000E8h	IFS6<10>	IEC6<10>	IPC26<10:8>
High/Low-Voltage Detect (HLVD)	80	72	0000A4h	IFS4<8>	IEC4<8>	IPC18<2:0>
I2C1 Bus Collision	92	84	0000BCh	IFS5<4>	IEC5<4>	IPC21<2:0>
I2C1 Master Event	25	17	000036h	IFS1<1>	IEC1<1>	IPC4<6:4>
I2C1 Slave Event	24	16	000034h	IFS1<0>	IEC1<0>	IPC4<2:0>
I2C2 Bus Collision	93	85	0000BEh	IFS5<5>	IEC5<5>	IPC21<6:4>
I2C2 Master Event	58	50	000078h	IFS3<2>	IEC3<2>	IPC12<10:8>
I2C2 Slave Event	57	49	000076h	IFS3<1>	IEC3<1>	IPC12<6:4>
I2C3 Master Event	79	71	0000A2h	IFS4<7>	IEC4<7>	IPC17<14:12>
I2C3 Slave Event	78	70	0000A0h	IFS4<6>	IEC4<6>	IPC17<10:8>
IC23 Collision	117	109	0000EEh	IFS6<13>	IEC6<13>	IPC27<6:4>
Input Capture 1	9	1	000016h	IFS0<1>	IEC0<1>	IPC0<6:4>
Input Capture 2	13	5	00001Eh	IFS0<5>	IEC0<5>	IPC1<6:4>
Input Capture 3	45	37	00005Eh	IFS2<5>	IEC2<5>	IPC9<6:4>
Input Capture 4	46	38	000060h	IFS2<6>	IEC2<6>	IPC9<10:8>
Input Capture 5	47	39	000062h	IFS2<7>	IEC2<7>	IPC9<14:12>
Input Capture 6	48	40	000064h	IFS2<8>	IEC2<8>	IPC10<2:0>
Interrupt-on-Change (IOC)	27	19	00003Ah	IFS1<3>	IEC1<3>	IPC4<14:12>
JTAG	125	117	0000FEh	IFS7<5>	IEC7<5>	IPC29<6:4>
LCD	108	100	0000DCh	IFS6<4>	IEC6<4>	IPC25<2:0>

REGISTER 8-4: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-0	R-0, HSC	R/W-0	U-0	U-0	U-0	U-0	R/W-0
GIE	DISI	SWTRAP	—	—	—	—	ALTIVT
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **GIE:** Global Interrupt Enable bit
1 = Interrupt and associated interrupt enable bits are enabled
0 = Interrupts are disabled; traps remain enabled

bit 14 **DISI:** DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active

bit 13 **SWTRAP:** Software Trap Status bit
1 = Generates a software trap
0 = Software trap is not requested

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **ALTIVT:** Enable Alternate Interrupt Vector Table bit
1 = Uses Alternate Interrupt Vector Table
0 = Uses standard (default) Interrupt Vector Table

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 3 **INT3EP:** External Interrupt 3 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

11.1.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a NOP.

11.1.2 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx and TRISx registers for data control, each port pin can also be individually configured for either a digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V) on any desired digital only pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

11.2 Configuring Analog Port Pins (ANSx)

The ANSx and TRISx registers control the operation of the pins with analog function. Each port pin with analog function is associated with one of the ANSx bits, which decides if the pin function should be analog or digital. Refer to Table 11-1 for detailed behavior of the pin for different ANSx and TRISx bit settings.

When reading the PORTx register, all pins configured as analog input channels will read as cleared (a low level).

11.2.1 ANALOG INPUT PINS AND VOLTAGE CONSIDERATIONS

The voltage tolerance of pins used as device inputs is dependent on the pin's input function. Most input pins are able to handle DC voltages of up to 5.5V, a level typical for digital logic circuits. However, several pins can only tolerate voltages up to VDD. Voltage excursions beyond VDD on these pins should always be avoided.

Information on voltage tolerance is provided in the pinout diagrams in the beginning of this data sheet. For more information, refer to **Section 36.0 "Electrical Characteristics"** for more details.

TABLE 11-1: CONFIGURING ANALOG/DIGITAL FUNCTION OF AN I/O PIN

Pin Function	ANSx Setting	TRISx Setting	Comments
Analog Input	1	1	It is recommended to keep ANSx = 1.
Analog Output	1	1	It is recommended to keep ANSx = 1.
Digital Input	0	1	Firmware must wait at least one instruction cycle after configuring a pin as a digital input before a valid input value can be read.
Digital Output	0	0	Make sure to disable the analog output function on the pin if any is present.

11.5 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. In an application that needs to use more than one peripheral multiplexed on a single pin, inconvenient work arounds in application code, or a complete redesign, may be the only option.

The Peripheral Pin Select (PPS) feature provides an alternative to these choices by enabling the user's peripheral set selection and its placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the microcontroller to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of any one of many digital peripherals to any one of these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.5.1 AVAILABLE PINS

The PPS feature is used with a range of up to 44 pins, depending on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the designation, "RPn" or "RPIn", in their full pin designation, where "n" is the remappable pin number. "RP" is used to designate pins that support both remappable input and output functions, while "RPI" indicates pins that support remappable input functions only.

PIC24FJ256GA412/GB412 family devices support a larger number of remappable input only pins than remappable input/output pins. In this device family, there are up to 32 remappable input/output pins, depending on the pin count of the particular device selected. These pins are numbered: RP0 through RP31. See Table 1-4 and Table 1-5 for a summary of pinout options in each package offering.

11.5.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer related peripherals (input capture and output compare) and external interrupt inputs. Also included are the outputs of the comparator module, since these are discrete digital signals.

PPS is not available for analog peripherals or these digital peripherals:

- I^2C (input and output)
- RTCC Alarm and Power Gate Outputs
- EPMP Signals (input and output)
- INT0

A key difference between pin select and non-pin select peripherals is that pin select peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-pin select peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

11.5.2.1 Peripheral Pin Select Function Priority

Pin-selectable peripheral outputs (e.g., output compare, UART transmit) will take priority over general purpose digital functions on a pin, such as EPMP and port I/O. Specialized digital outputs will take priority over PPS outputs on the same pin. The pin diagrams list peripheral outputs in the order of priority. Refer to them for priority concerns on a particular pin.

Unlike PIC24F devices with fixed peripherals, pin-selectable peripheral inputs will never take ownership of a pin. The pin's output buffer will be controlled by the TRISx setting or by a fixed peripheral on the pin. If the pin is configured in Digital mode, then the PPS input will operate correctly. If an analog function is enabled on the pin, the PPS input will be disabled.

11.5.3 CONTROLLING PERIPHERAL PIN SELECT

PPS features are controlled through two sets of Special Function Registers (SFRs): one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on if an input or an output is being mapped.

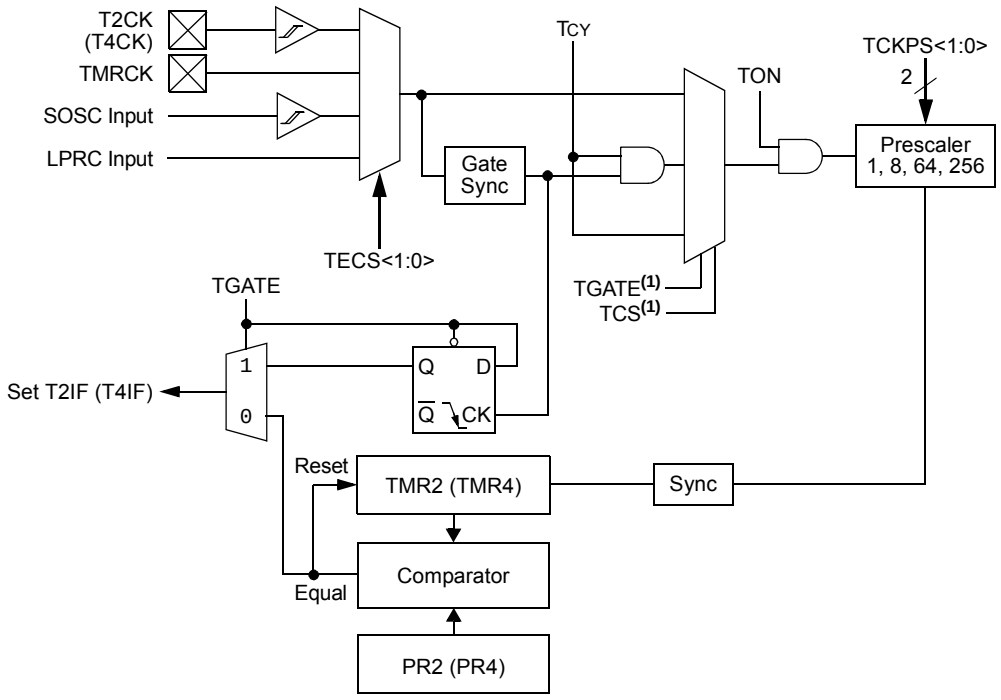
11.5.3.1 Input Mapping

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral; that is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers (Register 11-3 through Register 11-22) are used to configure peripheral input mapping. Each register contains two sets of 6-bit fields, with each set associated with one of the pin-selectable peripherals. Programming a given peripheral's bit field with an appropriate 6-bit value maps the RPn/RPIn pin with that value to that peripheral.

Table 11-11 summarizes the remappable inputs available with Peripheral Pin Select. For any given device, the valid range of values for any of the bit fields corresponds to the maximum number of Peripheral Pin Selections supported by the device.

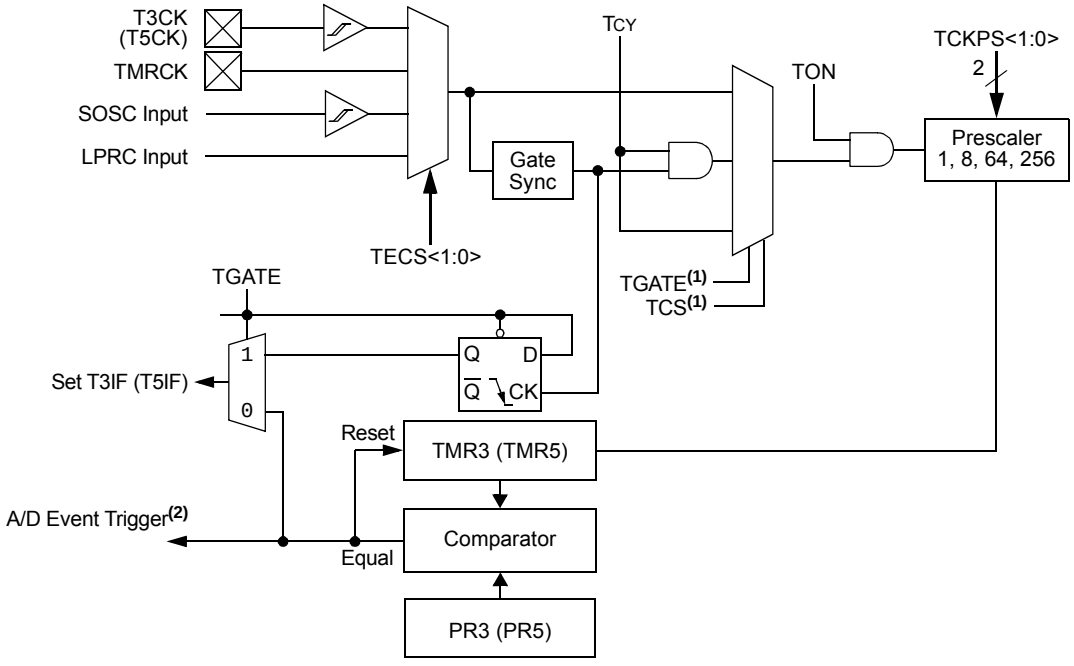
Note:	Unless otherwise noted, all remappable inputs utilize Schmitt Trigger buffers.

FIGURE 13-2: TIMER2 AND TIMER4 (16-BIT SYNCHRONOUS) BLOCK DIAGRAM



Note 1: The timer clock input must be assigned to an available RPn/RPIn pin before use. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

FIGURE 13-3: TIMER3 AND TIMER5 (16-BIT ASYNCHRONOUS) BLOCK DIAGRAM



Note 1: The timer clock input must be assigned to an available RPn/RPIn pin before use. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

2: The A/D Event Trigger is available only on Timer3.

NOTES:

REGISTER 25-3: CRYSTAT: CRYPTOGRAPHIC STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-x, HSC(1)	R-0, HSC(1)	R/C-0, HS(2)	R/C-0, HS(2)	U-0	R-0, HSC(1)	R-x, HSC(1)	R-x, HSC(1)
CRYBSY(4)	TXTABSY	CRYABRT(5)	ROLLOVR	—	MODFAIL(3)	KEYFAIL(3,4)	PGMFAIL(3,4)
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	HS = Hardware Settable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CRYBSY:** Cryptographic Engine Busy Status bit(1,4)
1 = A cryptographic operation is in progress
0 = No cryptographic operation is in progress

bit 6 **TXTABSY:** CRYTXTA Busy Status bit(1)
1 = The CRYTXTA register is busy and may not be written to
0 = The CRYTXTA is free and may be written to

bit 5 **CRYABRT:** Cryptographic Operation Aborted Status bit(2,5)
1 = Last operation was aborted by clearing the CRYGO bit in software
0 = Last operation completed normally (CRYGO cleared in hardware)

bit 4 **ROLLOVR:** Counter Rollover Status bit(2)
1 = The CRYTXTB counter rolled over on the last CTR mode operation; once set, this bit must be cleared by software before the CRYGO bit can be set again
0 = No rollover event has occurred

bit 3 **Unimplemented:** Read as '0'

bit 2 **MODFAIL:** Mode Configuration Fail Flag bit(1,3)
1 = Currently selected operating and Cipher mode configuration is invalid; the CRYWR bit cannot be set until a valid mode is selected (automatically cleared by hardware with any valid configuration)
0 = Currently selected operating and Cipher mode configurations are valid

bit 1 **KEYFAIL:** Key Configuration Fail Status bit(1,3,4)
See Table 25-1 and Table 25-2 for invalid key configurations.
1 = Currently selected key and mode configurations are invalid; the CRYWR bit cannot be set until a valid mode is selected (automatically cleared by hardware with any valid configuration)
0 = Currently selected configurations are valid

bit 0 **PGMFAIL:** Key Storage/Configuration Program Fail Flag bit(1,3,4)
1 = The page indicated by KEYPG<3:0> is reserved or locked; the CRYWR bit cannot be set and no programming operation can be started
0 = The page indicated by KEYPG<3:0> is available for programming

Note 1: These bits are reset on system Resets or whenever the CRYMD bit (PMD8<0>) is set.
2: These bits are reset on system Resets when the CRYMD bit is set or when CRYGO is cleared.
3: These bits are functional even when the module is disabled (CRYON = 0); this allows mode configurations to be validated for compatibility before enabling the module.
4: These bits are automatically set during all OTP read operations, including the initial read at POR. Once the read is completed, the bit assumes the proper state that reflects the current configuration.
5: If this bit is set, a cryptographic operation cannot be performed.

TABLE 25-2: AES KEY MODE/SOURCE SELECTION

Mode of Operation	KEYMOD<1:0>	KEYSRC<3:0>	Key Source		OTP Address
			SKEYEN = 0	SKEYEN = 1	
128-Bit AES	00	0000(1)	CRYKEY<127:0>		—
		0001	AES Key #1	Key Config Error(2)	<127:0>
		0010	AES Key #2		<255:128>
		0011	AES Key #3		<383:256>
		0100	AES Key #4		<511:384>
		1001	AES Key #5 (RAM)		<127:0>
		1010	AES Key #6 (RAM)		<255:128>
		1011	AES Key #7 (RAM)		<383:256>
		1100	AES Key #8 (RAM)		<511:384>
		1111	Reserved(2)		—
		All Others	Key Config Error(2)		—
192-Bit AES	01	0000(1)	CRYKEY<191:0>		—
		0001	AES Key #1	Key Config Error(2)	<191:0>
		0010	AES Key #2		<383:192>
		1001	AES Key #3 (RAM)		<191:0>
		1010	AES Key #4 (RAM)		<383:192>
		1111	Reserved(2)		—
		All Others	Key Config Error(2)		—
256-Bit AES	10	0000(1)	CRYKEY<255:0>		—
		0001	AES Key #1	Key Config Error(2)	<255:0>
		0010	AES Key #2		<511:256>
		1001	AES Key #3 (RAM)		<255:0>
		1010	AES Key #4 (RAM)		<511:256>
		1111	Reserved(2)		—
		All Others	Key Config Error(2)		—
(Reserved)	11	xxxx	Key Config Error(2)		—

Note 1: This configuration is considered a key configuration error (KEYFAIL bit is set) if SWKYDIS is also set.

2: The KEYFAIL bit (CRYSTAT<1>) is set when these configurations are selected and remains set until a valid configuration is selected.

26.0 32-BIT PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS30009729). The information in this data sheet supersedes the information in the FRM.

The 32-bit programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-Programmable CRC Polynomial Equation, up to 32 bits
- Programmable Shift Direction (little or big-endian)
- Independent Data and Polynomial Lengths
- Configurable Interrupt Output
- Data FIFO

Figure 26-1 displays a simplified block diagram of the CRC generator. A simple version of the CRC shift engine is displayed in Figure 26-2.

FIGURE 26-1: CRC MODULE BLOCK DIAGRAM

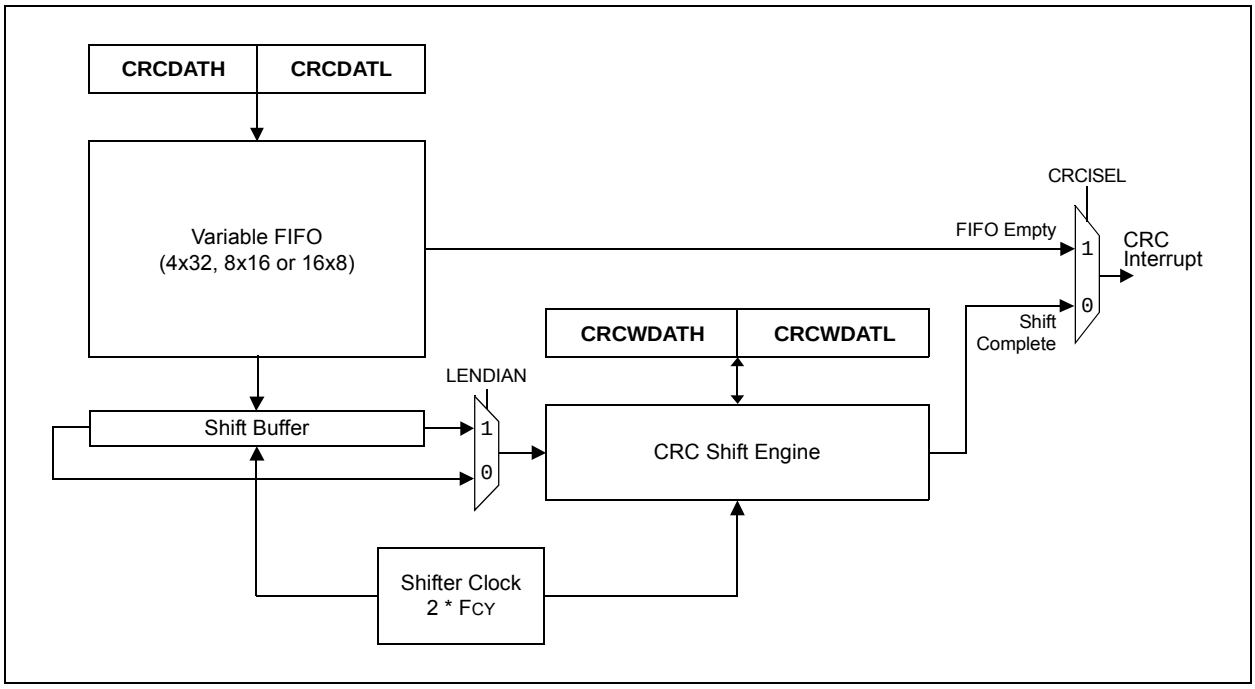
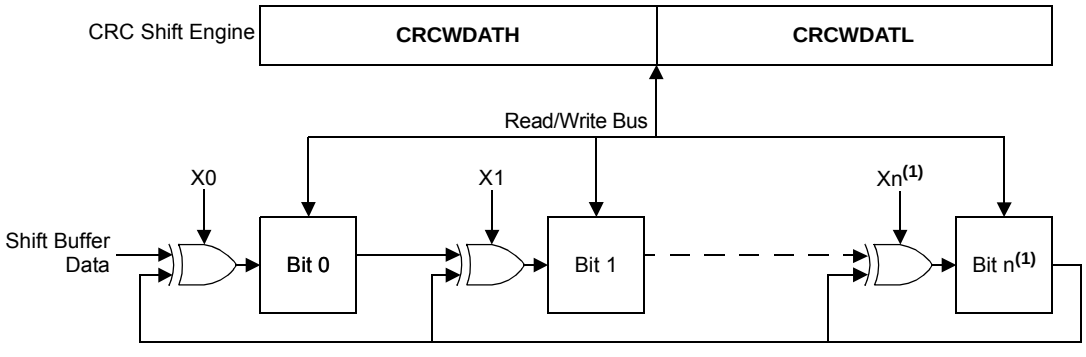


FIGURE 26-2: CRC SHIFT ENGINE DETAIL



Note 1: n = PLEN<4:1> + 1.

REGISTER 33-10: FDEVOPT1: DEVICE OPTIONS CONFIGURATION WORD

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 15							bit 8

U-1	U-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	U-1
—	—	—	ALTVREF(1)	TMPRWIPE	TMPRPIN	ALTCMPI(2)	—
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-5 **Unimplemented:** Read as '1'

bit 4 **ALTVREF:** Alternate External Voltage Reference Location Select bit(1)
1 = VREF+/CVREF+/DVREF+ and VREF-/CVREF- are mapped to RA10 and RA9, respectively
0 = VREF+/CVREF+/DVREF+ and VREF-/CVREF- are mapped to RB0 and RB1, respectively

bit 3 **TMPRWIPE:** Erase Key RAM on Tamper Event Enable Pin bit
1 = Cryptographic Engine Key RAM is not erased on $\overline{\text{TMPR}}$ pin events
0 = Cryptographic Engine Key RAM is erased when a $\overline{\text{TMPR}}$ pin event is detected

bit 2 **TMPRPIN:** Tamper Pin Disable bit
1 = $\overline{\text{TMPR}}$ pin is disabled
0 = $\overline{\text{TMPR}}$ pin is enabled

bit 1 **ALTCMPI:** Alternate Comparator Input Location Select bit(2)
1 = C1INC, C2INC and C3INC are mapped to their default pin locations
0 = C1INC, C2INC and C3INC are all mapped to RG9

bit 0 **Unimplemented:** Read as '1'

Note 1: Unimplemented on 64-pin devices; maintain this bit as '0' in those devices.
2: Unimplemented in PIC24FJXXXGAXXX devices.

TABLE 36-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
	VOL	**Output Low Voltage**					
DO10		I/O Ports	—	—	0.4	V	IOL = 6.6 mA, VDD = 3.6V
			—	—	0.4	V	IOL = 5.0 mA, VDD = 2V
DO16		OSCO/CLKO	—	—	0.4	V	IOL = 6.6 mA, VDD = 3.6V
			—	—	0.4	V	IOL = 5.0 mA, VDD = 2V
	VOH	**Output High Voltage**					
DO20		I/O Ports	3.0	—	—	V	IOH = -3.0 mA, VDD = 3.6V
			2.4	—	—	V	IOH = -6.0 mA, VDD = 3.6V
			1.65	—	—	V	IOH = -1.0 mA, VDD = 2V
			1.4	—	—	V	IOH = -3.0 mA, VDD = 2V
DO26		OSCO/CLKO	2.4	—	—	V	IOH = -6.0 mA, VDD = 3.6V
			1.4	—	—	V	IOH = -1.0 mA, VDD = 2V

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated.

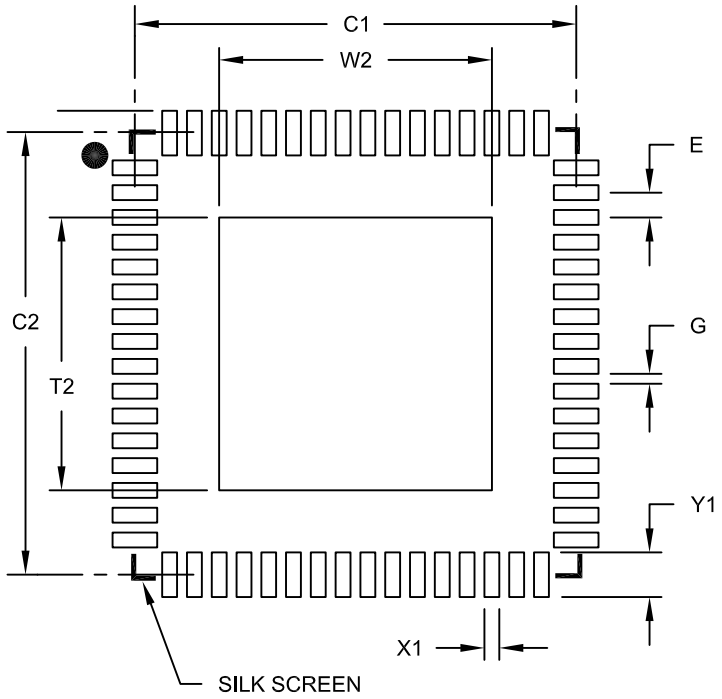
TABLE 36-10: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
		Program Flash Memory					
D130	EP	Cell Endurance	20000	—	—	E/W	-40°C to +85°C
D131	VPR	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D132B		VDD for Self-Timed Write	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D133A	TIW	Self-Timed Word Write Cycle Time	—	20	—	µs	
		Self-Timed Row Write Cycle Time	—	1.5	—	ms	
D133B	TIE	Self-Timed Page Erase Time	20	—	40	ms	
D134	TRETD	Characteristic Retention	20	—	—	Year	If no other specifications are violated
D135	IDDP	Supply Current During Programming	—	5	—	mA	

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length and 5.40x5.40mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			5.50
Optional Center Pad Length	T2			5.50
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

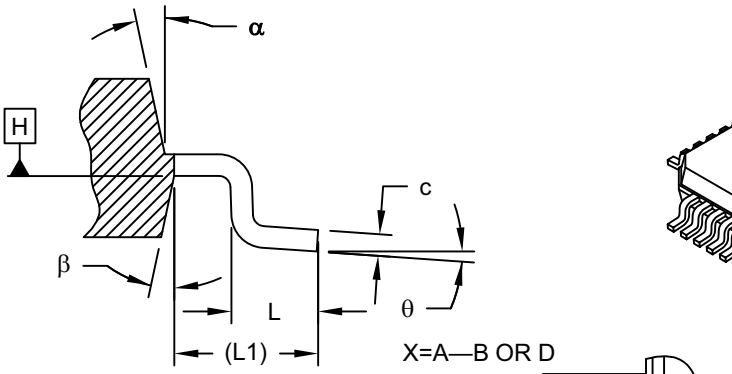
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

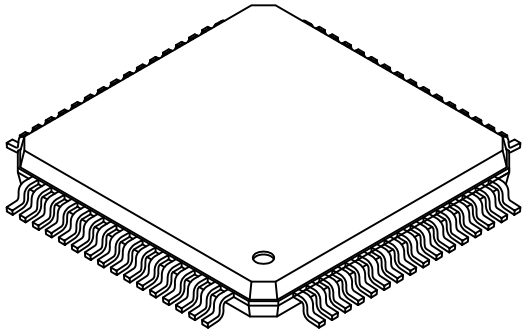
Microchip Technology Drawing No. C04-2154A

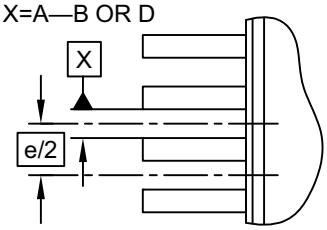
64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A





DETAIL 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		64	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

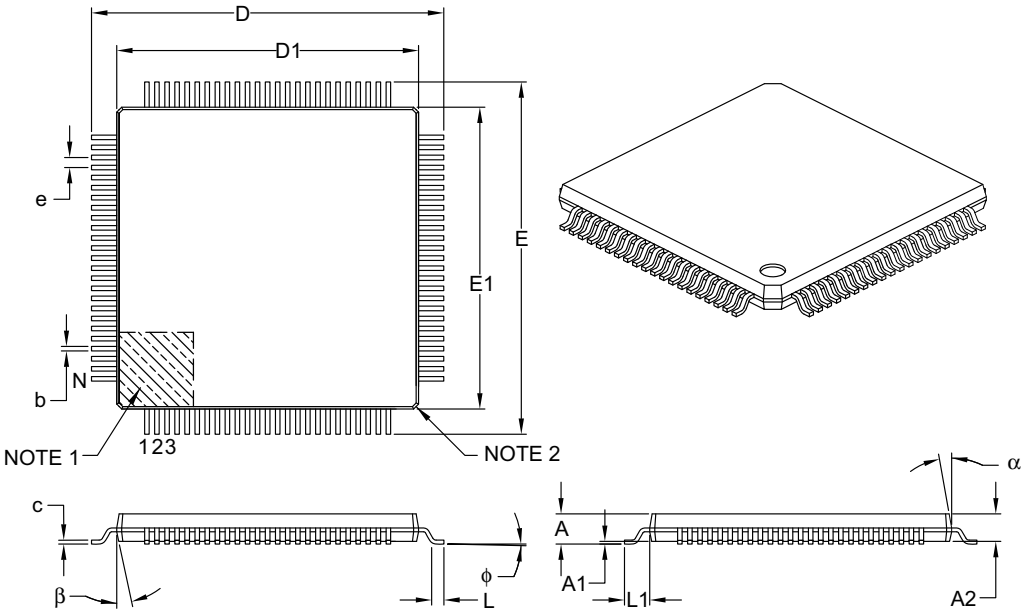
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085C Sheet 2 of 2

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		100	
Lead Pitch	e		0.40 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.13	0.18	0.23
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B