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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, PMP/PSP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128gb410t-i-pt

PIC24FJ256GA412/GB412 FAMILY

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- | | |
|-------------------|-------------------|
| • PIC24FJ64GA406 | • PIC24FJ64GB406 |
| • PIC24FJ128GA406 | • PIC24FJ128GB406 |
| • PIC24FJ256GA406 | • PIC24FJ256GB406 |
| • PIC24FJ64GA410 | • PIC24FJ64GB410 |
| • PIC24FJ128GA410 | • PIC24FJ128GB410 |
| • PIC24FJ256GA410 | • PIC24FJ256GB410 |
| • PIC24FJ64GA412 | • PIC24FJ64GB412 |
| • PIC24FJ128GA412 | • PIC24FJ128GB412 |
| • PIC24FJ256GA412 | • PIC24FJ256GB412 |

The PIC24FJ256GA412/GB412 family expands the capabilities of the PIC24F family by adding a complete selection of advanced analog peripherals to its existing digital features. This combination, along with its ultra low-power features, Direct Memory Access (DMA) for peripherals, USB On-The-Go (OTG) and a built-in LCD Controller and driver, makes this family the new standard for mixed-signal PIC® microcontrollers in one economical and power-saving package.

1.1 Core Features

1.1.1 16-BIT ARCHITECTURE

Central to all PIC24F devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC® Digital Signal Controllers (DSCs). The PIC24F CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths with the ability to move information between data and memory spaces
- Linear addressing of up to 12 Mbytes (program space) and 32 Kbytes (data)
- A 16-element Working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32 by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages, such as 'C'
- Operational performance up to 16 MIPS

1.1.2 XLP POWER-SAVING TECHNOLOGY

The PIC24FJ256GA412/GB412 family of devices incorporates a greatly expanded range of power-saving operating modes for the ultimate in power conservation. The new modes include:

- Retention Sleep, with essential circuits being powered from a separate low-voltage regulator
- Deep Sleep without RTCC, for the lowest possible power consumption under software control
- VBAT mode (with or without RTCC), to continue limited operation from a backup battery when VDD is removed

Many of these new low-power modes also support the continuous operation of the low-power, on-chip Real-Time Clock/Calendar (RTCC), making it possible for an application to keep time while the device is otherwise asleep.

Aside from these new features, the PIC24FJ256GA412/GB412 devices also include all of the legacy power-saving features of previous PIC24F microcontrollers, such as:

- On-the-Fly Clock Switching, allowing the selection of a lower power clock during run time
- Doze Mode Operation, for maintaining peripheral clock speed while slowing the CPU clock
- Instruction-Based Power-Saving Modes, for quick invocation of Idle and the many Sleep modes

1.1.3 DUAL PARTITION FLASH PROGRAM MEMORY

A brand new feature to the PIC24F family is the use of Dual Partition Flash program memory technology. This allows PIC24FJ256GA412/GB412 family devices a range of new operating options not available before:

- Dual Partition Operation, which can store two different applications in their own code partition, and allows for the support of robust bootloader applications and enhanced security
- Live Update Operation, which allows the main application to continue operation while the second Flash partition is being reprogrammed – all without adding Wait states to code execution
- Direct Run-Time Programming from Data RAM, with the option of data compression in the RAM image

PIC24FJ256GA412/GB412 family devices can also operate with their two Flash partitions as one large program memory, providing space for large and complex applications.

PIC24FJ256GA412/GB412 FAMILY

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
AN0	16	25	K2	I	ANA	A/D Analog Inputs
AN1	15	24	K1	I	ANA	
AN1-	15	24	K1	I	ANA	
AN2	14	23	J2	I	ANA	
AN3	13	22	J1	I	ANA	
AN4	12	21	H2	I	ANA	
AN5	11	20	H1	I	ANA	
AN6	17	26	L1	I	ANA	
AN7	18	27	J3	I	ANA	
AN8	21	32	K4	I	ANA	
AN9	22	33	L4	I	ANA	
AN10	23	34	H5	I	ANA	
AN11	24	35	K5	I	ANA	
AN12	27	41	J7	I	ANA	
AN13	28	42	L7	I	ANA	
AN14	29	43	K7	I	ANA	
AN15	30	44	L8	I	ANA	
AN16	—	9	E1	I	ANA	
AN17	—	10	E3	I	ANA	
AN18	—	11	F4	I	ANA	
AN19	—	12	F2	I	ANA	
AN20	—	14	F3	I	ANA	
AN21	—	19	G2	I	ANA	
AN22	—	92	E11	I	ANA	
AN23	—	91	E10	I	ANA	
AVDD	19	30	J4	P	—	Positive Supply for Analog modules
AVss	20	31	L3	P	—	Ground Reference for Analog modules
C1INA	11	20	H1	I	ANA	Comparator 1 Input A
C1INB	12	21	H2	I	ANA	Comparator 1 Input B
C1INC	5,8	11,14	F4,F3	I	ANA	Comparator 1 Input C
C1IND	4	10	E3	I	ANA	Comparator 1 Input D
C2INA	13	22	J1	I	ANA	Comparator 2 Input A
C2INB	14	23	J2	I	ANA	Comparator 2 Input B
C2INC	8	14	F3	I	ANA	Comparator 2 Input C
C2IND	6	12	F2	I	ANA	Comparator 2 Input D
C3INA	55	84	C7	I	ANA	Comparator 3 Input A
C3INB	54	83	D7	I	ANA	Comparator 3 Input B
C3INC	8,45	14,71	F3,C11	I	ANA	Comparator 3 Input C
C3IND	44	70	D11	I	ANA	Comparator 3 Input D
CLC3OUT	46	72	D9	O	DIG	CLC3 Output
CLC4OUT	42	68	E9	O	DIG	CLC4 Output

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus

ST = Schmitt Trigger input buffer
I²C = I²C/SMBus input buffer
XCVR = Dedicated transceiver

PIC24FJ256GA412/GB412 FAMILY

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
RB0	16	25	K2	I/O	DIG/ST	PORTB Digital I/Os
RB1	15	24	K1	I/O	DIG/ST	
RB2	14	23	J2	I/O	DIG/ST/TTL	
RB3	13	22	J1	I/O	DIG/ST/TTL	
RB4	12	21	H2	I/O	DIG/ST/TTL	
RB5	11	20	H1	I/O	DIG/ST/TTL	
RB6	17	26	L1	I/O	DIG/ST	
RB7	18	27	J3	I/O	DIG/ST/TTL	
RB8	21	32	K4	I/O	DIG/ST	
RB9	22	33	L4	I/O	DIG/ST	
RB10	23	34	H5	I/O	DIG/ST	
RB11	24	35	K5	I/O	DIG/ST	
RB12	27	41	J7	I/O	DIG/ST	
RB13	28	42	L7	I/O	DIG/ST	
RB14	29	43	K7	I/O	DIG/ST	
RB15	30	44	L8	I/O	DIG/ST	
RC1	—	6	D1	I/O	DIG/ST	PORTC Digital I/Os
RC2	—	7	E4	I/O	DIG/ST	
RC3	—	8	E2	I/O	DIG/ST	
RC4	—	9	E1	I/O	DIG/ST	
RC12	39	63	F9	I/O	DIG/ST	
RC13	47	73	C10	I	ST	
RC14	48	74	B11	I	ST	
RC15	40	64	F11	I/O	DIG/ST	
RD0	46	72	D9	I/O	DIG/ST	PORTD Digital I/Os
RD1	49	76	A11	I/O	DIG/ST	
RD2	50	77	A10	I/O	DIG/ST	
RD3	51	78	B9	I/O	DIG/ST	
RD4	52	81	C8	I/O	DIG/ST	
RD5	53	82	B8	I/O	DIG/ST	
RD6	54	83	D7	I/O	DIG/ST	
RD7	55	84	C7	I/O	DIG/ST	
RD8	42	68	E9	I/O	DIG/ST	
RD9	43	69	E10	I/O	DIG/ST	
RD10	44	70	D11	I/O	DIG/ST	
RD11	45	71	C11	I/O	DIG/ST	
RD12	—	79	A9	I/O	DIG/ST	
RD13	—	80	D8	I/O	DIG/ST	
RD14	—	47	L9	I/O	DIG/ST	
RD15	—	48	K9	I/O	DIG/ST	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus

ST = Schmitt Trigger input buffer
I²C = I²C/SMBus input buffer
XCVR = Dedicated transceiver

PIC24FJ256GA412/GB412 FAMILY

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT MICROCONTROLLERS

2.1 Basic Connection Requirements

Getting started with the PIC24FJ256GA412/GB412 family of 16-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All VDD and VSS pins (see **Section 2.2 “Power Supply Pins”**)
- All analog power pins (AVDD and AVSS), regardless of whether or not the analog device features are used (see **Section 2.2 “Power Supply Pins”**)
- The USB transceiver supply, VUSB3V3, regardless of whether or not the USB module is used (see **Section 2.2 “Power Supply Pins”**)
- MCLR pin (see **Section 2.3 “Master Clear (MCLR) Pin”**)
- VCAP pin (see **Section 2.4 “Voltage Regulator Pin (VCAP)”**)

These pins must also be connected if they are being used in the end application:

- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 “ICSP Pins”**)
- OSCI and OSCO pins when an external oscillator source is used (see **Section 2.6 “External Oscillator Pins”**)

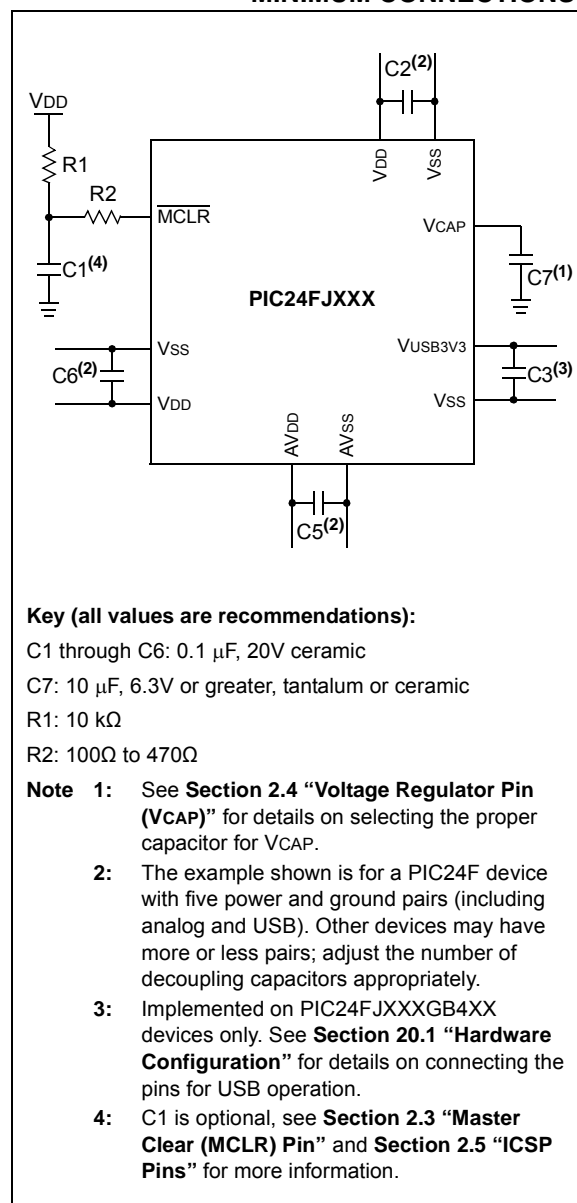
Additionally, the following pins may be required:

- Any voltage reference pins used when external voltage reference for analog modules is implemented (AVREF+/AVREF-, CVREF+/CVREF- and DVREF+)

Note: All analog power supply and return pins must always be connected, regardless of whether any of the analog modules are being used.

The minimum mandatory connections are shown in Figure 2-1.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTIONS



PIC24FJ256GA412/GB412 FAMILY

4.4.2 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the program space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two, 16-bit word-wide address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space which contains the least significant data word, and TBLRDH and TBLWTH access the space which contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

1. TBLRDL (Table Read Low): In Word mode, it maps the lower word of the program space location ($P<15:0>$) to a data address ($D<15:0>$). In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when byte select is '1'; the lower byte is selected when it is '0'.

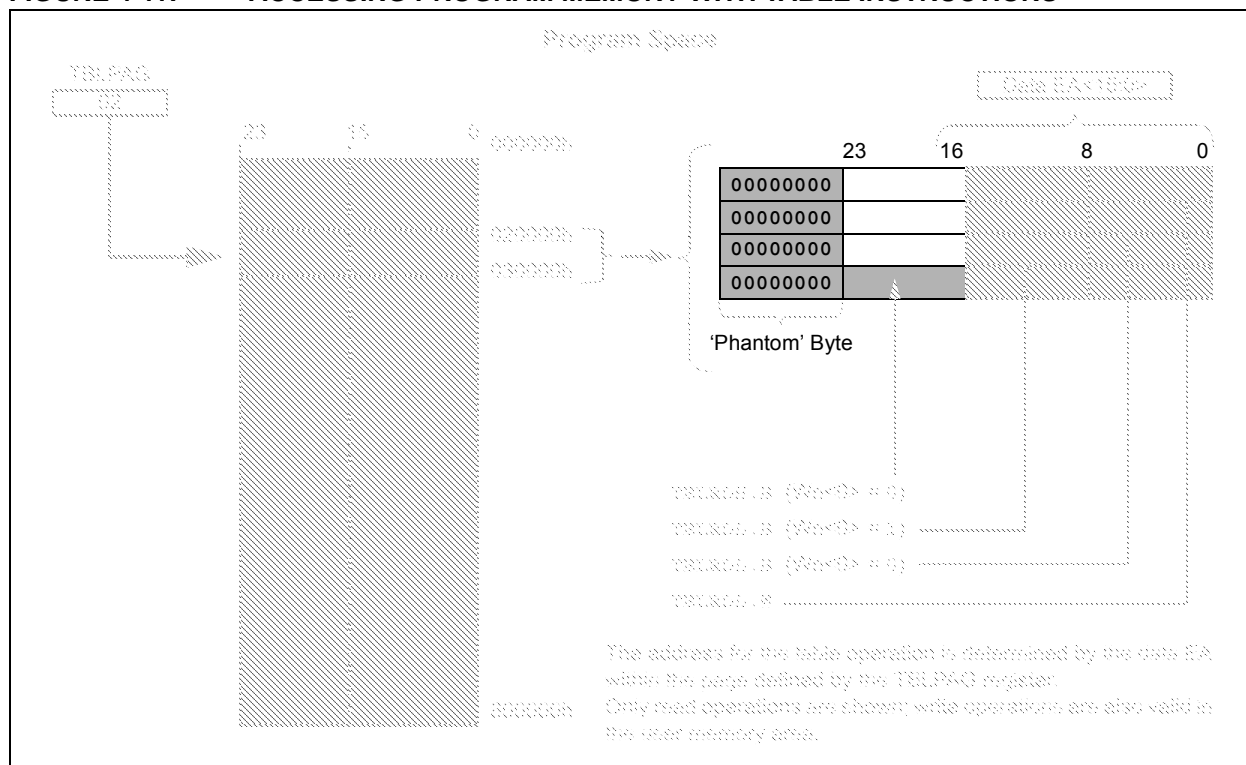
2. TBLRDH (Table Read High): In Word mode, it maps the entire upper word of a program address ($P<23:16>$) to a data address. Note that $D<15:8>$, the 'phantom' byte, will always be '0'. In Byte mode, it maps the upper or lower byte of the program word to $D<7:0>$ of the data address, as above. Note that the data will always be '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address. The details of their operation are described in **Section 6.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Memory Page Address (TBLPAG) register. TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When $TBLPAG<7> = 0$, the table page is located in the user memory space. When $TBLPAG<7> = 1$, the page is located in configuration space.

Note: Only Table Read operations will execute in the configuration memory space where Device IDs are located. Table Write operations are not allowed.

FIGURE 4-11: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



PIC24FJ256GA412/GB412 FAMILY

REGISTER 8-43: IPC21: INTERRUPT PRIORITY CONTROL REGISTER 21

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U4ERIP2	U4ERIP1	U4ERIP0	—	USB1IP2	USB1IP1	USB1IP0
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	I2C2BCIP2	I2C2BCIP1	I2C2BCIP0	—	I2C1BCIP2	I2C1BCIP1	I2C1BCIP0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **U4ERIP<2:0>:** UART4 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **USB1IP<2:0>:** USB1 (USB OTG) Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **I2C2BCIP<2:0>:** I2C2 Bus Collision Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **I2C1BCIP<2:0>:** I2C1 Bus Collision Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1
000 = Interrupt source is disabled

PIC24FJ256GA412/GB412 FAMILY

9.0 OSCILLATOR CONFIGURATION

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the “dsPIC33/PIC24 Family Reference Manual”, “Oscillator” (DS39700). The information in this data sheet supersedes the information in the FRM.

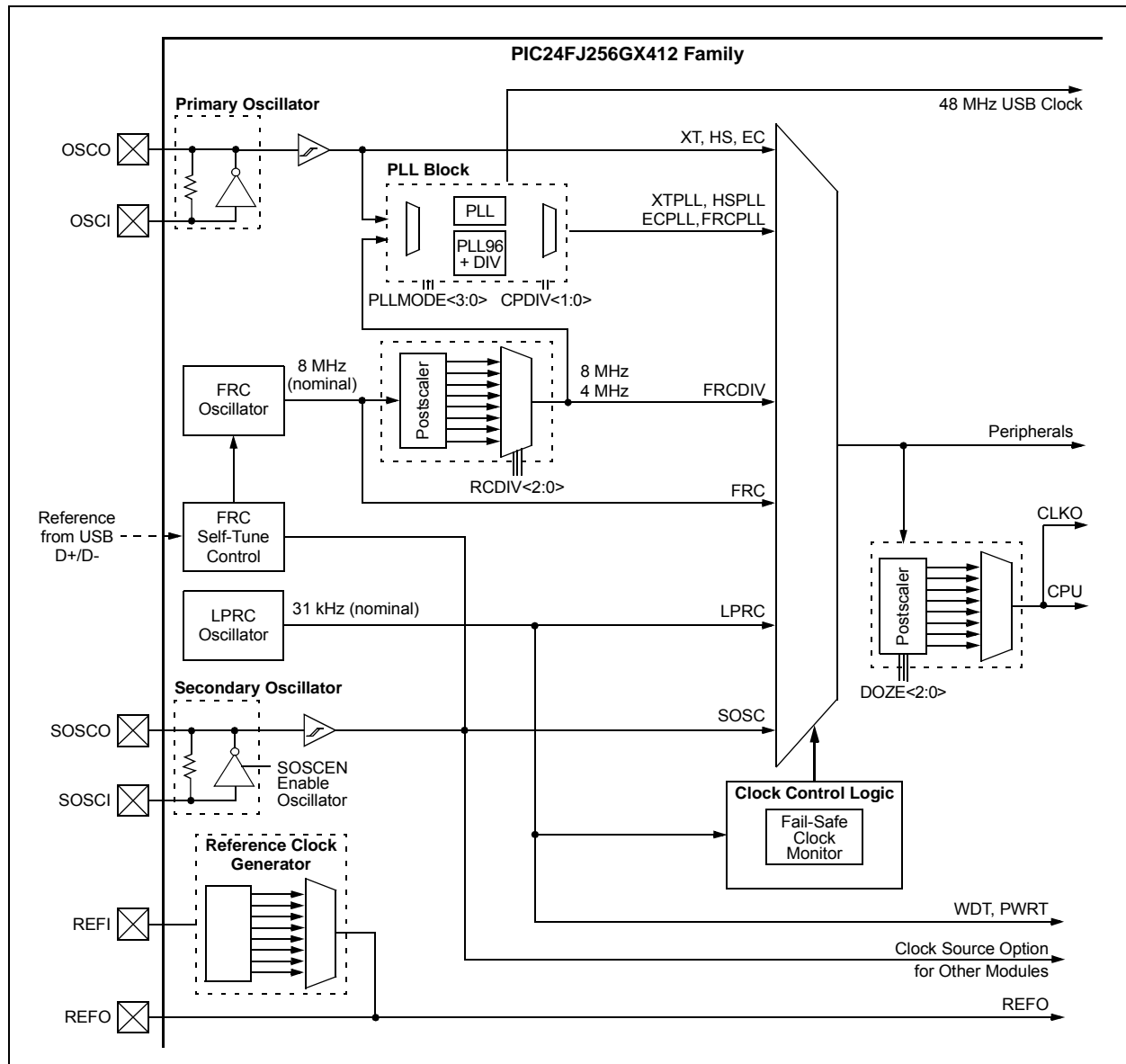
The oscillator system for PIC24FJ256GA412/GB412 family devices has the following features:

- A Total of Four External and Internal Oscillator Options as Clock Sources, providing 11 Different Clock Modes

- An On-Chip PLL Block to provide a Wide Range of Precise Frequency Options for the System Clock, plus a Stable 48 MHz Clock for USB Devices
- Software-Controllable Switching between Various Clock Sources
- Software-Controllable Postscaler for Selective Clocking of CPU for System Power Savings
- A Fail-Safe Clock Monitor (FSCM) that Detects Clock Failure and Permits Safe Application Recovery or Shutdown
- A Separate and Independently Configurable Reference Clock for Synchronizing External Hardware

A simplified diagram of the oscillator system is shown in Figure 9-1.

FIGURE 9-1: PIC24FJ256GA412/GB412 FAMILY GENERAL CLOCK DIAGRAM



PIC24FJ256GA412/GB412 FAMILY

REGISTER 11-7: RPINR4: PERIPHERAL PIN SELECT INPUT REGISTER 4

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	T5CKR5	T5CKR4	T5CKR3	T5CKR2	T5CKR1	T5CKR0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	T4CKR5	T4CKR4	T4CKR3	T4CKR2	T4CKR1	T4CKR0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **T5CKR<5:0>:** Assign Timer5 Clock Input (T5CK) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **T4CKR<5:0>:** Assign Timer4 Clock Input (T4CK) to Corresponding RPn or RPIn Pin bits

REGISTER 11-8: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	IC2R5	IC2R4	IC2R3	IC2R2	IC2R1	IC2R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	IC1R5	IC1R4	IC1R3	IC1R2	IC1R1	IC1R0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **IC2R<5:0>:** Assign Input Capture 2 (IC2) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IC1R<5:0>:** Assign Input Capture 1 (IC1) to Corresponding RPn or RPIn Pin bits

PIC24FJ256GA412/GB412 FAMILY

REGISTER 11-31: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP17R5	RP17R4	RP17R3	RP17R2	RP17R1	RP17R0
bit 15						bit 8	

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP16R5	RP16R4	RP16R3	RP16R2	RP16R1	RP16R0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP17R<5:0>:** RP17 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP17 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP16R<5:0>:** RP16 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP16 (see Table 11-12 for peripheral function numbers).

REGISTER 11-32: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP19R5	RP19R4	RP19R3	RP19R2	RP19R1	RP19R0
bit 15						bit 8	

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP18R5	RP18R4	RP18R3	RP18R2	RP18R1	RP18R0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP19R<5:0>:** RP19 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP19 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP18R<5:0>:** RP18 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP18 (see Table 11-12 for peripheral function numbers).

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NOTES:

PIC24FJ256GA412/GB412 FAMILY

13.0 TIMER2/3 AND TIMER4/5

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the “dsPIC33/PIC24 Family Reference Manual”, “Timers” (DS39704). The information in this data sheet supersedes the information in the FRM.

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent, 16-bit timers with selectable operating modes.

As 32-bit timers, Timer2/3 and Timer4/5 can each operate in three modes:

- Two Independent 16-Bit Timers with all 16-Bit Operating Modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep Modes
- Interrupt on a 32-Bit Period Register Match
- A/D Event Trigger (only on Timer2/3 in 32-bit mode and Timer3 in 16-bit mode)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed above, except for the A/D Event Trigger. This trigger is implemented only on Timer2/3 in 32-bit mode and Timer3 in 16-bit mode. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON and T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1; T3CON and T5CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word; Timer3 and Timer5 are the most significant word of the 32-bit timers.

Note: For 32-bit operation, T3CON and T5CON control bits are ignored. Only T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 or Timer5 interrupt flags.

To configure Timer2/3 or Timer4/5 for 32-bit operation:

1. Set the T32 or T45 bit (T2CON<3> or T4CON<3> = 1).
2. Select the prescaler ratio for Timer2 or Timer4 using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the TCS and TGATE bits. If TCS is set to an external clock, RPINRx (TxCK) must be configured to an available RPn/RPIn pin. For more information, see **Section 11.5 “Peripheral Pin Select (PPS)”**.
4. Load the timer period value. PR3 (or PR5) will contain the most significant word (msw) of the value, while PR2 (or PR4) contains the least significant word (lsw).
5. If interrupts are required, set the interrupt enable bit, T3IE or T5IE. Use the priority bits, T3IP<2:0> or T5IP<2:0>, to set the interrupt priority. Note that while Timer2 or Timer4 controls the timer, the interrupt appears as a Timer3 or Timer5 interrupt.
6. Set the TON bit (= 1).

The timer value, at any point, is stored in the register pair, TMR<3:2> (or TMR<5:4>). TMR3 (TMR5) always contains the most significant word of the count, while TMR2 (TMR4) contains the least significant word.

To configure any of the timers for individual 16-bit operation:

1. Clear the T32 bit corresponding to that timer (T2CON<3> for Timer2 and Timer3 or T4CON<3> for Timer4 and Timer5).
2. Select the timer prescaler ratio using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the TCS and TGATE bits. See **Section 11.5 “Peripheral Pin Select (PPS)”** for more information.
4. Load the timer period value into the PRx register.
5. If interrupts are required, set the interrupt enable bit, TxIE. Use the priority bits, TxIP<2:0>, to set the interrupt priority.
6. Set the TON (TxCON<15> = 1) bit.

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REGISTER 13-2: TyCON: TIMER3 AND TIMER5 CONTROL REGISTER⁽¹⁾

R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
TON ⁽²⁾	—	TSIDL ⁽²⁾	—	—	—	TECS1 ^(2,3)	TECS0 ^(2,3)
bit 15						bit 8	

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE ⁽²⁾	TCKPS1 ⁽²⁾	TCKPS0 ⁽²⁾	—	—	TCS ^(2,3)	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **TON:** Timery On bit⁽²⁾

1 = Starts 16-bit Timery

0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timery Stop in Idle Mode bit⁽²⁾

1 = Discontinues module operation when device enters Idle mode

0 = Continues module operation in Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9-8 **TECS<1:0>:** Timery Extended Clock Source Select bits (selected when TCS = 1)^(2,3)

11 = Generic Timer (TMRCK) external input

10 = LPRC Oscillator

01 = TxCK external clock input

00 = SOSC

bit 7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit⁽²⁾

When TCS = 1:

This bit is ignored.

When TCS = 0:

1 = Gated time accumulation is enabled

0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timery Input Clock Prescale Select bits⁽²⁾

11 = 1:256

10 = 1:64

01 = 1:8

00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timery Clock Source Select bit^(2,3)

1 = External clock from pin, TyCK (on the rising edge)

0 = Internal clock (Fosc/2)

bit 0 **Unimplemented:** Read as '0'

Note 1: Changing the value of TyCON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

2: When 32-bit operation is enabled (T2CON<3> or T4CON<3> = 1), these bits have no effect on Timery operation; all timer functions are set through T2CON and T4CON.

3: If TCS = 1 and TECS<1:0> = x1, the selected external timer input (TyCK) must be configured to an available RPN/RPn pin. For more information, see **Section 11.5 "Peripheral Pin Select (PPS)"**.

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REGISTER 15-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—
bit 15						bit 8	

U-0	R/W-0	R/W-0	R-0, HSC	R-0, HSC	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2 ⁽¹⁾	ICM1 ⁽¹⁾	ICM0 ⁽¹⁾
bit 7						bit 0	

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture x Module Stop in Idle Control bit
 1 = Input capture module halts in CPU Idle mode
 0 = Input capture module continues to operate in CPU Idle mode

bit 12-10 **ICTSEL<2:0>:** Input Capture x Timer Select bits
 111 = System clock (Fosc/2)
 110 = Reserved
 101 = Reserved
 100 = Timer1
 011 = Timer5
 010 = Timer4
 001 = Timer2
 000 = Timer3

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **ICI<1:0>:** Select Number of Captures per Interrupt bits
 11 = Interrupt on every fourth capture event
 10 = Interrupt on every third capture event
 01 = Interrupt on every second capture event
 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture x Overflow Status Flag bit (read-only)
 1 = Input capture overflow has occurred
 0 = No input capture overflow has occurred

bit 3 **ICBNE:** Input Capture x Buffer Empty Status bit (read-only)
 1 = Input capture buffer is not empty, at least one more capture value can be read
 0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture x Mode Select bits⁽¹⁾
 111 = Interrupt mode: Input capture functions as an interrupt pin only when the device is in Sleep or Idle mode (rising edge detect only, all other control bits are not applicable)
 110 = Unused (module is disabled)
 101 = Prescaler Capture mode: Capture on every 16th rising edge
 100 = Prescaler Capture mode: Capture on every 4th rising edge
 011 = Simple Capture mode: Capture on every rising edge
 010 = Simple Capture mode: Capture on every falling edge
 001 = Edge Detect Capture mode: Capture on every edge (rising and falling); ICI<1:0> bits do not control interrupt generation for this mode
 000 = Input capture module is turned off

Note 1: The ICx input must also be configured to an available RPN/RPIn pin. For more information, see **Section 11.5 “Peripheral Pin Select (PPS)”**.

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FIGURE 17-4: SPIx MASTER/SLAVE CONNECTION (ENHANCED BUFFER MODES)

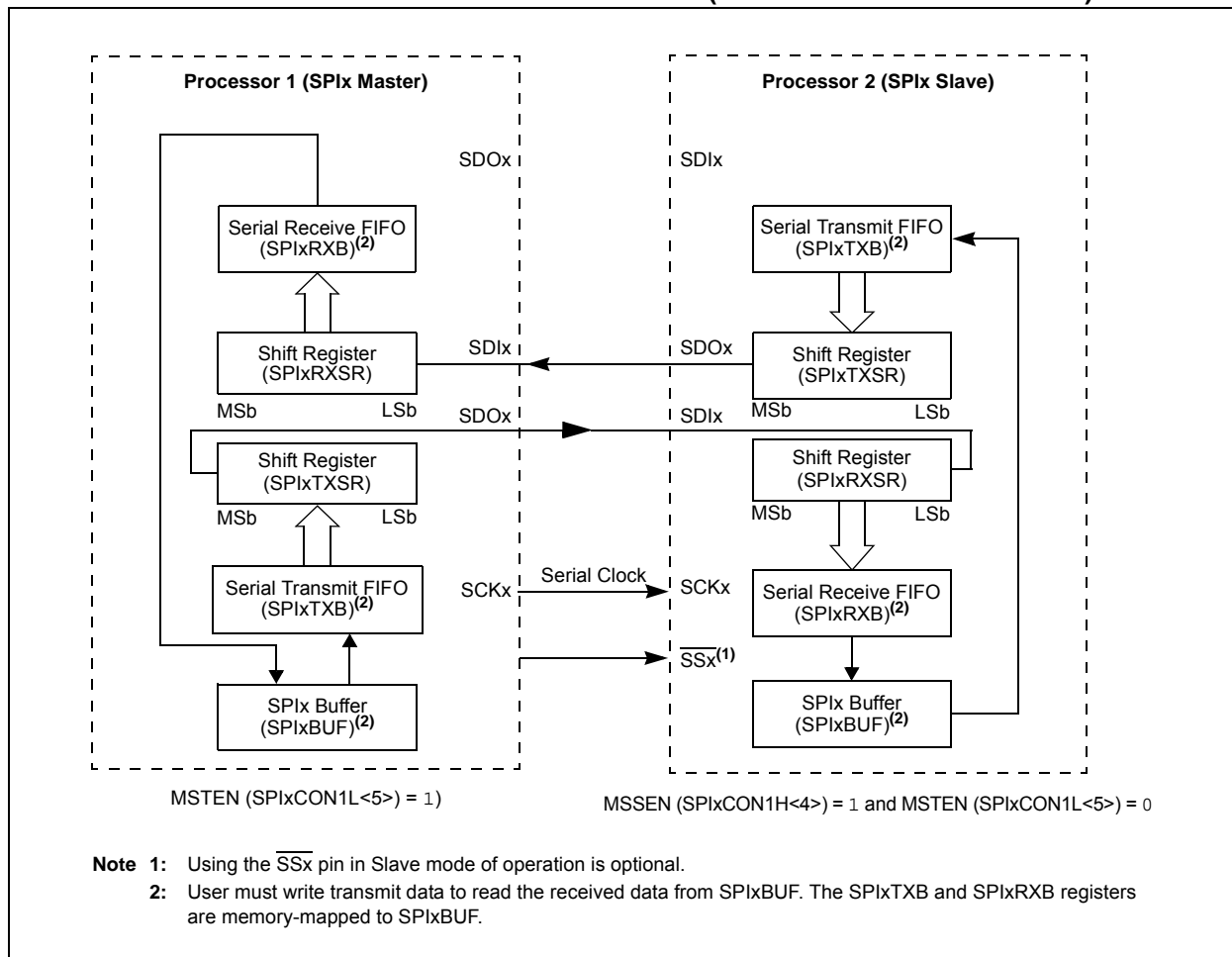
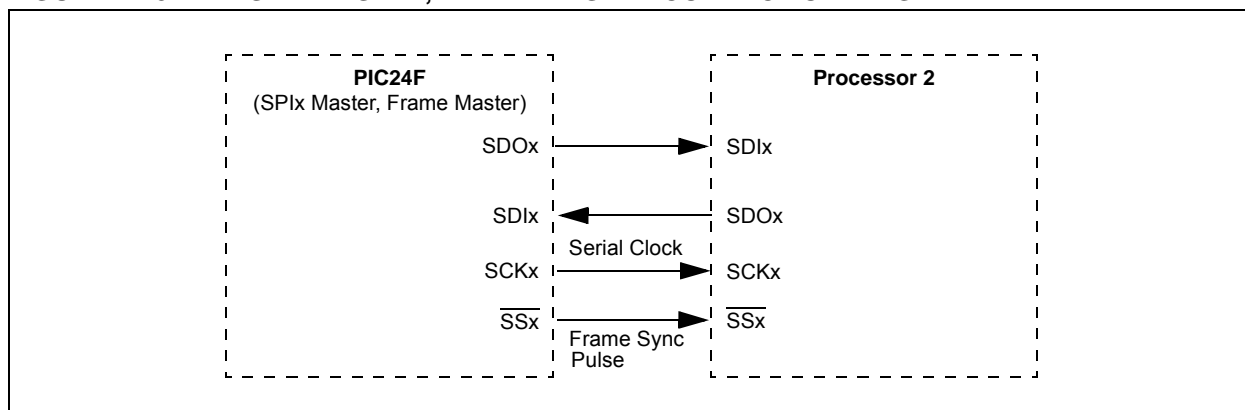


FIGURE 17-5: SPIx MASTER, FRAME MASTER CONNECTION DIAGRAM



PIC24FJ256GA412/GB412 FAMILY

REGISTER 19-2: UxSTAL: UARTx STATUS LOW AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0	R-0, HSC	R-1, HSC
UTXISEL1	UTXINV ⁽¹⁾	UTXISEL0	URXEN	UTXBRK	UTXEN ⁽²⁾	UTXBF	TRMT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-1, HSC	R-0, HSC	R-0, HSC	R/C-0, HS	R-0, HSC
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
HS = Hardware Settable bit	HC = Hardware Clearable bit	x = Bit is unknown

- bit 15,13 **UTXISEL<1:0>**: UARTx Transmission Interrupt Mode Selection bits
 11 = Reserved; do not use
 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR), and as a result, the transmit buffer becomes empty
 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 **UTXINV**: UARTx IrDA[®] Encoder Transmit Polarity Inversion bit⁽¹⁾
 For IREN = 0:
 1 = UxTX Idle state is '0'
 0 = UxTX Idle state is '1'
 For IREN = 1:
 1 = UxTX Idle state is '1'
 0 = UxTX Idle state is '0'
- bit 12 **URXEN**: UARTx Receive Enable bit
 1 = Receive is enabled, UxRX pin is controlled by UARTx
 0 = Receive is disabled, UxRX pin is controlled by the port
- bit 11 **UTXBRK**: UARTx Transmit Break bit
 1 = Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
 0 = Sync Break transmission is disabled or completed
- bit 10 **UTXEN**: UARTx Transmit Enable bit⁽²⁾
 1 = Transmit is enabled, UxTX pin is controlled by UARTx
 0 = Transmit is disabled, any pending transmission is aborted and the buffer is reset; UxTX pin is controlled by the port
- bit 9 **UTXBF**: UARTx Transmit Buffer Full Status bit (read-only)
 1 = Transmit buffer is full
 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 **TRMT**: Transmit Shift Register Empty bit (read-only)
 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
 0 = Transmit Shift Register is not empty, a transmission is in progress or queued

Note 1: The value of this bit only affects the transmit properties of the module when the IrDA encoder is enabled (IREN = 1).

2: If UARTEN = 1, the peripheral inputs and outputs must be configured to an available RPN/RPIN pin. For more information, see **Section 11.5 “Peripheral Pin Select (PPS)”**.

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REGISTER 20-16: U1IR: USB INTERRUPT STATUS REGISTER (DEVICE MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/K-0, HS	U-0	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS
STALLIF	—	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	K = Write '1' to Clear bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15-8 **Unimplemented:** Read as '0'
- bit 7 **STALLIF:** STALL Handshake Interrupt bit
 1 = A STALL handshake was sent by the peripheral during the handshake phase of the transaction in Device mode
 0 = A STALL handshake has not been sent
- bit 6 **Unimplemented:** Read as '0'
- bit 5 **RESUMEIF:** Resume Interrupt bit
 1 = A K-state is observed on the D+ or D- pin for 2.5 μ s (differential '1' for low speed, differential '0' for full speed)
 0 = No K-state is observed
- bit 4 **IDLEIF:** Idle Detect Interrupt bit
 1 = Idle condition is detected (constant Idle state of 3 ms or more)
 0 = No Idle condition is detected
- bit 3 **TRNIF:** Token Processing Complete Interrupt bit
 1 = Processing of the current token is complete; read the U1STAT register for endpoint information
 0 = Processing of the current token is not complete; clear the U1STAT register or load the next token from STAT (clearing this bit causes the STAT FIFO to advance)
- bit 2 **SOFIF:** Start-of-Frame Token Interrupt bit
 1 = A Start-of-Frame token is received by the peripheral or the Start-of-Frame threshold is reached by the host
 0 = No Start-of-Frame token is received or threshold reached
- bit 1 **UERRIF:** USB Error Condition Interrupt bit
 1 = An unmasked error condition has occurred; only error states enabled in the U1EIE register can set this bit
 0 = No unmasked error condition has occurred
- bit 0 **URSTIF:** USB Reset Interrupt bit
 1 = Valid USB Reset has occurred for at least 2.5 μ s; Reset state must be cleared before this bit can be reasserted
 0 = No USB Reset has occurred; individual bits can only be cleared by writing a '1' to the bit position as part of a word write operation on the entire register. Using Boolean instructions or bitwise operations to write to a single bit position will cause all set bits, at the moment of the write, to become cleared

Note: Individual bits can only be cleared by writing a '1' to the bit position as part of a word write operation on the entire register. Using Boolean instructions or bitwise operations to write to a single bit position will cause all set bits, at the moment of the write, to become cleared.

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REGISTER 21-5: PMCSxCF: EPMP CHIP SELECT x CONFIGURATION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
CSDIS	CSP	CSPTEN	BEP	—	WRSP	RDSP	SM
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
ACKP	PTSZ1	PTSZ0	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **CSDIS:** Chip Select x Disable bit
 1 = Disables the Chip Select x functionality
 0 = Enables the Chip Select x functionality
- bit 14 **CSP:** Chip Select x Polarity bit
 1 = Active-high (PMCSx)
 0 = Active-low (PMCSx)
- bit 13 **CSPTEN:** PMCSx Port Enable bit
 1 = PMCSx port is enabled
 0 = PMCSx port is disabled
- bit 12 **BEP:** Chip Select x Nibble/Byte Enable Polarity bit
 1 = Nibble/byte enable is active-high (PMBE0, PMBE1)
 0 = Nibble/byte enable is active-low (PMBE0, PMBE1)
- bit 11 **Unimplemented:** Read as '0'
- bit 10 **WRSP:** Chip Select x Write Strobe Polarity bit
For Slave Modes and Master Mode when SM = 0:
 1 = Write strobe is active-high (PMWR)
 0 = Write strobe is active-low (PMWR)
For Master Mode when SM = 1:
 1 = Enable strobe is active-high (PMENB)
 0 = Enable strobe is active-low (PMENB)
- bit 9 **RDSP:** Chip Select x Read Strobe Polarity bit
For Slave Modes and Master Mode when SM = 0:
 1 = Read strobe is active-high (PMRD)
 0 = Read strobe is active-low (PMRD)
For Master Mode when SM = 1:
 1 = Read/write strobe is active-high (PMRD/PMWR)
 0 = Read/Write strobe is active-low (PMRD/PMWR)
- bit 8 **SM:** Chip Select x Strobe Mode bit
 1 = Read/write and enable strobes (PMRD/PMWR and PMENB)
 0 = Read and write strobes (PMRD and PMWR)
- bit 7 **ACKP:** Chip Select x Acknowledge Polarity bit
 1 = ACK is active-high (PMACK1)
 0 = ACK is active-low (PMACK1)
- bit 6-5 **PTSZ<1:0>:** Chip Select x Port Size bits
 11 = Reserved
 10 = 16-bit port size (PMD<15:0>)
 01 = 4-bit port size (PMD<3:0>)
 00 = 8-bit port size (PMD<7:0>)
- bit 4-0 **Unimplemented:** Read as '0'

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REGISTER 25-4: CRYOTP: CRYPTOGRAPHIC OTP PAGE PROGRAM CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	KEYPSEL
bit 15							bit 8

R-x, HSC ⁽¹⁾	R/W-0 ⁽¹⁾	R/S-1, HC	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/S-0, HC ⁽²⁾
PGMTST	OTPIE	CRYREAD ^(3,4)	KEYPG3	KEYPG2	KEYPG1	KEYPG0	CRYWR ^(3,4)
bit 7							bit 0

Legend:	S = Settable Only bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
HC = Hardware Clearable bit		x = Bit is unknown

- bit 15-9 **Unimplemented:** Read as '0'
- bit 8 **KEYPSEL:** Key Storage Programming Select bit
 1 = Programming operations write to Key RAM
 0 = Programming operations write to the Secure OTP Array
- bit 7 **PGMTST:** Key Storage/Configuration Program Test bit⁽¹⁾
 This bit mirrors the state of the TSTPGM bit and is used to test the programming of the Secure OTP Array after programming.
 1 = TSTPGM (CFGPAGE<30>) is programmed ('1')
 0 = TSTPGM is not programmed ('0')
- bit 6 **OTPIE:** Key Storage/Configuration Program Interrupt Enable bit⁽¹⁾
 1 = Generates an interrupt when the current programming or read operation completes
 0 = Does not generate an interrupt when the current programming or read operation completes; software must poll the CRYWR, CRYREAD or CRYBSY bit to determine when the current programming operation is complete
- bit 5 **CRYREAD:** Cryptographic Key Storage/Configuration Read bit^(3,4)
 1 = This bit is set to start a read operation; read operation is in progress while this bit is set and CRYGO = 1
 0 = Read operation has completed
- bit 4-1 **KEYPG<3:0>:** Key Storage/Configuration Program Page Select bits⁽¹⁾
 1111
 ... = Reserved
 1001
 1000 = OTP Page 8
 0111 = OTP Page 7
 0110 = OTP Page 6
 0101 = OTP Page 5
 0100 = OTP Page 4
 0011 = OTP Page 3
 0010 = OTP Page 2
 0001 = OTP Page 1
 0000 = Configuration Page (CFGPAGE, OTP Page 0)
- bit 0 **CRYWR:** Cryptographic Key Storage/Configuration Program bit^(2,3,4)
 1 = Programs the Key Storage/Configuration bits with the value found in CRYTXTC<63:0>
 0 = Program operation has completed

- Note 1:** These bits are reset on system Resets or whenever the CRYMD bit (PMD8<0>) is set.
- Note 2:** These bits are reset on system Resets when the CRYMD bit is set or when CRYGO is cleared.
- Note 3:** Set this bit only when CRYON = 1 and CRYGO = 0. Do not set CRYREAD or CRYWR both, at any given time.
- Note 4:** Do not clear CRYON or these bits while they are set; always allow the hardware operation to complete and clear the bits automatically.

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NOTES:

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