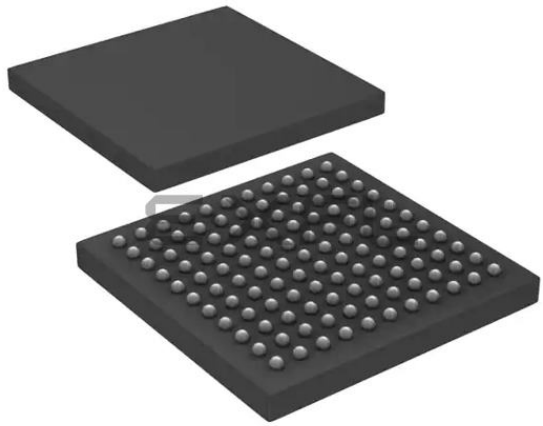
# Microchip Technology - PIC24FJ128GB412-I/BG Datasheet



**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

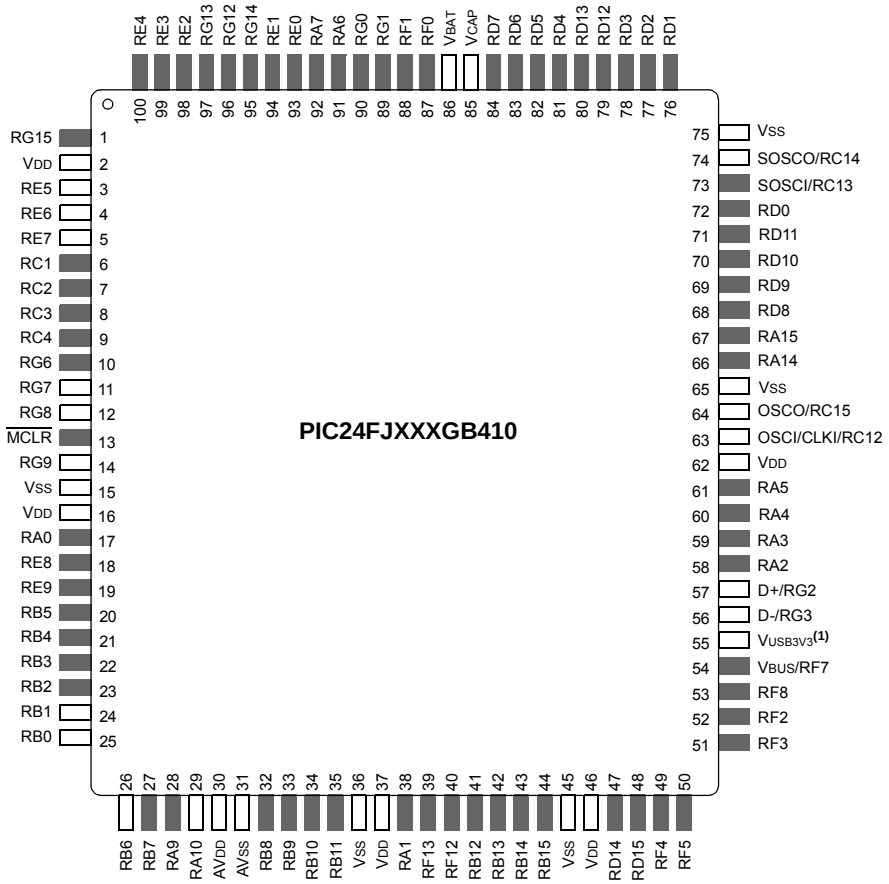
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT |
| Number of I/O | 101 |
| Program Memory Size | 128KB (43K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 24x10/12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 121-TFBGA |
| Supplier Device Package | 121-TFBGA (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128gb412-i-bg |

## Pin Diagrams (Continued)

**100-Pin TQFP**




**Legend:** **Shaded pins** indicate pins tolerant to up to +5.5 VDC. See Table 4 for a complete description of pin functions.
**Note 1:** PIC24FJ256GB410 devices use VUSB3V3 instead of RF6.

**TABLE 1-5: PIC24FJ256GB412 FAMILY PINOUT DESCRIPTION (CONTINUED)**

| Pin Function | Pin/Pad Number | | | I/O | Input Buffer | Description |
|---|---|---|---|---|---|---|
| | 64-Pin TQFP | 100-Pin TQFP | 121-Pin TFBGA | | | |
| SEG0 | 4 | 10 | E3 | O | ANA | LCD Driver Segment Outputs |
| SEG1 | 8 | 14 | F3 | O | ANA | |
| SEG2 | 11 | 20 | H1 | O | ANA | |
| SEG3 | 12 | 21 | H2 | O | ANA | |
| SEG4 | 13 | 22 | J1 | O | ANA | |
| SEG5 | 14 | 23 | J2 | O | ANA | |
| SEG6 | 15 | 24 | K1 | O | ANA | |
| SEG7 | 16 | 25 | K2 | O | ANA | |
| SEG8 | 29 | 43 | K7 | O | ANA | |
| SEG9 | 30 | 44 | L8 | O | ANA | |
| SEG10 | 31 | 49 | L10 | O | ANA | |
| SEG11 | 32 | 50 | L11 | O | ANA | |
| SEG12 | 33 | 51 | K10 | O | ANA | |
| SEG13 | 42 | 68 | E9 | O | ANA | |
| SEG14 | 43 | 69 | E10 | O | ANA | |
| SEG15 | 44 | 70 | D11 | O | ANA | |
| SEG16 | 45 | 71 | C11 | O | ANA | |
| SEG17 | 46 | 72 | D9 | O | ANA | |
| SEG18 | 27 | 41 | J7 | O | ANA | |
| SEG19 | 28 | 42 | L7 | O | ANA | |
| SEG20 | 49 | 76 | A11 | O | ANA | |
| SEG21 | 50 | 77 | A10 | O | ANA | |
| SEG22 | 51 | 78 | B9 | O | ANA | |
| SEG23 | 52 | 81 | C8 | O | ANA | |
| SEG24 | 53 | 82 | B8 | O | ANA | |
| SEG25 | 54 | 83 | D7 | O | ANA | |
| SEG26 | 55 | 84 | C7 | O | ANA | |
| SEG27 | 58 | 87 | B6 | O | ANA | |
| SEG28 | — | 61 | G9 | O | ANA | |
| SEG29 | 23 | 34 | H5 | O | ANA | |
| SEG30 | 22 | 33 | L4 | O | ANA | |
| SEG31 | 21 | 32 | K4 | O | ANA | |
| SEG32 | — | 6 | D1 | O | ANA | |
| SEG33 | — | 8 | E2 | O | ANA | |
| SEG34 | — | 18 | G1 | O | ANA | |
| SEG35 | — | 19 | G2 | O | ANA | |
| SEG36 | — | 28 | L2 | O | ANA | |
| SEG37 | — | 29 | K3 | O | ANA | |
| SEG38 | — | 47 | L9 | O | ANA | |
| SEG39 | — | 48 | K9 | O | ANA | |
| SEG40 | — | 52 | K11 | O | ANA | |

**Legend:** TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
$I^2C$ = $I^2C$/SMBus input buffer
XCVR = Dedicated transceiver

**TABLE 1-5: PIC24FJ256GB412 FAMILY PINOUT DESCRIPTION (CONTINUED)**

| Pin Function | Pin/Pad Number | | | I/O | Input Buffer | Description |
|---|---|---|---|---|---|---|
| | 64-Pin TQFP | 100-Pin TQFP | 121-Pin TFBGA | | | |
| SEG41 | — | 53 | J10 | O | ANA | LCD Driver Segment Outputs |
| SEG42 | — | 66 | E11 | O | ANA | |
| SEG43 | — | 67 | E8 | O | ANA | |
| SEG44 | — | 79 | A9 | O | ANA | |
| SEG45 | — | 80 | D8 | O | ANA | |
| SEG46 | — | 89 | E6 | O | ANA | |
| SEG47 | 59 | 88 | A6 | O | ANA | |
| SEG48 | — | 17 | G3 | O | ANA | |
| SEG49 | — | 90 | A5 | O | ANA | |
| SEG50 | — | 1 | B2 | O | ANA | |
| SEG51 | — | 7 | E4 | O | ANA | |
| SEG52 | — | 9 | E1 | O | ANA | |
| SEG53 | — | 39 | L6 | O | ANA | |
| SEG54 | — | 40 | K6 | O | ANA | |
| SEG55 | — | 58 | H11 | O | ANA | |
| SEG56 | — | 59 | G10 | O | ANA | |
| SEG57 | — | 91 | C5 | O | ANA | |
| SEG58 | — | 92 | B5 | O | ANA | |
| SEG59 | — | 95 | C4 | O | ANA | |
| SEG60 | — | 96 | C3 | O | ANA | |
| SEG61 | — | 97 | A3 | O | ANA | |
| SEG62 | 64 | 100 | A1 | O | ANA | |
| SEG63 | 18 | 27 | J3 | O | ANA | |
| SOSCI | 47 | 73 | C10 | — | — | Secondary Oscillator/Timer1 Clock Input |
| SOSCO | 48 | 74 | B11 | — | — | Secondary Oscillator/Timer1 Clock Output |
| $\overline{SS4}$/FSYNC4 | 24 | 35 | K5 | I/O | DIG/ST | SPI4 Slave Select/Frame Sync |
| T1CK | 22 | 33 | L4 | I | ST | Timer1 Clock |
| TCK | 27 | 38 | J6 | I | ST | JTAG Test Clock/Programming Clock Input |
| TDI | 28 | 60 | G11 | I | ST | JTAG Test Data/Programming Data Input |
| TDO | 24 | 61 | G9 | O | DIG | JTAG Test Data Output |
| $\overline{TMPR}$ | 22 | 33 | L4 | — | — | Tamper Detect Input |
| TMS | 23 | 17 | G3 | I | ST | JTAG Test Mode Select Input |
| $\overline{U5CTS}$ | 58 | 87 | B6 | I | ST | UART5 Clear-to-Send Output |
| $\overline{U5RTS}$/U5BCLK | 55 | 84 | C7 | O | DIG | UART5 Request-to-Send Input |
| U5RX | 54 | 83 | D7 | I | ST | UART5 Receive Input |
| U5TX | 49 | 76 | A11 | O | DIG | UART5 Transmit Output |
| $\overline{U6CTS}$ | 46 | 72 | D9 | I | ST | UART6 Clear-to-Send Output |
| $\overline{U6RTS}$/U6BCLK | 42 | 68 | E9 | O | DIG | UART6 Request-to-Send Input |
| U6RX | 27 | 41 | J7 | I | ST | UART6 Receive Input |
| U6TX | 18 | 27 | J3 | O | DIG | UART6 Transmit Output |

**Legend:** TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
$I^2C$ = $I^2C$/SMBus input buffer
XCVR = Dedicated transceiver

## 2.7 Configuration of Analog and Digital Pins During ICSP Operations

If an ICSP compliant emulator is selected as a debugger, it automatically initializes all of the A/D input pins (ANx) as “digital” pins. This is done by clearing all bits in the ANSx registers. Refer to **Section 11.2 “Configuring Analog Port Pins (ANSx)”** for more specific information.

The bits in these registers that correspond to the A/D pins that initialized the emulator must not be changed by the user application; otherwise, communication errors will result between the debugger and the device.

If your application needs to use certain A/D pins as analog input pins during the debug session, it must set the bits corresponding to the pin(s) to be configured as analog. Do not change any other bits, particularly those corresponding to the PGECx/PGEDx pair, at any time.

When a Microchip debugger/emulator is used as a programmer, the user application must correctly configure the ANSx registers. Automatic initialization of these registers is only done during debugger operation. Failure to correctly configure the register(s) will result in all A/D pins being recognized as analog input pins, resulting in the port value being read as a logic ‘0’, which may affect user application functionality.

## 2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to VSS on unused pins and drive the output to logic low.

## 8.3 Interrupt Control and Status Registers

The PIC24FJ256GA412/GB412 family of devices implements a total of 50 registers for the interrupt controller:

- INTCON1
- INTCON2
- INTCON4
- IFS0 through IFS7
- IEC0 through IEC7
- IPC0 through ICP29
- INTTREG

Global interrupt control functions are controlled from INTCON1 and INTCON2. INTCON1 contains the Interrupt Nesting Disable (NSTDIS) bit, as well as the control and status flags for the processor trap sources. The INTCON2 register controls global interrupt generation, the external interrupt request signal behavior and the use of the Alternate Interrupt Vector Table (AIVT). INTCON2 and INTCON4 also contain status flags for various hardware trap events.

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or an external signal and is cleared via software.

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number (VECNUM<6:0>) and the Interrupt Priority Level (ILR<3:0>) bit fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the order of their vector numbers, as shown in Table 8-2. For example, the INT0 (External Interrupt 0) is shown as having a vector number and a natural order priority of 0. Thus, the INT0IF status bit is found in IFS0<0>, the INT0IE enable bit in IEC0<0> and the INT0IP<2:0> priority bits in the first position of IPC0 (IPC0<2:0>).

Although they are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. The ALU STATUS Register (SR) contains the IPL<2:0> bits (SR<7:5>). These indicate the current CPU Interrupt Priority Level. The user can change the current CPU priority level by writing to the IPLx bits.

The CORCON register contains the IPL3 bit, which together with the IPL<2:0> bits, indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

The interrupt controller has the Interrupt Controller Test register, INTTREG, which displays the status of the interrupt controller. When an interrupt request occurs, its associated vector number and the new Interrupt Priority Level are latched into INTTREG. This information can be used to determine a specific interrupt source if a generic ISR is used for multiple vectors (such as when ISR remapping is used in bootloader applications) or to check if another interrupt is pending while in an ISR.

All Interrupt registers are described in Register 8-3 through Register 8-52 in the succeeding pages.

**REGISTER 8-17: IEC3: INTERRUPT ENABLE CONTROL REGISTER 3**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CCP1IE | RTCIE | DMA5IE | SPI3RXIE | SPI2RXIE | SPI1RXIE | SPI4RXIE | KEYSTRIE |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CRYDNIE | INT4IE(1) | INT3IE(1) | — | CCT7IE | MI2C2IE | SI2C2IE | CCT6IE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CCP1IE:** MCCP1 Capture/Compare Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 14 **RTCIE:** Real-Time Clock and Calendar Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13 **DMA5IE:** DMA Channel 5 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12 **SPI3RXIE:** SPI3 Receive Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 11 **SPI2RXIE:** SPI2 Receive Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 10 **SPI1RXIE:** SPI1 Receive Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 9 **SPI4RXIE:** SPI4 Receive Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 8 **KEYSTRIE:** Cryptographic Key Store Program Done Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 7 **CRYDNIE:** Cryptographic Operation Done Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 6 **INT4IE:** External Interrupt 4 Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 5 **INT3IE:** External Interrupt 3 Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 4 **Unimplemented:** Read as '0'

**Note 1:** If an external interrupt is enabled, the interrupt input must also be configured to an available RPn or RPIn pin. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

**REGISTER 8-40: IPC18: INTERRUPT PRIORITY CONTROL REGISTER 18**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | CCP7IP2 | CCP7IP1 | CCP7IP0 | — | HLVDIP2 | HLVDIP1 | HLVDIP0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-4 **CCP7IP<2:0>:** SCCP7 Capture/Compare Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **HLVDIP<2:0>:** High/Low-Voltage Detect Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

**REGISTER 9-5: REFOCONH: REFERENCE CLOCK CONTROL HIGH REGISTER**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | RODIV<14:8> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| RODIV<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-0 **RODIV<14:0>:** Reference Clock Integer Divisor Select bits
Divisor for the selected input clock source is two times the selected value.
111 1111 1111 1111 = Base clock value divided by 65,534 (2 * 7FFFh)
111 1111 1111 1110 = Base clock value divided by 65,532 (2 * 7FFEh)
111 1111 1111 1101 = Base clock value divided by 65,530 (2 * 7FFDh)
• • •
000 0000 0000 0010 = Base clock value divided by 4 (2 * 2)
000 0000 0000 0001 = Base clock value divided by 2 (2 * 1)
000 0000 0000 0000 = Base clock value

**REGISTER 9-6: REFOTRIML: REFERENCE CLOCK TRIM REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ROTRIM<8:1> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| ROTRIM0 | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **ROTRIM<8:0>:** Reference Clock Fractional Divisor Select bits
Added fractional portion of the divisor for the selected input clock source is the value, divided by 512.
111111111 = 1 (512/512)
111111110 = 0.998947 (511/512)
111111101 = 0.996094 (510/512)
• • •
000000010 = 0.003906 (2/512)
000000001 = 0.001953 (1/512)
000000000 = No fractional portion (0/512)

bit 6-0 **Unimplemented:** Read as '0'

Once the device wakes back up, all I/O pins continue to maintain their previous states, even after the device has finished the POR sequence and is executing application code again. Pins configured as inputs during Deep Sleep remain high-impedance and pins configured as outputs continue to drive their previous value. After waking up, the TRISx and LATx registers, and the SOSCEN bit (OSCCON<1>), are reset. If firmware modifies any of these bits or registers, the I/O will not immediately go to the newly configured states. Once the firmware clears the RELEASE bit (DSCON<0>), the I/O pins are “released”. This causes the I/O pins to take the states configured by their respective TRISx and LATx bit values.

This means that keeping the SOSC running after waking up requires the SOSCEN bit to be set before clearing RELEASE.

If the Deep Sleep BOR (DSBOR) is enabled, and a DSBOR or a true POR event occurs during Deep Sleep, the I/O pins will be immediately released, similar to clearing the RELEASE bit. All previous state information will be lost, including the general purpose DSGPR0 and DSGPR1 contents.

If a $\overline{\text{MCLR}}$ Reset event occurs during Deep Sleep, the DSGPRx, DSCON and DSWAKE registers will remain valid, and the RELEASE bit will remain set. The state of the SOSC will also be retained. The I/O pins, however, will be reset to their $\overline{\text{MCLR}}$ Reset state. Since RELEASE is still set, changes to the SOSCEN bit (OSCCON<1>) cannot take effect until the RELEASE bit is cleared.

In all other Deep Sleep wake-up cases, application firmware must clear the RELEASE bit in order to reconfigure the I/O pins.

### 10.4.5 DEEP SLEEP WDT

To enable the DSWDT in Deep Sleep mode, program the Configuration bit, DSWDTEN (FDS<7>). The device WDT need not be enabled for the DSWDT to function. Entry into Deep Sleep modes automatically resets the DSWDT.

The DSWDT clock source is selected by the DSWDTOSC Configuration bit (FDS<5>). The postscaler options are programmed by the DSWDTPS<4:0> Configuration bits (FDS<4:0>). The minimum time-out period that can be achieved is 1 ms and the maximum is 25.7 days. For more details on DSWDT configuration options, refer to **Section 33.0 “Special Features”**.

#### 10.4.5.1 Switching Clocks in Deep Sleep Mode

Both the RTCC and the DSWDT may run from either SOSC or the LPRC clock source. This allows both the RTCC and DSWDT to run without requiring both the LPRC and SOSC to be enabled together, reducing power consumption.

Running the RTCC from LPRC will result in a loss of accuracy in the RTCC, of approximately 5 to 10%. If a more accurate RTCC is required, it must be run from the SOSC clock source. The RTCC clock source is selected with the CLKSEL<1:0> bits (RTCCON2L<1:0>).

Under certain circumstances, it is possible for the DSWDT clock source to be off when entering Deep Sleep mode. In this case, the clock source is turned on automatically (if DSWDT is enabled) without the need for software intervention. However, this can cause a delay in the start of the DSWDT counters. In order to avoid this delay when using SOSC as a clock source, the application can activate SOSC prior to entering Deep Sleep mode.

### 10.4.6 CHECKING AND CLEARING THE STATUS OF DEEP SLEEP

Upon entry into Deep Sleep mode, the status bit, DPSLP (RCON<10>), becomes set and must be cleared by the software.

On power-up, the software should read this status bit to determine if the Reset was due to an exit from Deep Sleep mode and clear the bit if it is set. Of the four possible combinations of DPSLP and POR bit states, three cases can be considered:

- Both the DPSLP and POR bits are cleared. In this case, the Reset was due to some event other than a Deep Sleep mode exit.
- The DPSLP bit is clear, but the POR bit is set; this is a normal POR.
- Both the DPSLP and POR bits are set. This means that Deep Sleep mode was entered, the device was powered down and Deep Sleep mode was exited.

### 10.4.7 POWER-ON RESETS (PORs)

$V_{DD}$ voltage is monitored to produce PORs. Since exiting from Deep Sleep mode functionally looks like a POR, the technique described in **Section 10.4.6 “Checking and Clearing the Status of Deep Sleep”** should be used to distinguish between Deep Sleep and a true POR event. When a true POR occurs, the entire device, including all Deep Sleep logic (Deep Sleep registers, RTCC, DSWDT, etc.), is reset.

**REGISTER 10-5: PMD2: PERIPHERAL MODULE DISABLE REGISTER 2**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | IC6MD | IC5MD | IC4MD | IC3MD | IC2MD | IC1MD |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | OC6MD | OC5MD | OC4MD | OC3MD | OC2MD | OC1MD |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **IC6MD:** Input Capture 6 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 12 **IC5MD:** Input Capture 5 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 11 **IC4MD:** Input Capture 4 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 10 **IC3MD:** Input Capture 3 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 9 **IC2MD:** Input Capture 2 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 8 **IC1MD:** Input Capture 1 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **OC6MD:** Output Capture 6 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 4 **OC5MD:** Output Capture 5 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 3 **OC4MD:** Output Capture 4 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 2 **OC3MD:** Output Capture 3 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 1 **OC2MD:** Output Capture 2 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 0 **OC1MD:** Output Capture 1 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

**REGISTER 17-7: SPIxIMSKH: SPIx INTERRUPT MASK REGISTER HIGH**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| RXWIEN | — | RXMSK5(1) | RXMSK4(1,4) | RXMSK3(1,3) | RXMSK2(1,2) | RXMSK1(1) | RXMSK0(1) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TXWIEN | — | TXMSK5(1) | TXMSK4(1,4) | TXMSK3(1,3) | TXMSK2(1,2) | TXMSK1(1) | TXMSK0(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **RXWIEN:** Receive Watermark Interrupt Enable bit
1 = Triggers receive buffer element watermark interrupt when RXMSK<5:0> ≤ RXELM<5:0>
0 = Disables receive buffer element watermark interrupt

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **RXMSK<5:0>:** RX Buffer Mask bits(1,2,3,4)
RX mask bits; used in conjunction with the RXWIEN bit.

bit 7 **TXWIEN:** Transmit Watermark Interrupt Enable bit
1 = Triggers transmit buffer element watermark interrupt when TXMSK<5:0> = TXELM<5:0>
0 = Disables transmit buffer element watermark interrupt

bit 6 **Unimplemented:** Read as '0'

bit 5-0 **TXMSK<5:0>:** TX Buffer Mask bits(1,2,3,4)
TX mask bits; used in conjunction with the TXWIEN bit.

**Note 1:** Mask values higher than FIFODEPTH are not valid. The module will not trigger a match for any value in this case.
**2:** RXMSK2 and TXMSK2 bits are only present when FIFODEPTH = 8 or higher.
**3:** RXMSK3 and TXMSK3 bits are only present when FIFODEPTH = 16 or higher.
**4:** RXMSK4 and TXMSK4 bits are only present when FIFODEPTH = 32.

## 18.0 INTER-INTEGRATED CIRCUIT ($I^2C$)

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Inter-Integrated Circuit ($I^2C$)"** (DS70000195). The information in this data sheet supersedes the information in the FRM.

The Inter-Integrated Circuit ($I^2C$) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, display drivers, A/D Converters, etc.

The $I^2C$ module supports these features:

- Independent Master and Slave Logic
- 7-Bit and 10-Bit Device Addresses
- General Call Address as Defined in the $I^2C$ Protocol
- Clock Stretching to Provide Delays for the Processor to Respond to a Slave Data Request
- Both 100 kHz and 400 kHz Bus Specifications
- Configurable Address Masking
- Multi-Master Modes to Prevent Loss of Messages in Arbitration
- Bus Repeater mode, Allowing the Acceptance of All Messages as a Slave, Regardless of the Address
- Automatic SCL

A block diagram of the module is shown in Figure 18-1.

### 18.1 Communicating as a Master in a Single Master Environment

The details of sending a message in Master mode depends on the communications protocol for the device being communicated with. Typically, the sequence of events is as follows:

1. Assert a Start condition on SDAx and SCLx.
2. Send the $I^2C$ device address byte to the slave with a write indication.
3. Wait for and verify an Acknowledge from the slave.
4. Send the first data byte (sometimes known as the command) to the slave.
5. Wait for and verify an Acknowledge from the slave.
6. Send the serial memory address low byte to the slave.
7. Repeat Steps 4 and 5 until all data bytes are sent.
8. Assert a Repeated Start condition on SDAx and SCLx.
9. Send the device address byte to the slave with a read indication.
10. Wait for and verify an Acknowledge from the slave.
11. Enable master reception to receive serial memory data.
12. Generate an ACK or NACK condition at the end of a received byte of data.
13. Generate a Stop condition on SDAx and SCLx.

**REGISTER 21-1: PMCON1: EPMP CONTROL REGISTER 1**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PMEN | — | PSIDL | ADRMUX1 | ADRMUX0 | — | MODE1 | MODE0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CSF1 | CSF0 | ALP | ALMODE | — | BUSKEEP | IRQM1 | IRQM0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **PMEN:** Parallel Master Port Enable bit
1 = EPMP is enabled
0 = EPMP is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **PSIDL:** Parallel Master Port Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
11 = Lower address bits are multiplexed with data bits using 3 address phases
10 = Lower address bits are multiplexed with data bits using 2 address phases
01 = Lower address bits are multiplexed with data bits using 1 address phase
00 = Address and data appear on separate pins

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits
11 = Master mode
10 = Enhanced PSP; pins used are PMRD, PMWR, PMCS, PMD<7:0> and PMA<1:0>
01 = Buffered PSP; pins used are PMRD, PMWR, PMCS and PMD<7:0>
00 = Legacy Parallel Slave Port; pins used are PMRD, PMWR, PMCS and PMD<7:0>

bit 7-6 **CSF<1:0>:** Chip Select Function bits
11 = Reserved
10 = PMA15 is used for Chip Select 2, PMA14 is used for Chip Select 1
01 = PMA15 is used for Chip Select 2, PMCS1 is used for Chip Select 1
00 = PMCS2 is used for Chip Select 2, PMCS1 is used for Chip Select 1

bit 5 **ALP:** Address Latch Polarity bit
1 = Active-high (PMALL, PMALH and PMALU)
0 = Active-low ($\overline{\text{PMALL}}$, $\overline{\text{PMALH}}$ and $\overline{\text{PMALU}}$)

bit 4 **ALMODE:** Address Latch Strobe Mode bit
1 = Enables "smart" address strobes (each address phase is only present if the current access would cause a different address in the latch than the previous address)
0 = Disables "smart" address strobes

bit 3 **Unimplemented:** Read as '0'

bit 2 **BUSKEEP:** Bus Keeper bit
1 = Data bus keeps its last value when not actively being driven
0 = Data bus is in a high-impedance state when not actively being driven

bit 1-0 **IRQM<1:0>:** Interrupt Request Mode bits
11 = Interrupt is generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode), or on a read or write operation when PMA<1:0> = 11 (Addressable PSP mode only)
10 = Reserved
01 = Interrupt is generated at the end of a read/write cycle
00 = No interrupt is generated

**REGISTER 23-5: CLCxGLSH: CLCx GATE LOGIC INPUT SELECT HIGH REGISTER (CONTINUED)**

bit 3 **G3D2T:** Gate 3 Data Source 2 True Enable bit
1 = Data Source 2 inverted signal is enabled for Gate 3
0 = Data Source 2 inverted signal is disabled for Gate 3

bit 2 **G3D2N:** Gate 3 Data Source 2 Negated Enable bit
1 = Data Source 2 inverted signal is enabled for Gate 3
0 = Data Source 2 inverted signal is disabled for Gate 3

bit 1 **G3D1T:** Gate 3 Data Source 1 True Enable bit
1 = Data Source 1 inverted signal is enabled for Gate 3
0 = Data Source 1 inverted signal is disabled for Gate 3

bit 0 **G3D1N:** Gate 3 Data Source 1 Negated Enable bit
1 = Data Source 1 inverted signal is enabled for Gate 3
0 = Data Source 1 inverted signal is disabled for Gate 3

## 27.0 12-BIT A/D CONVERTER WITH THRESHOLD DETECT

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the 12-Bit A/D Converter, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"12-Bit A/D Converter with Threshold Detect"** (DS39739). The information in this data sheet supersedes the information in the FRM.

The 12-bit A/D Converter has the following key features:

- Successive Approximation Register (SAR) Conversion
- Conversion Speeds of up to 200 ksps
- Up to 20 Analog Input Channels (internal and external)
- Selectable 10-Bit or 12-Bit (default) Conversion Resolution
- Multiple Internal Reference Input Channels
- External Voltage Reference Input Pins
- Unipolar Differential Sample-and-Hold (S/H) Amplifier
- Automated Threshold Scan and Compare Operation to Pre-Evaluate Conversion Results
- Selectable Conversion Trigger Source
- Fixed Length (one word per channel), Configurable Conversion Result Buffer
- Four Options for Results Alignment
- Configurable Interrupt Generation
- Enhanced DMA Operations with Indirect Address Generation
- Operation During CPU Sleep and Idle modes

The 12-bit A/D Converter module is an enhanced version of the 10-bit module offered in earlier PIC24 devices. It is a Successive Approximation Register (SAR) Converter, enhanced with 12-bit resolution, a wide range of automatic sampling options, tighter integration with other analog modules and a configurable results buffer.

It also includes a unique Threshold Detect feature that allows the module itself to make simple decisions based on the conversion results, and enhanced operation with the DMA Controller through Peripheral Indirect Addressing (PIA).

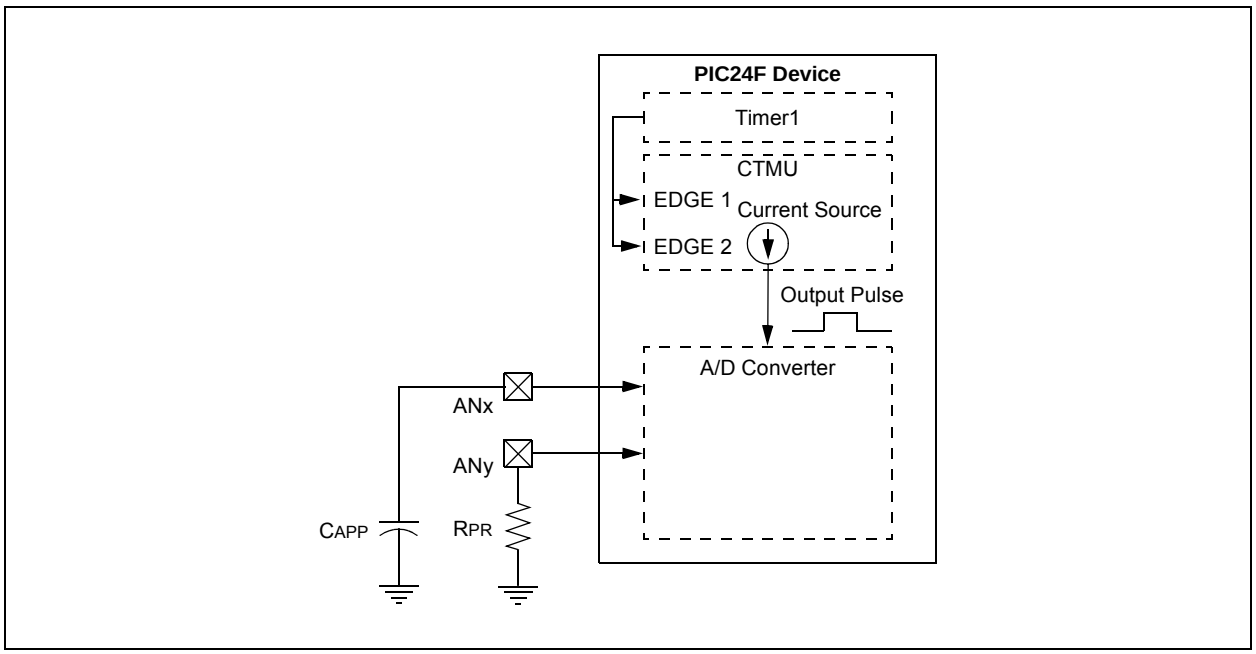
A simplified block diagram for the module is shown in Figure 27-1.

### 27.1 Basic Operation

To perform a standard A/D conversion:

1. Configure the module:
   a) Configure port pins as analog inputs by setting the appropriate bits in the ANSx registers (see **Section 11.2 "Configuring Analog Port Pins (ANSx)"** for more information).
   b) Select the voltage reference source to match the expected range on analog inputs (AD1CON2<15:13>).
   c) Select the positive and negative multiplexer inputs for each channel (AD1CHS<15:0>).
   d) Select the analog conversion clock to match the desired data rate with the processor clock (AD1CON3<7:0>).
   e) Select the appropriate sample/conversion sequence (AD1CON1<7:4> and AD1CON3<12:8>).
   f) For Channel A scanning operations, select the positive channels to be included (AD1CSSH and AD1CSSL registers).
   g) Select how conversion results are presented in the buffer (AD1CON1<9:8> and AD1CON5 register).
   h) Select the interrupt rate (AD1CON2<6:2>).
   i) Turn on A/D module (AD1CON1<15>).
2. Configure the A/D interrupt (if required):
   a) Clear the AD1IF bit (IFS0<13>).
   b) Enable the AD1IE interrupt (IEC0<13>).
   c) Select the A/D interrupt priority (IPC3<6:4>).
3. If the module is configured for manual sampling, set the SAMP bit (AD1CON1<1>) to begin sampling.

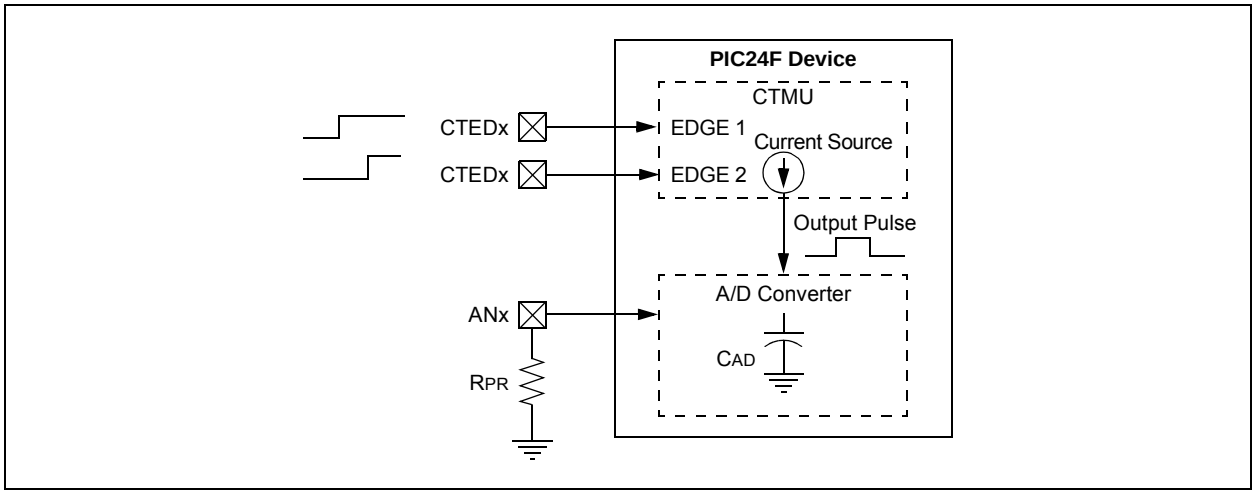
**FIGURE 31-1: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR CAPACITANCE MEASUREMENT**




## 31.2 Measuring Time

Time measurements on the pulse width can be similarly performed using the A/D module's Internal Capacitor ($C_{AD}$) and a precision resistor for current calibration. Figure 31-2 displays the external connections used for time measurements, and how the CTMU and A/D modules are related in this application. This example also shows both edge events coming from the external CTEDx pins, but other configurations using internal edge sources are possible.

**FIGURE 31-2: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR TIME MEASUREMENT**



**REGISTER 33-10: FDEVOPT1: DEVICE OPTIONS CONFIGURATION WORD**

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 23 | | | | | | | bit 16 |

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-1 | U-1 | U-1 | R/PO-1 | R/PO-1 | R/PO-1 | R/PO-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | ALTVREF(1) | TMPRWIPE | TMPRPIN | ALTCMPI(2) | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | PO = Program Once bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 23-5 **Unimplemented:** Read as '1'

bit 4 **ALTVREF:** Alternate External Voltage Reference Location Select bit(1)
1 = VREF+/CVREF+/DVREF+ and VREF-/CVREF- are mapped to RA10 and RA9, respectively
0 = VREF+/CVREF+/DVREF+ and VREF-/CVREF- are mapped to RB0 and RB1, respectively

bit 3 **TMPRWIPE:** Erase Key RAM on Tamper Event Enable Pin bit
1 = Cryptographic Engine Key RAM is not erased on $\overline{\text{TMPR}}$ pin events
0 = Cryptographic Engine Key RAM is erased when a $\overline{\text{TMPR}}$ pin event is detected

bit 2 **TMPRPIN:** Tamper Pin Disable bit
1 = $\overline{\text{TMPR}}$ pin is disabled
0 = $\overline{\text{TMPR}}$ pin is enabled

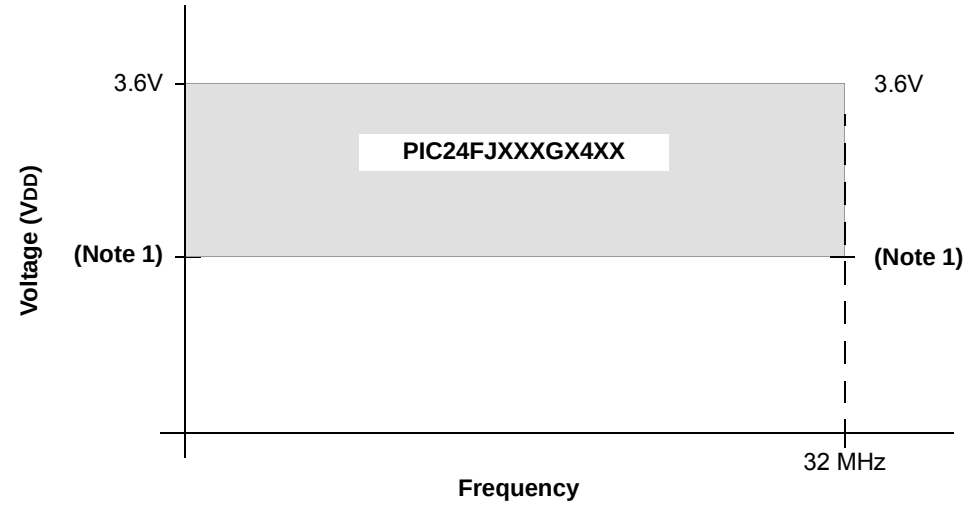
bit 1 **ALTCMPI:** Alternate Comparator Input Location Select bit(2)
1 = C1INC, C2INC and C3INC are mapped to their default pin locations
0 = C1INC, C2INC and C3INC are all mapped to RG9

bit 0 **Unimplemented:** Read as '1'

**Note 1:** Unimplemented on 64-pin devices; maintain this bit as '0' in those devices.
**2:** Unimplemented in PIC24FJXXXGAXXX devices.

## 36.1 DC Characteristics

**FIGURE 36-1: PIC24FJ256GA412/GB412 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)**




**Note 1:** Lower recommended operating boundary is 2.0V or VBOR (when BOR is enabled). For best analog performance, operation above 2.2V is suggested, but not required.

**TABLE 36-1: THERMAL OPERATING CONDITIONS**

| Rating | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| PIC24FJ256GA412/GB412 Family: | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +100 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +85 | °C |
| Power Dissipation:<br>Internal Chip Power Dissipation: PINT = VDD x (IDD – Σ IOH)<br>I/O Pin Power Dissipation:<br>PI/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL) | PD | PINT + PI/O | | | W |
| Maximum Allowed Power Dissipation | PDMAX | (TJMAX – TA)/θJA | | | W |

**TABLE 36-2: THERMAL PACKAGING CHARACTERISTICS**

| Characteristic | Symbol | Typ | Max | Unit | Note |
|---|---|---|---|---|---|
| Package Thermal Resistance, 12x12x1 mm 100-pin TQFP | θJA | 45.0 | — | °C/W | **(Note 1)** |
| Package Thermal Resistance, 10x10x1 mm 64-pin TQFP | θJA | 48.3 | — | °C/W | **(Note 1)** |
| Package Thermal Resistance, 9x9x0.9 mm 64-pin QFN | θJA | 28.0 | — | °C/W | **(Note 1)** |
| Package Thermal Resistance, 10x10x1.1 mm 121-pin TFBGA | θJA | 40.2 | — | °C/W | **(Note 1)** |

**Note 1:** Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

**FIGURE 36-13: SPIx MODULE MASTER MODE TIMING CHARACTERISTICS (CKE = 0)**

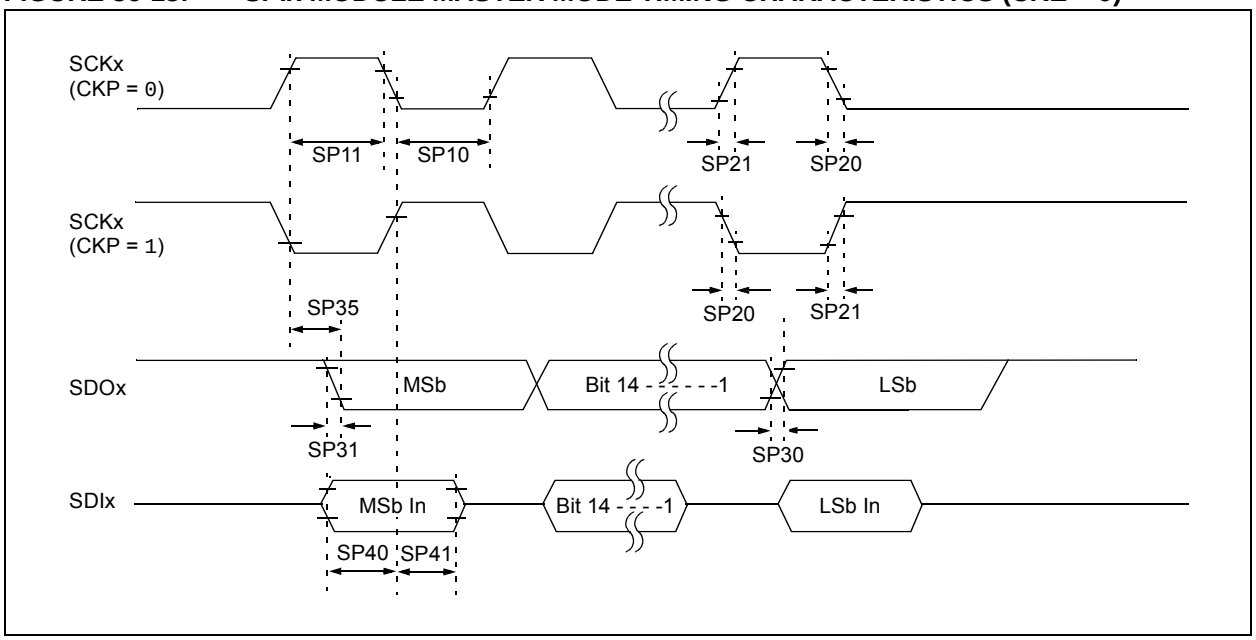



**TABLE 36-34: SPIx MASTER MODE TIMING REQUIREMENTS (CKE = 0)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| SP10 | TscL | SCKx Output Low Time(2) | TCY/2 | — | — | ns | |
| SP11 | TscH | SCKx Output High Time(2) | TCY/2 | — | — | ns | |
| SP20 | TscF | SCKx Output Fall Time(3) | — | 10 | 25 | ns | |
| SP21 | TscR | SCKx Output Rise Time(3) | — | 10 | 25 | ns | |
| SP30 | TdoF | SDOx Data Output Fall Time(3) | — | 10 | 25 | ns | |
| SP31 | TdoR | SDOx Data Output Rise Time(3) | — | 10 | 25 | ns | |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid After SCKx Edge | — | — | 30 | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 20 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 20 | — | — | ns | |

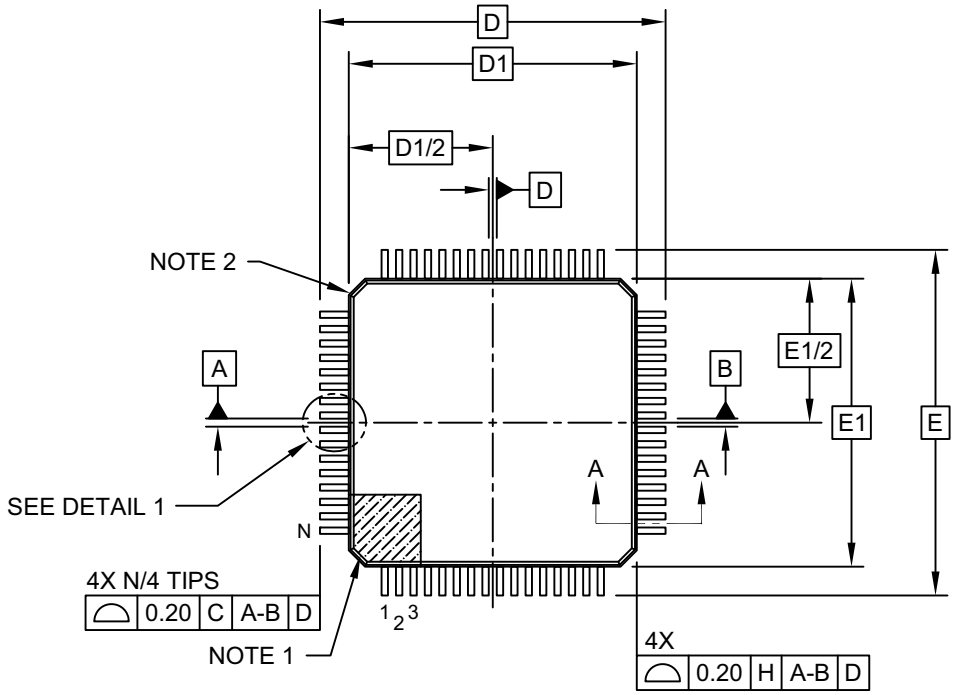
**Note 1:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** The minimum clock period for SCKx is 100 ns; therefore, the clock generated in Master mode must not violate this specification.

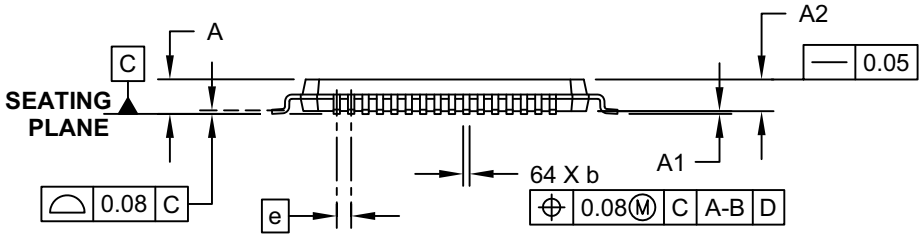
**3:** Assumes 50 pF load on all SPIx pins.

**64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]**

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




TOP VIEW




SIDE VIEW

Microchip Technology Drawing C04-085C Sheet 1 of 2