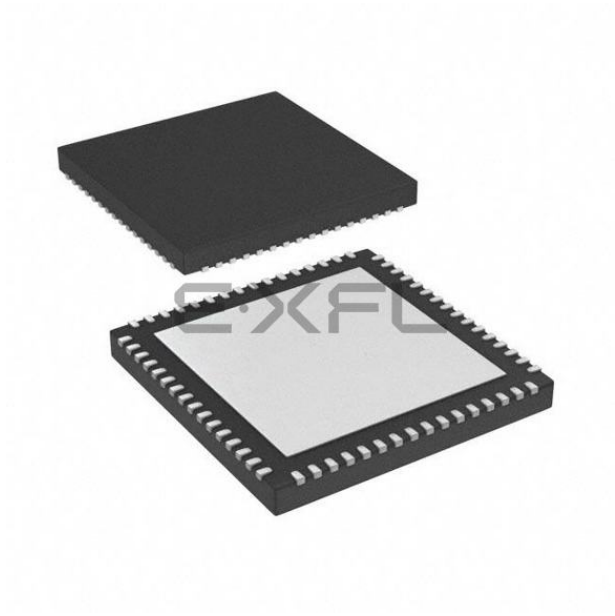

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256ga406-i-mr

2.4 Voltage Regulator Pin (VCAP)

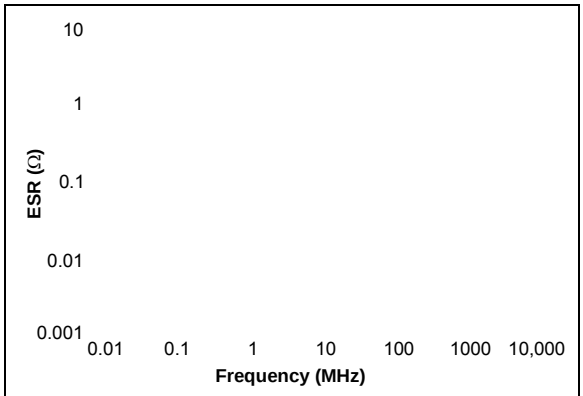
A low-ESR (< 5Ω) capacitor is required on the VCAP pin to stabilize the output voltage of the on-chip voltage regulator. The VCAP pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specification can be used.

The placement of this capacitor should be close to VCAP. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 36.0 "Electrical Characteristics"** for additional information.

Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

Refer to **Section 33.2 "On-Chip Voltage Regulator"** for details on connecting and using the on-chip regulator.

FIGURE 2-3: FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at +25°C, 0V DC bias.

TABLE 2-1: SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to +125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to +85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to +125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to +85ºC
Murata	GRM32DR71C106KA01L	10 µF	±10%	16V	-55 to +125ºC
Murata	GRM31CR61C106KC31L	10 µF	±10%	16V	-55 to +85ºC

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface-mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

Typical low-cost, 10 μF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R), or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

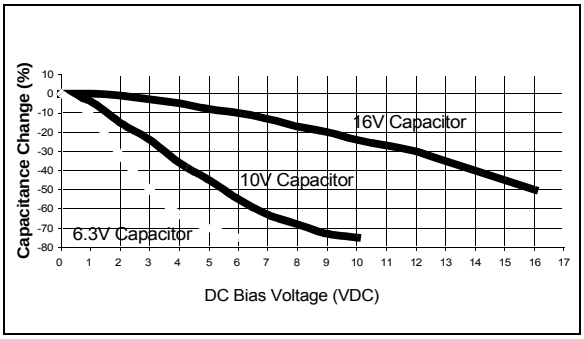
The X5R and X7R capacitors typically exhibit satisfactory temperature stability (i.e., ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 μF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

Typical DC bias voltage vs. capacitance graph for X7R type capacitors is shown in Figure 2-4.

When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 2.5V or 1.8V core voltage. Suggested capacitors are shown in Table 2-1.

FIGURE 2-4: DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming (ICSP) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

For device emulation, ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins), programmed into the device, matches the physical connections for the ICSP to the Microchip debugger/emulator tool.

The $\overline{MCLR}$ connection from the ICSP header should connect directly to the $\overline{MCLR}$ pin on the device. A capacitor to ground (C1 in Figure 2-2) is optional, but if used, may interfere with ICSP operation if the value exceeds 0.01 μF. In most cases, this capacitor is not required.

For more information on available Microchip development tools connection requirements, refer to **Section 34.0 "Development Support"**.

TABLE 4-12: SFR BLOCK 700h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
I/O (Continued)			AD1CON1	746	0000000000000000	RPINR13	7AA	0011111100111111
PORTJ	700	0000000000000000	AD1CON2	748	0000000000000000	RPINR14	7AC	0011111100111111
LATJ	702	0000000000000000	AD1CON3	74A	0000000000000000	RPINR15	7AE	0011111100111111
ODCJ	704	0000000000000000	AD1CHS	74C	0000000000000000	RPINR16	7B0	0011111100111111
IOCPJ	708	0000000000000000	AD1CSSL	74E	0000000000000000	RPINR17	7B2	0011111100111111
IOCNJ	70A	0000000000000000	AD1CSSH	750	0000000000000000	RPINR18	7B4	0011111100111111
IOCFJ	70C	0000000000000000	AD1CON4	752	0000000000000000	RPINR19	7B6	0011111100111111
IOCPUJ	70E	0000000000000000	AD1CON5	754	0000000000000000	RPINR20	7B8	0011111100111111
IOCPDJ	710	0000000000000000	AD1CHITL	756	0000000000000000	RPINR21	7BA	0011111100111111
A/D			AD1CHITH	758	0000000000000000	RPINR22	7BC	0011111100111111
AD1BUF0	712	xxxxxxxxxxxxxxxx	ADC1CTMENL	75A	0000000000000000	RPINR23	7BE	0011111100111111
AD1BUF1	714	xxxxxxxxxxxxxxxx	ADC1CTMENH	75C	0000000000000000	RPINR24	7C0	0011111100111111
AD1BUF2	716	xxxxxxxxxxxxxxxx	ADC1RESDMA	75E	0000000000000000	RPINR25	7C2	0011111100111111
AD1BUF3	718	xxxxxxxxxxxxxxxx	**NVM Controller**			RPINR26	7C4	0011111100111111
AD1BUF4	71A	xxxxxxxxxxxxxxxx	NVMCON	760	0000000000000000(1)	RPINR27	7C6	0011111100111111
AD1BUF5	71C	xxxxxxxxxxxxxxxx	NVMADRL	762	0000000000000000	RPINR28	7C8	0011111100111111
AD1BUF6	71E	xxxxxxxxxxxxxxxx	NVMADRH	764	0000000000000000	RPINR29	7CA	0011111100111111
AD1BUF7	720	xxxxxxxxxxxxxxxx	NVMKEY	766	0000000000000000	RPINR30	7CC	0011111100111111
AD1BUF8	722	xxxxxxxxxxxxxxxx	NVMSRCADRL	768	0000000000000000	RPINR31	7CE	0011111100111111
AD1BUF9	724	xxxxxxxxxxxxxxxx	NVMSRCADRH	76A	0000000000000000	RPOR0	7D4	0000000000000000
AD1BUF10	726	xxxxxxxxxxxxxxxx	JDATAL	77C	xxxxxxxxxxxxxxxx	RPOR1	7D6	0000000000000000
AD1BUF11	728	xxxxxxxxxxxxxxxx	JDATAH	77E	xxxxxxxxxxxxxxxx	RPOR2	7D8	0000000000000000
AD1BUF12	72A	xxxxxxxxxxxxxxxx	**Peripheral Pin Select**			RPOR3	7DA	0000000000000000
AD1BUF13	72C	xxxxxxxxxxxxxxxx	RPINR0	790	0011111100111111	RPOR4	7DC	0000000000000000
AD1BUF14	72E	xxxxxxxxxxxxxxxx	RPINR1	792	0011111100111111	RPOR5	7DE	0000000000000000
AD1BUF15	730	xxxxxxxxxxxxxxxx	RPINR2	794	0011111100111111	RPOR6	7E0	0000000000000000
AD1BUF16	732	xxxxxxxxxxxxxxxx	RPINR3	796	0011111100111111	RPOR7	7E2	0000000000000000
AD1BUF17	734	xxxxxxxxxxxxxxxx	RPINR4	798	0011111100111111	RPOR8	7E4	0000000000000000
AD1BUF18	736	xxxxxxxxxxxxxxxx	RPINR5	79A	0011111100111111	RPOR9	7E6	0000000000000000
AD1BUF19	738	xxxxxxxxxxxxxxxx	RPINR6	79C	0011111100111111	RPOR10	7E8	0000000000000000
AD1BUF20	73A	xxxxxxxxxxxxxxxx	RPINR7	7A2	0011111100111111	RPOR11	7EA	0000000000000000
AD1BUF21	73C	xxxxxxxxxxxxxxxx	RPINR8	7A0	0011111100111111	RPOR12	7EC	0000000000000000
AD1BUF22	73E	xxxxxxxxxxxxxxxx	RPINR9	7A2	0011111100111111	RPOR13	7EE	0000000000000000
AD1BUF23	740	xxxxxxxxxxxxxxxx	RPINR10	7A4	0011111100111111	RPOR14	7F0	0000000000000000
AD1BUF24	742	xxxxxxxxxxxxxxxx	RPINR11	7A6	0011111100111111	RPOR15	7F2	0000000000000000
AD1BUF25	744	xxxxxxxxxxxxxxxx	RPINR12	7A8	0011111100111111			

Legend: x = unknown or indeterminate value. Reset and address values are in hexadecimal.

Note 1: The Reset value shown is for POR only. The value on other Reset states is dependent on the state of memory write/erase operations or partition swap at the time of Reset.

REGISTER 8-9: IFS3: INTERRUPT FLAG STATUS REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CCP1IF	RTCIF	DMA5IF	SPI3RXIF	SPI2RXIF	SPI1RXIF	SPI4RXIF	KEYSTRIF
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
CRYDNIF	INT4IF	INT3IF	—	CCT7IF	MI2C2IF	SI2C2IF	CCT6IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CCP1IF:** MCCP1 Capture/Compare Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 14 **RTCIF:** Real-Time Clock and Calendar Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13 **DMA5IF:** DMA Channel 5 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12 **SPI3RXIF:** SPI3 Receive Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 11 **SPI2RXIF:** SPI2 Receive Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 10 **SPI1RXIF:** SPI1 Receive Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 9 **SPI4RXIF:** SPI4 Receive Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 8 **KEYSTRIF:** Cryptographic Key Store Program Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 7 **CRYDNIF:** Cryptographic Operation Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6 **INT4IF:** External Interrupt 4 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5 **INT3IF:** External Interrupt 3 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4 **Unimplemented:** Read as '0'

bit 3 **CCT7IF:** SCCP7 Timer Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 8-26: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CNIP2	CNIP1	CNIP0	—	CMIP2	CMIP1	CMIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **CNIP<2:0>:** Input Change Notification Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **CMIP<2:0>:** Comparator Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **MI2C1IP<2:0>:** Master I2C1 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **SI2C1IP<2:0>:** Slave I2C1 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

A recommended code sequence for a clock switch includes the following:

1. Disable interrupts during the OSCCON register unlock and write sequence.
2. Execute the unlock sequence for the OSCCON high byte by writing 78h and 9Ah to OSCCON<15:8> in two back-to-back instructions.
3. Write the new oscillator source to the NOSCx bits in the instruction immediately following the unlock sequence.
4. Execute the unlock sequence for the OSCCON low byte by writing 46h and 57h to OSCCON<7:0> in two back-to-back instructions.
5. Set the OSWEN bit in the instruction immediately following the unlock sequence.
6. Continue to execute code that is not clock-sensitive (optional).
7. Invoke an appropriate amount of software delay (cycle counting) to allow the selected oscillator and/or PLL to start and stabilize.
8. Check to see if OSWEN is '0'. If it is, the switch was successful. If OSWEN is still set, then check the LOCK bit to determine the cause of the failure.

The core sequence for unlocking the OSCCON register and initiating a clock switch is shown in Example 9-1.

EXAMPLE 9-1: BASIC CODE SEQUENCE FOR CLOCK SWITCHING

```
;Place the new oscillator selection in W0
;OSCCONH (high byte) Unlock Sequence
MOV         #OSCCONH, w1
MOV         #0x78, w2
MOV         #0x9A, w3
MOV.b       w2, [w1]
MOV.b       w3, [w1]
;Set new oscillator selection
MOV.b       WREG, OSCCONH
;OSCCONL (low byte) unlock sequence
MOV         #OSCCONL, w1
MOV         #0x46, w2
MOV         #0x57, w3
MOV.b       w2, [w1]
MOV.b       w3, [w1]
;Start oscillator switch operation
BSET        OSCCON,#0
```

9.5 FRC Active Clock Tuning

PIC24FJ256GA412/GB412 family devices include an automatic mechanism to calibrate the FRC during run time. This system uses active clock tuning from a source of known accuracy to maintain the FRC within a very narrow margin of its nominal 8 MHz frequency. This allows for a frequency accuracy that is well within the requirements of the *"USB 2.0 Specification"*, regarding full-speed USB devices.

Note:	The self-tune feature maintains sufficient accuracy for operation in USB Device mode. For applications that function as a USB host, a high-accuracy clock source (±0.05%) is still required.

The self-tune system is controlled by the bits in the upper half of the OSCTUN register. Setting the STEN bit (OSCTUN<15>) enables the self-tuning feature, allowing the hardware to calibrate to a source selected by the STSRC bit (OSCTUN<12>). When STSRC = 1, the system uses the Start-of-Frame (SOF) packets from an external USB host for its source. When STSRC = 0, the system uses the crystal-controlled SOSC for its calibration source. Regardless of the source, the system uses the TUN<5:0> bits (OSCTUN<5:0>) to change the FRC Oscillator's frequency. Frequency monitoring and adjustment is dynamic, occurring continuously during run time. While the system is active, the TUNx bits cannot be written to by software.

Note:	To use the USB as a reference clock tuning source (STSRC = 1), the microcontroller must be configured for USB device operation and connected to a non-suspended USB host or hub port. If the SOSC is to be used as the reference clock tuning source (STSRC = 0), the SOSC must also be enabled for clock tuning to occur.

The self-tune system can generate a hardware interrupt, FSTIF. The interrupt can result from a drift of the FRC from the reference by greater than 0.2%, in either direction, or whenever the frequency deviation is beyond the ability of the TUNx bits to correct (i.e., greater than 1.5%). The STLOCK and STOR status bits (OSCTUN<11,9>) are used to indicate these conditions.

The STLPOL and STORPOL bits (OSCTUN<10,8>) configure the FSTIF interrupt to occur in the presence or the absence of the conditions. It is the user's responsibility to monitor both the STLOCK and STOR bits to determine the exact cause of the interrupt.

Note:	The STLPOL and STORPOL bits should be ignored when the self-tune system is disabled (STEN = 0).

TABLE 10-2: EXITING POWER-SAVING MODES

Mode	Exit Conditions								Code Execution Resumes
	Interrupts		Resets			RTCC Alarm	WDT	VDD Restore(2)	
	All	INT0	All	POR	$\overline{MCLR}$				
Idle	Y	Y	Y	Y	Y	Y	Y	N/A	Next instruction
Sleep (all modes)	Y	Y	Y	Y	Y	Y	Y	N/A	
Deep Sleep	N	Y	N	Y	Y	Y	Y(1)	N/A	Reset vector
VBAT	N	N	N	N	N	N	N	Y	Reset vector

Note 1: Deep Sleep WDT.

2: A POR or POR-like Reset results whenever VDD is removed and restored in any mode.

10.1.1 INSTRUCTION-BASED POWER-SAVING MODES

Three of the power-saving modes are entered through the execution of the PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. Deep Sleep mode stops clock operation, code execution and all peripherals, except RTCC and DSWDT. It also freezes I/O states and removes power to Flash memory, and may remove power to SRAM.

The assembly syntax of the PWRSAV instruction is shown in Example 10-1. Sleep and Idle modes are entered directly with a single assembler command. Deep Sleep requires an additional sequence to unlock and enable the entry into Deep Sleep, which is described in **Section 10.4.1 "Entering Deep Sleep Mode"**.

Note:	SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

The features enabled with the low-voltage/retention regulator result in some changes to the way that Sleep and Deep Sleep modes behave. See **Section 10.3 "Sleep Mode"** and **Section 10.4 "Deep Sleep Mode"** for additional information.

10.1.1.1 Interrupts Coincident with Power Save Instructions

Any interrupt that coincides with the execution of a PWRSAV instruction will be held off until entry into Sleep or Idle mode has completed. The device will then wake-up from Sleep or Idle mode.

For Deep Sleep mode, interrupts that coincide with the execution of the PWRSAV instruction may be lost. The microcontroller resets on leaving Deep Sleep and the interrupt will be lost.

Interrupts that occur during the Deep Sleep unlock sequence will interrupt the mandatory five-instruction cycle sequence timing and cause a failure to enter Deep Sleep. For this reason, it is recommended to disable all interrupts during the Deep Sleep unlock sequence.

EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

```
// Syntax to enter Sleep mode:
PWRSAV     #SLEEP_MODE        ; Put the device into SLEEP mode
//
//Synatx to enter Idle mode:
PWRSAV     #IDLE_MODE         ; Put the device into IDLE mode
//
// Syntax to enter Deep Sleep mode:
// First use the unlock sequence to set the DSEN bit (see Example 10-2)
BSET       DSCON, #DSEN       ; Enable Deep Sleep
BSET       DSCON, #DSEN       ; Enable Deep Sleep(repeat the command)
PWRSAV     #SLEEP_MODE        ; Put the device into Deep SLEEP mode
```

TABLE 11-4: PORTC REGISTER MAP(1)

Register Name	Bit Range	Bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANSC	15:0	—	—	—	—	—	—	—	—	—	—	—	ANSC<4:1>				—
TRISC	15:0	TRISC15	—	—	TRISC12	—	—	—	—	—	—	—	TRISC<4:1>				—
PORTC	15:0	PORTC<15:12>				—	—	—	—	—	—	—	PORTC<4:1>				—
LATC	15:0	LATC15	—	—	LATC12	—	—	—	—	—	—	—	LATC<4:1>				—
ODCC	15:0	ODCC15	—	—	ODCC12	—	—	—	—	—	—	—	ODCC<4:1>				—
IOCPC	15:0	IOCPC<15:12>				—	—	—	—	—	—	—	IOCPC<4:1>				—
IOCNC	15:0	IOCNC<15:12>				—	—	—	—	—	—	—	IOCNC<4:1>				—
IOCFC	15:0	IOCFC<15:12>				—	—	—	—	—	—	—	IOCFC<4:1>				—
IOCPUC	15:0	IOCPUC<15:12>				—	—	—	—	—	—	—	IOCPUC<4:1>				—
IOCPDC	15:0	IOCPDC<15:12>				—	—	—	—	—	—	—	IOCPDC<4:1>				—

Legend: — = unimplemented, read as '0'.

Note 1: PORT register maps show full pin count devices. Please refer to Table 1-4 and Table 1-5 for pin count-specific PORT I/O implementation.

TABLE 11-5: PORTD REGISTER MAP(1)

Register Name	Bit Range	Bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANSD	15:0	ANSD<15:0>															
TRISD	15:0	TRISD<15:0>															
PORTD	15:0	PORTD<15:0>															
LATD	15:0	LATD<15:0>															
ODCD	15:0	ODCD<15:0>															
IOCPD	15:0	IOCPD<15:0>															
IOCND	15:0	IOCND<15:0>															
IOCFD	15:0	IOCFD<15:0>															
IOCPUD	15:0	IOCPUD<15:0>															
IOCPDD	15:0	IOCPDD<15:0>															

Legend: — = unimplemented, read as '0'.

Note 1: PORT register maps show full pin count devices. Please refer to Table 1-4 and Table 1-5 for pin count-specific PORT I/O implementation.

REGISTER 11-27: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP9R5	RP9R4	RP9R3	RP9R2	RP9R1	RP9R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP8R5	RP8R4	RP8R3	RP8R2	RP8R1	RP8R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP9R<5:0>:** RP9 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP9 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP8R<5:0>:** RP8 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP8 (see Table 11-12 for peripheral function numbers).

REGISTER 11-28: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP11R5	RP11R4	RP11R3	RP11R2	RP11R1	RP11R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP10R5	RP10R4	RP10R3	RP10R2	RP10R1	RP10R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP11R<5:0>:** RP11 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP11 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP10R<5:0>:** RP10 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP10 (see Table 11-12 for peripheral function numbers).

REGISTER 13-2: TyCON: TIMER3 AND TIMER5 CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
TON(2)	—	TSIDL(2)	—	—	—	TECS1(2,3)	TECS0(2,3)
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE(2)	TCKPS1(2)	TCKPS0(2)	—	—	TCS(2,3)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timery On bit(2)
1 = Starts 16-bit Timery
0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timery Stop in Idle Mode bit(2)
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9-8 **TECS<1:0>:** Timery Extended Clock Source Select bits (selected when TCS = 1)(2,3)
11 = Generic Timer (TMRCK) external input
10 = LPRC Oscillator
01 = TxCK external clock input
00 = SOSC

bit 7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit(2)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timery Input Clock Prescale Select bits(2)
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timery Clock Source Select bit(2,3)
1 = External clock from pin, TyCK (on the rising edge)
0 = Internal clock (FOSC/2)

bit 0 **Unimplemented:** Read as '0'

Note 1: Changing the value of TyCON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

2: When 32-bit operation is enabled (T2CON<3> or T4CON<3> = 1), these bits have no effect on Timery operation; all timer functions are set through T2CON and T4CON.

3: If TCS = 1 and TECS<1:0> = x1, the selected external timer input (TyCK) must be configured to an available RPn/RPIn pin. For more information, see **Section 11.5 "Peripheral Pin Select (PPS)"**.

14.3 Output Compare Mode

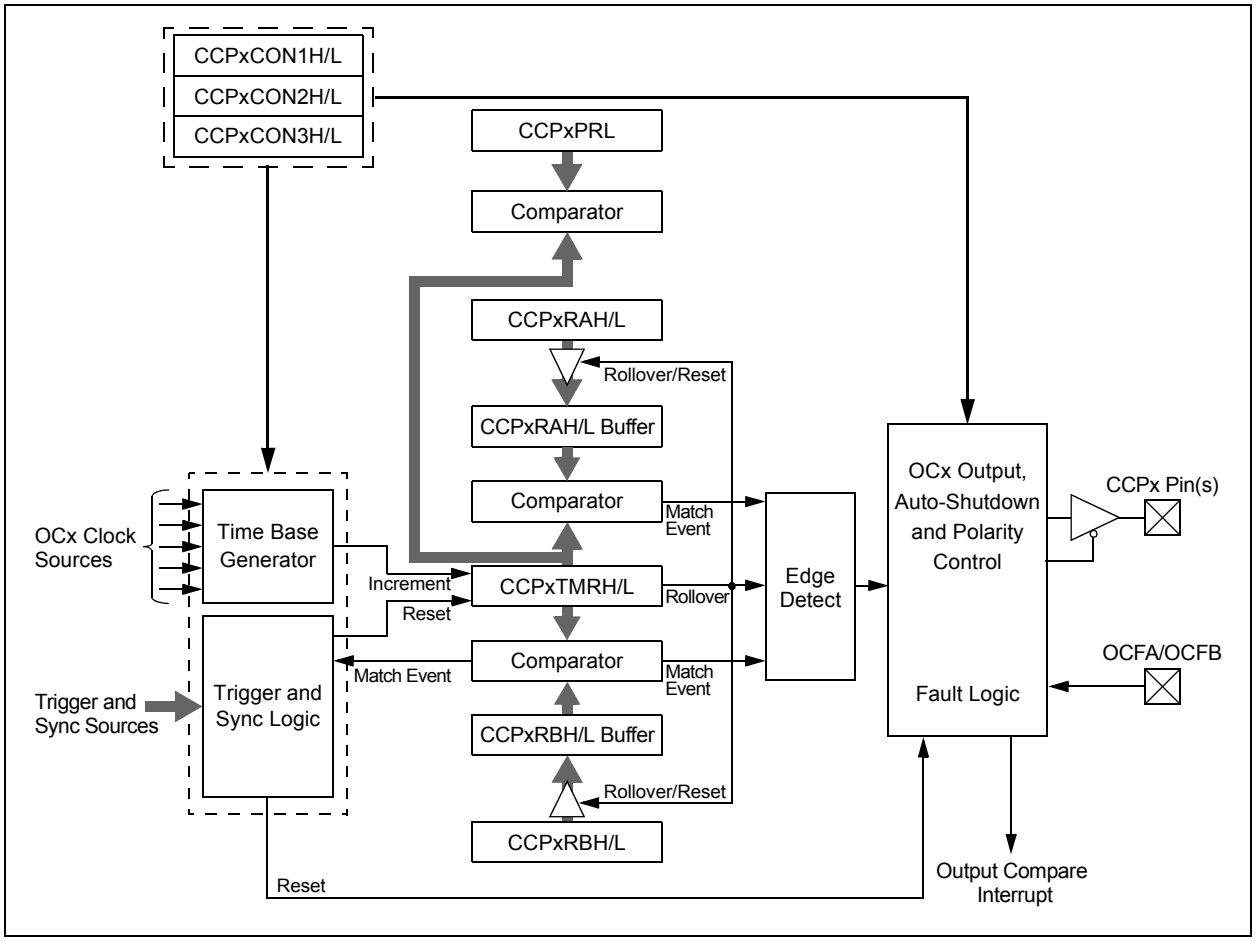
Output Compare mode compares the Timer register value with the value of one or two Compare registers, depending on its mode of operation. The Output Compare x module, on compare match events, has the ability to generate a single output transition or a train of output pulses. Like most PIC® MCU peripherals, the Output Compare x module can also generate interrupts on a compare match event.

Table 14-2 shows the various modes available in Output Compare modes.

TABLE 14-2: OUTPUT COMPARE/PWM MODES

MOD<3:0> (CCPxCON1L<3:0>)	T32 (CCPxCON1L<5>)	Operating Mode	
0001	0	Output High on Compare (16-bit)	Single Edge Mode
0001	1	Output High on Compare (32-bit)	
0010	0	Output Low on Compare (16-bit)	
0010	1	Output Low on Compare (32-bit)	
0011	0	Output Toggle on Compare (16-bit)	
0011	1	Output Toggle on Compare (32-bit)	
0100	0	Dual Edge Compare (16-bit)	Dual Edge Mode
0101	0	Dual Edge Compare (16-bit buffered)	PWM Mode
0110	0	Center-Aligned Pulse (16-bit buffered)	Center PWM
0111	0	Variable Frequency Pulse (16-bit)	
0111	1	Variable Frequency Pulse (32-bit)	

FIGURE 14-5: OUTPUT COMPARE x BLOCK DIAGRAM



14.4 Input Capture Mode

Input Capture mode is used to capture a timer value from an independent timer base upon an event on an input pin or other internal trigger source. The input capture features are useful in applications requiring frequency (time period) and pulse measurement. Figure 14-6 depicts a simplified block diagram of Input Capture mode.

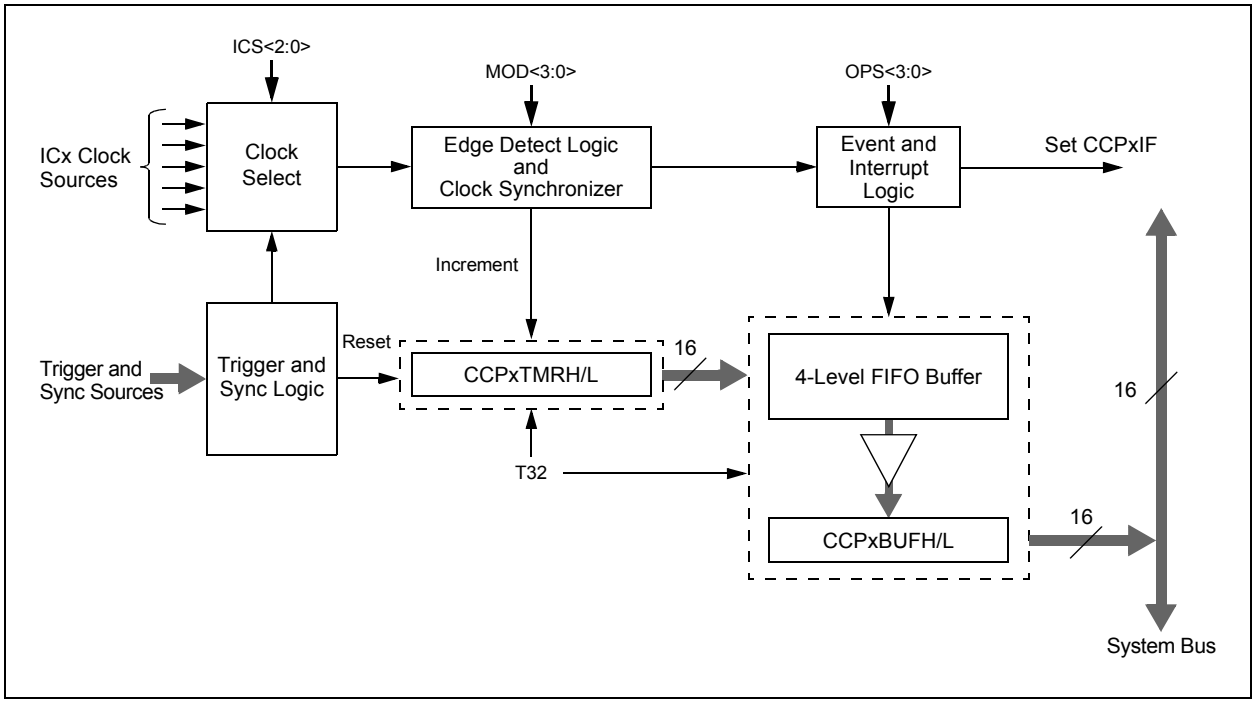
Input Capture mode uses a dedicated 16/32-bit, synchronous, up counting timer for the capture function. The timer value is written to the FIFO when a capture event occurs. The internal value may be read (with a synchronization delay) using the CCPxTMRH/L register.

To use Input Capture mode, the CCSEL bit (CCPxCON1L<4>) must be set. The T32 and the MOD<3:0> bits are used to select the proper Capture mode, as shown in Table 14-3.

TABLE 14-3: INPUT CAPTURE MODES

MOD<3:0> (CCPxCON1L<3:0>)	T32 (CCPxCON1L<5>)	Operating Mode
0000	0	Edge Detect (16-bit capture)
0000	1	Edge Detect (32-bit capture)
0001	0	Every Rising (16-bit capture)
0001	1	Every Rising (32-bit capture)
0010	0	Every Falling (16-bit capture)
0010	1	Every Falling (32-bit capture)
0011	0	Every Rise/Fall (16-bit capture)
0011	1	Every Rise/Fall (32-bit capture)
0100	0	Every 4th Rising (16-bit capture)
0100	1	Every 4th Rising (32-bit capture)
0101	0	Every 16th Rising (16-bit capture)
0101	1	Every 16th Rising (32-bit capture)

FIGURE 14-6: INPUT CAPTURE x BLOCK DIAGRAM



REGISTER 21-2: PMCON2: EPMP CONTROL REGISTER 2

R-0, HSC	U-0	R/C-0, HS	R/C-0, HS	U-0	U-0	U-0	U-0
BUSY	—	ERROR	TIMEOUT	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RADDR23(1)	RADDR22(1)	RADDR21(1)	RADDR20(1)	RADDR19(1)	RADDR18(1)	RADDR17(1)	RADDR16(1)
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	HS = Hardware Settable bit

bit 15 **BUSY:** Busy bit (Master mode only)
1 = Port is busy
0 = Port is not busy

bit 14 **Unimplemented:** Read as '0'

bit 13 **ERROR:** Error bit
1 = Transaction error (illegal transaction was requested)
0 = Transaction completed successfully

bit 12 **TIMEOUT:** Time-out bit
1 = Transaction timed out
0 = Transaction completed successfully

bit 11-8 **Unimplemented:** Read as '0'

bit 7-0 **RADDR<23:16>:** Parallel Master Port Reserved Address Space bits(1)

Note 1: If RADDR<23:16> = 00000000, then the last EDS address for Chip Select 2 will be FFFFFFh.

REGISTER 23-1: CLCxCONL: CLCx CONTROL REGISTER (LOW) (CONTINUED)

bit 2-0 **MODE<2:0>:** CLCx Mode bits
111 = Single input transparent latch with S and R
110 = JK flip-flop with R
101 = Two-input D flip-flop with R
100 = Single input D flip-flop with S and R
011 = SR latch
010 = Four-input AND
001 = Four-input OR-XOR
000 = Four-input AND-OR

REGISTER 23-2: CLCxCONH: CLCx CONTROL REGISTER (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	G4POL	G3POL	G2POL	G1POL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **G4POL:** Gate 4 Polarity Control bit
1 = Channel 4 logic output is inverted when applied to the logic cell
0 = Channel 4 logic output is not inverted

bit 2 **G3POL:** Gate 3 Polarity Control bit
1 = Channel 3 logic output is inverted when applied to the logic cell
0 = Channel 3 logic output is not inverted

bit 1 **G2POL:** Gate 2 Polarity Control bit
1 = Channel 2 logic output is inverted when applied to the logic cell
0 = Channel 2 logic output is not inverted

bit 0 **G1POL:** Gate 1 Polarity Control bit
1 = Channel 1 logic output is inverted when applied to the logic cell
0 = Channel 1 logic output is not inverted

24.5.4 DATE/ALARM/TIMESTAMP VALUE REGISTERS

REGISTER 24-9: DATEL/ALMDATEL/TSADATEL/TSBDATEL: DATE REGISTER (LOW)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-0
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-12 **DAYTEN<1:0>:** Binary Coded Decimal Value of Days ‘10’ Digit bits
Contains a value from 0 to 3.

bit 11-8 **DAYONE<3:0>:** Binary Coded Decimal Value of Days ‘1’ Digit bits
Contains a value from 0 to 9.

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekdays ‘1’ Digit bits
Contains a value from 0 to 6.

REGISTER 24-10: DATEH/ALMDATEH/TSADATEH/TSBDATEH: DATE REGISTER (HIGH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	—	MTHTEN	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **YRTEN<3:0>:** Binary Coded Decimal Value of Years ‘10’ Digit bits

bit 11-8 **YRONE<3:0>:** Binary Coded Decimal Value of Years ‘1’ Digit bits

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **MTHTEN:** Binary Coded Decimal Value of Months ‘10’ Digit bit
Contains a value from 0 to 1.

bit 3-0 **MTHONE<3:0>:** Binary Coded Decimal Value of Months ‘1’ Digit bits
Contains a value from 0 to 9.

REGISTER 27-2: AD1CON2: A/D CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	r-0	R/W-0	R/W-0	U-0	U-0
PVCFG1	PVCFG0	NVCFG0	—	BUFREGEN	CSCNA	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS(1)	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM(1)	ALTS
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **PVCFG<1:0>:** A/D Converter Positive Voltage Reference Configuration bits
1x = Unimplemented, do not use
01 = External VREF+
00 = AVDD

bit 13 **NVCFG0:** A/D Converter Negative Voltage Reference Configuration bit
1 = External VREF-
0 = AVSS

bit 12 **Reserved:** Maintain as '0'

bit 11 **BUFREGEN:** A/D Buffer Register Enable bit
1 = Conversion result is loaded into the buffer location determined by the converted channel
0 = A/D result buffer is treated as a FIFO

bit 10 **CSCNA:** Scan Input Selections for CH0+ During Sample A bit
1 = Scans inputs
0 = Does not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit(1)
1 = A/D is currently filling ADC1BUF13-ADC1BUF25, user should access data in ADC1BUF0-ADC1BUF12
0 = A/D is currently filling ADC1BUF0-ADC1BUF12, user should access data in ADC1BUF13-ADC1BUF25

bit 6-2 **SMPI<4:0>:** Interrupt Sample/DMA Increment Rate Select bits
When DMAEN = 1:
11111 = Increments the DMA address after completion of the 32nd sample/conversion operation
11110 = Increments the DMA address after completion of the 31st sample/conversion operation
• • •
00001 = Increments the DMA address after completion of the 2nd sample/conversion operation
00000 = Increments the DMA address after completion of each sample/conversion operation
When DMAEN = 0:
11111 = Interrupts at the completion of the conversion for each 32nd sample
11110 = Interrupts at the completion of the conversion for each 31st sample
• • •
00001 = Interrupts at the completion of the conversion for every other sample
00000 = Interrupts at the completion of the conversion for each sample

Note 1: These bits are only applicable when the buffer is used in FIFO mode (BUFREGEN = 0). In addition, BUFS is only used when BUFM = 1.

TABLE 36-6: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Operating Temperature**	**VDD**	**Conditions**
Power-Down Current (IPD)						
DC60	3.24	—	µA	-40°C	2.0V	Sleep(2)
	4.08	22	µA	+25°C		
	7.81	—	µA	+60°C		
	23.25	40	µA	+85°C		
	3.20	—	µA	-40°C	3.3V	
	4.07	25	µA	+25°C		
	7.94	—	µA	+60°C		
	19.85	42	µA	+85°C		
DC61	0.07	—	µA	-40°C	2.0V	Low-Voltage Sleep(3)
	0.07	—	µA	+25°C		
	3.54	—	µA	+60°C		
	15.30	—	µA	+85°C		
	0.10	—	µA	-40°C	3.3V	
	0.06	—	µA	+25°C		
	3.68	—	µA	+60°C		
	15.65	—	µA	+85°C		
DC70	120	—	nA	-40°C	2.0V	Deep Sleep, capacitor on VCAP is fully discharged
	80	800	nA	+25°C		
	620	—	nA	+60°C		
	1.13	5	µA	+85°C		
	110	—	nA	-40°C	3.3V	
	110	1500	nA	+25°C		
	830	—	nA	+60°C		
	3.67	10	µA	+85°C		
DC74	0.6	3	µA	-40°C to +85°C	0V	RTCC with VBAT mode (LPRC/SOSC)(4)

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The low-voltage/retention regulator is disabled; RETEN (RCON<12>) = 0, $\overline{\text{LPCFG}}$ (FPOR<2>) = 1.

3: The low-voltage/retention regulator is enabled; RETEN (RCON<12>) = 1, $\overline{\text{LPCFG}}$ (FPOR<2>) = 0.

4: The VBAT pin is connected to the battery and RTCC is running with VDD = 0.

FIGURE 36-8: PWMx MODULE TIMING REQUIREMENTS

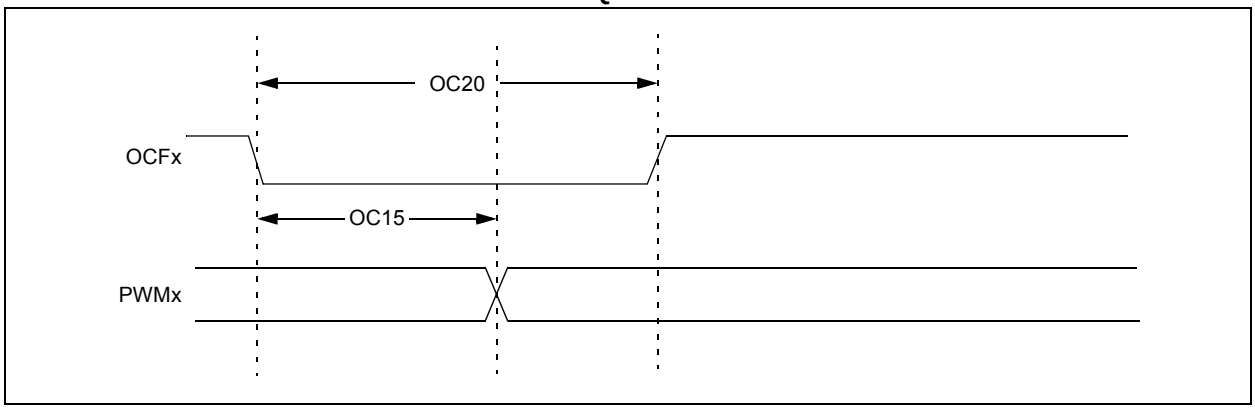


TABLE 36-29: PWMx TIMING REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Typ(1)	Max	Unit	Condition
OC15	TFD	Fault Input to PWM I/O Change	—	—	25	ns	VDD = 3.0V, -40°C to +85°C
OC20	TFH	Fault Input Pulse Width	50	—	—	ns	VDD = 3.0V, -40°C to +85°C

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 36-13: SPIx MODULE MASTER MODE TIMING CHARACTERISTICS (CKE = 0)

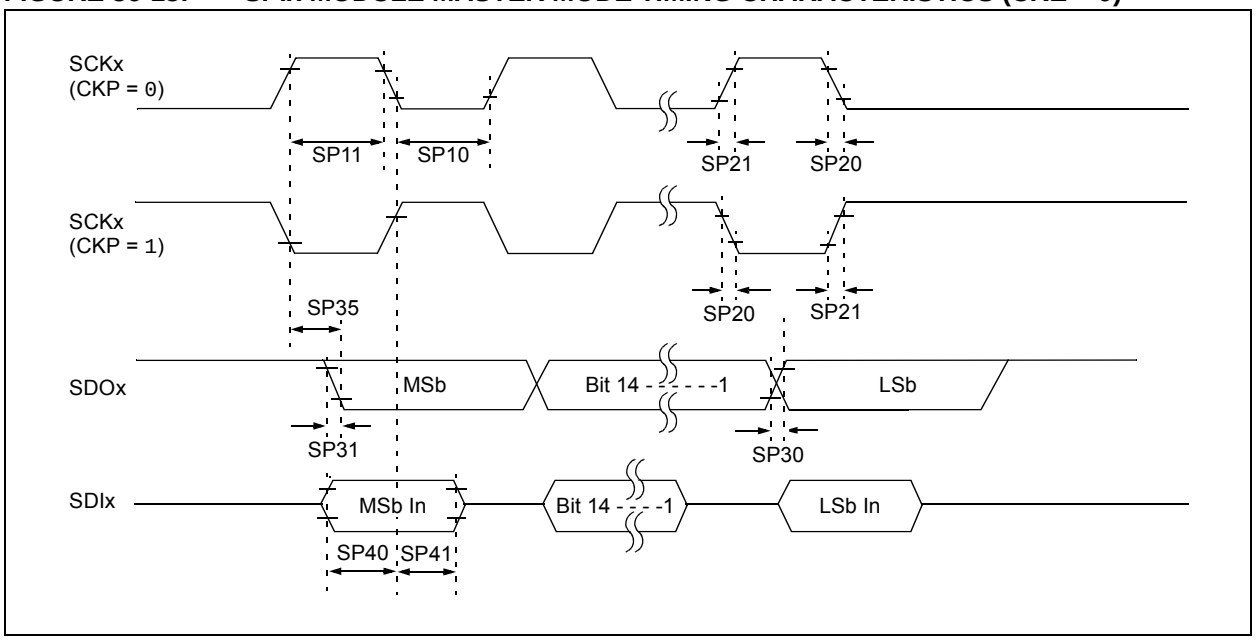


TABLE 36-34: SPIx MASTER MODE TIMING REQUIREMENTS (CKE = 0)

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
SP10	TscL	SCKx Output Low Time(2)	TCY/2	—	—	ns	
SP11	TscH	SCKx Output High Time(2)	TCY/2	—	—	ns	
SP20	TscF	SCKx Output Fall Time(3)	—	10	25	ns	
SP21	TscR	SCKx Output Rise Time(3)	—	10	25	ns	
SP30	TdoF	SDOx Data Output Fall Time(3)	—	10	25	ns	
SP31	TdoR	SDOx Data Output Rise Time(3)	—	10	25	ns	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	—	30	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	—	—	ns	

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The minimum clock period for SCKx is 100 ns; therefore, the clock generated in Master mode must not violate this specification.

3: Assumes 50 pF load on all SPIx pins.