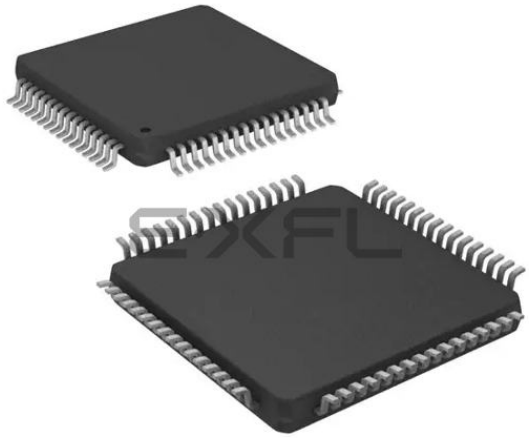

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256ga406-i-pt

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
PMACK1	50	77	A10	I	ST/TTL	Parallel Master Port Acknowledge Input 1
PMACK2	43	69	E10	I	ST/TTL	Parallel Master Port Acknowledge Input 2
PMBE0	51	78	B9	O	DIG	Parallel Master Port Byte Enable 0 Strobe
PMBE1	—	67	E8	O	DIG	Parallel Master Port Byte Enable 1 Strobe
PMCS1	—	18	G1	O	DIG	Parallel Master Port Chip Select 1 Strobe
PMCS2	—	9	E1	O	DIG	Parallel Master Port Chip Select 2 Strobe
PMD0	60	93	E12	I/O	DIG/ST/TTL	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMD1	61	94	E15	I/O	DIG/ST/TTL	
PMD2	62	98	E19	I/O	DIG/ST/TTL	
PMD3	63	99	A2	I/O	DIG/ST/TTL	
PMD4	64	100	A1	I/O	DIG/ST/TTL	
PMD5	1	3	D3	I/O	DIG/ST/TTL	
PMD6	2	4	C1	I/O	DIG/ST/TTL	
PMD7	3	5	D2	I/O	DIG/ST/TTL	
PMD8	—	90	A5	I/O	DIG/ST/TTL	
PMD9	—	89	E6	I/O	DIG/ST/TTL	
PMD10	—	88	A6	I/O	DIG/ST/TTL	
PMD11	—	87	B6	I/O	DIG/ST/TTL	
PMD12	—	79	A9	I/O	DIG/ST/TTL	
PMD13	—	80	D8	I/O	DIG/ST/TTL	
PMD14	—	83	D7	I/O	DIG/ST/TTL	
PMD15	—	84	C7	I/O	DIG/ST/TTL	
PMRD/$\overline{\text{PMWR}}$	53	82	B8	I/O	DIG/ST/TTL	Parallel Master Port Read Strobe/Write Strobe
PMWR/PMENB	52	81	C8	I/O	DIG/ST/TTL	Parallel Master Port Write Strobe/Enable Strobe
PWRGT	21	32	K4	O	DIGMV	Real-Time Clock Power Control Output
PWRLCLK	48	74	B11	I	STMV	Real-Time Clock 50/60 Hz Clock Input
RA0	—	17	G3	I/O	DIG/ST	PORTA Digital I/Os
RA1	—	38	J6	I/O	DIG/ST	
RA2	—	58	H11	I/O	DIG/ST/TTL	
RA3	—	59	G10	I/O	DIG/ST/TTL	
RA4	—	60	G11	I/O	DIG/ST	
RA5	—	61	G9	I/O	DIG/ST	
RA6	—	91	E10	I/O	DIG/ST	
RA7	—	92	E11	I/O	DIG/ST	
RA9	—	28	L2	I/O	DIG/ST/TTL	
RA10	—	29	K3	I/O	DIG/ST	
RA14	—	66	E11	I/O	DIG/ST/TTL	
RA15	—	67	E8	I/O	DIG/ST/TTL	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
SEG0	4	10	E3	O	ANA	LCD Driver Segment Outputs
SEG1	8	14	F3	O	ANA	
SEG2	11	20	H1	O	ANA	
SEG3	12	21	H2	O	ANA	
SEG4	13	22	J1	O	ANA	
SEG5	14	23	J2	O	ANA	
SEG6	15	24	K1	O	ANA	
SEG7	16	25	K2	O	ANA	
SEG8	29	43	K7	O	ANA	
SEG9	30	44	L8	O	ANA	
SEG10	31	49	L10	O	ANA	
SEG11	32	50	L11	O	ANA	
SEG12	33	51	K10	O	ANA	
SEG13	42	68	E9	O	ANA	
SEG14	43	69	E10	O	ANA	
SEG15	44	70	D11	O	ANA	
SEG16	45	71	C11	O	ANA	
SEG17	46	72	D9	O	ANA	
SEG18	27	41	J7	O	ANA	
SEG19	28	42	L7	O	ANA	
SEG20	49	76	A11	O	ANA	
SEG21	50	77	A10	O	ANA	
SEG22	51	78	B9	O	ANA	
SEG23	52	81	C8	O	ANA	
SEG24	53	82	B8	O	ANA	
SEG25	54	83	D7	O	ANA	
SEG26	55	84	C7	O	ANA	
SEG27	58	87	B6	O	ANA	
SEG28	—	61	G9	O	ANA	
SEG29	23	34	H5	O	ANA	
SEG30	22	33	L4	O	ANA	
SEG31	21	32	K4	O	ANA	
SEG32	—	6	D1	O	ANA	
SEG33	—	8	E2	O	ANA	
SEG34	—	18	G1	O	ANA	
SEG35	—	19	G2	O	ANA	
SEG36	—	28	L2	O	ANA	
SEG37	—	29	K3	O	ANA	
SEG38	—	47	L9	O	ANA	
SEG39	—	48	K9	O	ANA	
SEG40	34	52	K11	O	ANA	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

REGISTER 8-7: IFS1: INTERRUPT FLAG STATUS REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CCP6IF	CCP5IF	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **U2TXIF:** UART2 Transmitter Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 14 **U2RXIF:** UART2 Receiver Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13 **INT2IF:** External Interrupt 2 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12 **T5IF:** Timer5 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 11 **T4IF:** Timer4 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 10 **OC4IF:** Output Compare Channel 4 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 9 **OC3IF:** Output Compare Channel 3 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 8 **DMA2IF:** DMA Channel 2 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 7 **CCP6IF:** SCCP6 Capture/Compare Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6 **CCP5IF:** SCCP5 Capture/Compare Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5 **Unimplemented:** Read as '0'

bit 4 **INT1IF:** External Interrupt 1 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **CNIF:** Interrupt-on-Change Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

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REGISTER 8-9: IFS3: INTERRUPT FLAG STATUS REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CCP1IF	RTCIF	DMA5IF	SPI3RXIF	SPI2RXIF	SPI1RXIF	SPI4RXIF	KEYSTRIF
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
CRYDNIF	INT4IF	INT3IF	—	CCT7IF	MI2C2IF	SI2C2IF	CCT6IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CCP1IF:** MCCP1 Capture/Compare Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 14 **RTCIF:** Real-Time Clock and Calendar Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13 **DMA5IF:** DMA Channel 5 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12 **SPI3RXIF:** SPI3 Receive Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 11 **SPI2RXIF:** SPI2 Receive Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 10 **SPI1RXIF:** SPI1 Receive Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 9 **SPI4RXIF:** SPI4 Receive Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 8 **KEYSTRIF:** Cryptographic Key Store Program Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 7 **CRYDNIF:** Cryptographic Operation Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6 **INT4IF:** External Interrupt 4 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5 **INT3IF:** External Interrupt 3 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4 **Unimplemented:** Read as '0'

bit 3 **CCT7IF:** SCCP7 Timer Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

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REGISTER 8-19: IEC5: INTERRUPT ENABLE CONTROL REGISTER 5 (CONTINUED)

bit 3 **U3TXIE:** UART3 Transmitter Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **U3RXIE:** UART3 Receiver Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **U3ERIE:** UART3 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **Unimplemented:** Read as '0'

REGISTER 8-42: IPC20: INTERRUPT PRIORITY CONTROL REGISTER 20

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U3TXIP2	U3TXIP1	U3TXIP0	—	U3RXIP2	U3RXIP1	U3RXIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	U3ERIP2	U3ERIP1	U3ERIP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **U3TXIP<2:0>:** UART3 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **U3RXIP<2:0>:** UART3 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **U3ERIP<2:0>:** UART3 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

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REGISTER 8-44: IPC22: INTERRUPT PRIORITY CONTROL REGISTER 22

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPI3TXIP2	SPI3TXIP1	SPI3TXIP0	—	SPI3IP2	SPI3IP1	SPI3IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U4TXIP2	U4TXIP1	U4TXIP0	—	U4RXIP2	U4RXIP1	U4RXIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **SPI3TXIP<2:0>:** SPI3 Transmit Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **SPI3IP<2:0>:** SPI3 General Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **U4TXIP<2:0>:** UART4 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **U4RXIP<2:0>:** UART4 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

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8.4 Interrupt Setup Procedures

8.4.1 INITIALIZATION

To configure an interrupt source:

1. Set the NSTDIS (INTCON1<15>) control bit if nested interrupts are not desired.
2. Select the user-assigned priority level for the interrupt source by writing the control bits in the appropriate IPCx register. The priority level will depend on the specific application and type of interrupt source. If multiple priority levels are not desired, the IPCx register control bits, for all enabled interrupt sources, may be programmed to the same non-zero value.

Note: At a device Reset, the IPCx registers are initialized such that all user interrupt sources are assigned to Priority Level 4.

3. Clear the interrupt flag status bit associated with the peripheral in the associated IFSx register.
4. Enable the interrupt source by setting the interrupt enable control bit associated with the source in the appropriate IECx register.

8.4.2 INTERRUPT SERVICE ROUTINE (ISR)

The method that is used to declare an Interrupt Service Routine (ISR) and initialize the IVT with the correct vector address will depend on the programming language (i.e., 'C' or assembler), and the language development toolsuite that is used to develop the application. In general, the user must clear the interrupt flag in the appropriate IFSx register for the source of the interrupt that the ISR handles; otherwise, the ISR will be re-entered immediately after exiting the routine. If the ISR is coded in assembly language, it must be terminated using a `RETFIE` instruction to unstack the saved PC value, SRL value and old CPU priority level.

8.4.3 TRAP SERVICE ROUTINE (TSR)

A Trap Service Routine (TSR) is coded like an ISR, except that the appropriate trap status flag in the INTCON1 register must be cleared to avoid re-entry into the TSR.

8.4.4 INTERRUPT DISABLE

All user interrupts can be disabled using the following procedure:

1. Push the current SR value onto the software stack using the `PUSH` instruction.
2. Force the CPU to Priority Level 7 by inclusive ORing the value, 0Eh, with SRL.

To enable user interrupts, the `POP` instruction may be used to restore the previous SR value.

Note that only user interrupts with a priority level of 7 or less can be disabled. Trap sources (Levels 8-15) cannot be disabled.

The `DISI` instruction provides a convenient way to disable interrupts of Priority Levels 1-6 for a fixed period of time. Level 7 interrupt sources are not disabled by the `DISI` instruction.

9.6 PLL Block

PIC24FJ256GA412/GB412 family devices include a versatile PLL block as part of the clock generation system. This allows for economical high-speed operation up to FOSCMAX (32 MHz) without the need of an external HS crystal for most applications. It also provides the option to generate a high-precision 48 MHz clock for USB operation, without regard for the system clock frequency. The PLL block is shown in Figure 9-2.

The PLL block has two separate branches:

- A Fixed PLL branch that multiplies the input clock frequency by a factor of 4, 6 or 8. The output frequency is provided as the system clock, as well as an input for the reference clock.
- A 96 MHz PLL that multiplies the input frequency to 96 MHz. The PLL is able to generate a system clock output of 4 MHz, 8 MHz, 16 MHz or 32 MHz. In USB devices, this branch also generates the 48 MHz full-speed USB clock. The 96 MHz output is provided directly as an input for the reference clock.

The PLL block uses either the Primary Oscillator or the FRC as its input source, as selected by the COSC<2:0> or NOSC<2:0> oscillator select bits. For both PLL branches, the minimum input frequency is 4 MHz. For the FRC, the only valid input options are 4 MHz or 8 MHz. The input from the Primary Oscillator can range from up to 48 MHz, in 4 MHz increments.

The fixed PLL multiplier is selected by the PLLMODE<3:0> Configuration bits. As it does not automatically sense the input frequency, the user must select a frequency that will not result in an output frequency greater than 32 MHz.

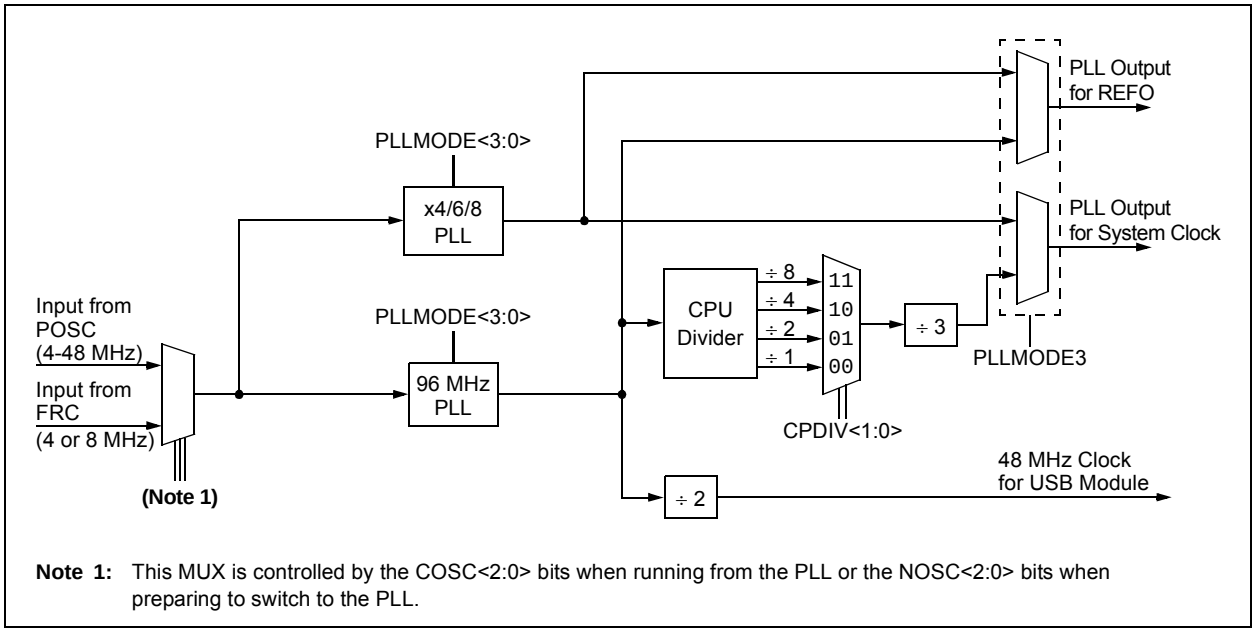
The 96 MHz PLL branch does not automatically sense the incoming oscillator frequency. The user must manually configure the PLL for the input frequency in order to generate the 96 MHz output, using the PLLMODE<3:0> Configuration bits. This limits the choices for input frequencies to a total of 8 possibilities, shown in Table 9-2. The CPDIV<1:0> bits independently select the system clock speed; available clock options are listed in Table 9-3.

TABLE 9-2: VALID OSCILLATOR INPUTS FOR 96 MHz PLL

Input Oscillator Frequency	Clock Mode	PLL Multiplier (PLLMODE<3:0>)
48 MHz	ECPLL	2 (0111)
32 MHz	HSPLL, ECPLL	3 (0110)
24 MHz	HSPLL, ECPLL	4 (0101)
20 MHz	HSPLL, ECPLL	4.8 (0100)
16 MHz	HSPLL, ECPLL	6 (0011)
12 MHz	HSPLL, ECPLL	8 (0010)
8 MHz	ECPLL, XTPLL, FRCPLL(1)	12 (0001)
4 MHz	ECPLL, XTPLL, FRCPLL(1)	24 (0000)

Note 1: This requires the use of the FRC self-tune feature to maintain required clock accuracy.

FIGURE 9-2: PLL SYSTEM BLOCK



Note 1: This MUX is controlled by the COSC<2:0> bits when running from the PLL or the NOSC<2:0> bits when preparing to switch to the PLL.

REGISTER 11-27: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP9R5	RP9R4	RP9R3	RP9R2	RP9R1	RP9R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP8R5	RP8R4	RP8R3	RP8R2	RP8R1	RP8R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP9R<5:0>:** RP9 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP9 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP8R<5:0>:** RP8 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP8 (see Table 11-12 for peripheral function numbers).

REGISTER 11-28: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP11R5	RP11R4	RP11R3	RP11R2	RP11R1	RP11R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP10R5	RP10R4	RP10R3	RP10R2	RP10R1	RP10R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP11R<5:0>:** RP11 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP11 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP10R<5:0>:** RP10 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP10 (see Table 11-12 for peripheral function numbers).

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REGISTER 14-6: CCPxCON3H: CCPx CONTROL 3 HIGH REGISTERS

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
OETRIG	OSCNT2	OSCNT1	OSCNT0	—	OUTM2(1)	OUTM1(1)	OUTM0(1)
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	POLACE	POLBDF(1)	PSSACE1	PSSACE0	PSSBDF1(1)	PSSBDF0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OETRIG:** CCPx Dead-Time Select bit
1 = For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered
0 = Normal output pin operation

bit 14-12 **OSCNT<2:0>:** One-Shot Event Count bits
111 = Extends one-shot event by 7 time base periods (8 time base periods total)
110 = Extends one-shot event by 6 time base periods (7 time base periods total)
101 = Extends one-shot event by 5 time base periods (6 time base periods total)
100 = Extends one-shot event by 4 time base periods (5 time base periods total)
011 = Extends one-shot event by 3 time base periods (4 time base periods total)
010 = Extends one-shot event by 2 time base periods (3 time base periods total)
001 = Extends one-shot event by 1 time base period (2 time base periods total)
000 = Does not extend one-shot trigger event

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **OUTM<2:0>:** PWMx Output Mode Control bits(1)
111 = Reserved
110 = Output Scan mode
101 = Brush DC Output mode, forward
100 = Brush DC Output mode, reverse
011 = Reserved
010 = Half-Bridge Output mode
001 = Push-Pull Output mode
000 = Steerable Single Output mode

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **POLACE:** CCPx Output Pins, OCMx, OCMxA, OCMxC and OCMxE, Polarity Control bit
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 4 **POLBDF:** CCPx Output Pins, OCxB, OCxD and OCxF, Polarity Control bit(1)
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 3-2 **PSSACE<1:0>:** PWMx Output Pins, OCMx, OCMxA, OCMxC and OCMxE, Shutdown State Control bits
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are tri-stated when a shutdown event occurs

bit 1-0 **PSSBDF<1:0>:** PWMx Output Pins, OCxB, OCxD, and OCxF, Shutdown State Control bits(1)
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are in a high-impedance state when a shutdown event occurs

Note 1: These bits are implemented in MCCPx modules only.

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REGISTER 15-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	IC32
bit 15							bit 8

R/W-0	R/W-0, HS	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICTRIG	TRIGSTAT	—	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **IC32:** Cascade Two IC Modules Enable bit (32-bit operation)
1 = ICx and ICy operate in cascade as a 32-bit module (this bit must be set in both modules)
0 = ICx functions independently as a 16-bit module

bit 7 **ICTRIG:** ICx Sync/Trigger Select bit
1 = Triggers ICx from the source designated by the SYNCSELx bits
0 = Synchronizes ICx with the source designated by the SYNCSELx bits

bit 6 **TRIGSTAT:** Timer Trigger Status bit
1 = Timer source has been triggered and is running (set in hardware, can be set in software)
0 = Timer source has not been triggered and is being held clear

bit 5 **Unimplemented:** Read as '0'

Note 1: Use these inputs as trigger sources only and never as sync sources.
2: Never use an ICx module as its own trigger source by selecting this mode.

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16.0 OUTPUT COMPARE WITH DEDICATED TIMERS

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual",* **"Output Compare with Dedicated Timer"** (DS70005159). The information in this data sheet supersedes the information in the FRM.

Devices in the PIC24FJ256GA412/GB412 family all feature six independent output compare modules. Each of these modules offers a wide range of configuration and operating options for generating pulse trains on internal device events, and can produce Pulse-Width Modulated (PWM) waveforms for driving power applications.

Key features of the output compare module include:

- Hardware-Configurable for 32-Bit Operation in All Modes by Cascading Two Adjacent Modules
- Synchronous and Trigger Modes of Output Compare Operation, with up to 31 User-Selectable Trigger/Sync Sources Available
- Two Separate Period Registers (a main register, OCxR, and a secondary register, OCxRS) for Greater Flexibility in Generating Pulses of Varying Widths
- Configurable for Single Pulse or Continuous Pulse Generation on an Output Event, or Continuous PWM Waveform Generation
- Up to 6 Clock Sources Available for Each Module, Driving a Separate Internal 16-Bit Counter

16.1 General Operating Modes

16.1.1 SYNCHRONOUS AND TRIGGER MODES

When the output compare module operates in a Free-Running mode, the internal 16-bit counter, OCxTMR, runs counts up continuously, wrapping around from 0xFFFF to 0x0000 on each overflow. Its period is synchronized to the selected external clock source. Compare or PWM events are generated each time a match between the internal counter and one of the Period registers occurs.

In Synchronous mode, the module begins performing its compare or PWM operation as soon as its selected clock source is enabled. Whenever an event occurs on the selected sync source, the module's internal counter is reset. In Trigger mode, the module waits for a sync event from another internal module to occur before allowing the counter to run.

Free-Running mode is selected by default or any time that the SYNCSEL<4:0> bits (OCxCON2<4:0>) are set to '00000'. Synchronous or Trigger modes are selected any time the SYNCSELx bits are set to any value except '00000'. The OCTRIG bit (OCxCON2<7>) selects either Synchronous or Trigger mode; setting the bit selects Trigger mode operation. In both modes, the SYNCSELx bits determine the sync/trigger source.

16.1.2 CASCADED (32-BIT) MODE

By default, each module operates independently with its own set of 16-bit Timer and Duty Cycle registers. To increase resolution, adjacent even and odd modules can be configured to function as a single 32-bit module. (For example, Modules 1 and 2 are paired, as are Modules 3 and 4, and so on.) The odd numbered module, Output Compare x (OCx), provides the Least Significant 16 bits of the 32-bit register pairs and the even numbered module, Output Compare y (OCy), provides the Most Significant 16 bits. Wrap arounds of the OCx registers cause an increment of their corresponding OCy registers.

Cascaded operation is configured in hardware by setting the OC32 bit (OCxCON2<8>) for both modules. For more information on cascading, refer to the *"dsPIC33/PIC24 Family Reference Manual",* **"Output Compare with Dedicated Timer"** (DS70005159).

REGISTER 21-1: PMCON1: EPMP CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
PMEN	—	PSIDL	ADRMUX1	ADRMUX0	—	MODE1	MODE0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
CSF1	CSF0	ALP	ALMODE	—	BUSKEEP	IRQM1	IRQM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PMEN:** Parallel Master Port Enable bit
1 = EPMP is enabled
0 = EPMP is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **PSIDL:** Parallel Master Port Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
11 = Lower address bits are multiplexed with data bits using 3 address phases
10 = Lower address bits are multiplexed with data bits using 2 address phases
01 = Lower address bits are multiplexed with data bits using 1 address phase
00 = Address and data appear on separate pins

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits
11 = Master mode
10 = Enhanced PSP; pins used are PMRD, PMWR, PMCS, PMD<7:0> and PMA<1:0>
01 = Buffered PSP; pins used are PMRD, PMWR, PMCS and PMD<7:0>
00 = Legacy Parallel Slave Port; pins used are PMRD, PMWR, PMCS and PMD<7:0>

bit 7-6 **CSF<1:0>:** Chip Select Function bits
11 = Reserved
10 = PMA15 is used for Chip Select 2, PMA14 is used for Chip Select 1
01 = PMA15 is used for Chip Select 2, PMCS1 is used for Chip Select 1
00 = PMCS2 is used for Chip Select 2, PMCS1 is used for Chip Select 1

bit 5 **ALP:** Address Latch Polarity bit
1 = Active-high (PMALL, PMALH and PMALU)
0 = Active-low ($\overline{\text{PMALL}}$, $\overline{\text{PMALH}}$ and $\overline{\text{PMALU}}$)

bit 4 **ALMODE:** Address Latch Strobe Mode bit
1 = Enables "smart" address strobes (each address phase is only present if the current access would cause a different address in the latch than the previous address)
0 = Disables "smart" address strobes

bit 3 **Unimplemented:** Read as '0'

bit 2 **BUSKEEP:** Bus Keeper bit
1 = Data bus keeps its last value when not actively being driven
0 = Data bus is in a high-impedance state when not actively being driven

bit 1-0 **IRQM<1:0>:** Interrupt Request Mode bits
11 = Interrupt is generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode), or on a read or write operation when PMA<1:0> = 11 (Addressable PSP mode only)
10 = Reserved
01 = Interrupt is generated at the end of a read/write cycle
00 = No interrupt is generated

REGISTER 22-6: LCDREF: LCD REFERENCE LADDER CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LCDIRE	—	LCDCST2	LCDCST1	LCDCST0	VLCD3PE	VLCD2PE	VLCD1PE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
LRLAP1	LRLAP0	LRLBP1	LRLBP0	—	LRLAT2	LRLAT1	LRLAT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **LCDIRE**: LCD Internal Reference Enable bit
1 = Internal LCD reference is enabled and connected to the internal contrast control circuit
0 = Internal LCD reference is disabled

bit 14 **Unimplemented**: Read as '0'

bit 13-11 **LCDCST<2:0>**: LCD Contrast Control bits
Selects the Resistance of the LCD Contrast Control Resistor Ladder:
111 = Resistor ladder is at maximum resistance (minimum contrast)
110 = Resistor ladder is at 6/7th of maximum resistance
101 = Resistor ladder is at 5/7th of maximum resistance
100 = Resistor ladder is at 4/7th of maximum resistance
011 = Resistor ladder is at 3/7th of maximum resistance
010 = Resistor ladder is at 2/7th of maximum resistance
001 = Resistor ladder is at 1/7th of maximum resistance
000 = Minimum resistance (maximum contrast); resistor ladder is shorted

bit 10 **VLCD3PE**: LCD Bias 3 Pin Enable bit
1 = Bias 3 level is connected to the external pin, LCDBIAS3
0 = Bias 3 level is internal (internal resistor ladder)

bit 9 **VLCD2PE**: LCD Bias 2 Pin Enable bit
1 = Bias 2 level is connected to the external pin, LCDBIAS2
0 = Bias 2 level is internal (internal resistor ladder)

bit 8 **VLCD1PE**: LCD Bias 1 Pin Enable bit
1 = Bias 1 level is connected to the external pin, LCDBIAS1
0 = Bias 1 level is internal (internal resistor ladder)

bit 7-6 **LRLAP<1:0>**: LCD Reference Ladder A Time Power Control bits
During Time Interval A:
11 = Internal LCD reference ladder is powered in High-Power mode
10 = Internal LCD reference ladder is powered in Medium Power mode
01 = Internal LCD reference ladder is powered in Low-Power mode
00 = Internal LCD reference ladder is powered down and unconnected

bit 5-4 **LRLBP<1:0>**: LCD Reference Ladder B Time Power Control bits
During Time Interval B:
11 = Internal LCD reference ladder is powered in High-Power mode
10 = Internal LCD reference ladder is powered in Medium Power mode
01 = Internal LCD reference ladder is powered in Low-Power mode
00 = Internal LCD reference ladder is powered down and unconnected

bit 3 **Unimplemented**: Read as '0'

24.3 Power Control

The RTCC includes a power control feature that allows the device to periodically wake-up an external device, wait for the device to be stable before sampling wake-up events from that device and then shut down the external device. This can be done completely autonomously by the RTCC, without the need to wake from the current lower power mode.

To use this feature:

1. Enable the RTCC (RTCEN = 1).
2. Set the PWCEN bit (RTCCON1L<10>).
3. Configure the RTCC pin to drive the PWC control signal (RTCOE = 1 and OUTSEL<2:0> = 011).

The polarity of the PWC control signal is selected by the PWCPOL bit (RTCCON1L<9>). An active-low or active-high signal may be used with the appropriate external switch to turn on or off the power to one or more external devices. The active-low setting may also be used in conjunction with an open-drain setting on the RTCC pin, in order to drive the ground pin(s) of the external device directly (with the appropriate external VDD pull-up device), without the need for external switches. Finally, the CHIME bit should be set to enable the PWC periodicity.

Once the RTCC and PWC are enabled and running, the PWC logic will generate a control output and a sample gate output. The control output is driven out on the RTCC pin (when RTCOE = 1 and OUTSEL<2:0> = 011) and is used to power-up or power-down the device, as described above.

Once the control output is asserted, the Stability Window begins, in which the external device is given enough time to power-up and provide a stable output.

Once the output is stable, the RTCC provides a sample gate during the Sample Window. The use of this sample gate depends on the external device being used, but typically, it is used to mask out one or more wake-up signals from the external device.

Finally, both the Stability and the Sample Windows close after the expiration of the Sample Window, and the external device is powered down.

24.3.1 POWER CONTROL CLOCK SOURCE

The Stability and Sample Windows are controlled by the PWCSAMP<7:0> and PWCSTAB<7:0> bits field in the RTCCON3L register (RTCCON3L<15:8> and <7:0>, respectively). As both the Stability and Sample Windows are defined in terms of the RTCC clock, their absolute values vary by the value of the PWC clock base period. The 8-bit magnitude of PWCSTABx and PWCSAMPx allows for a window size of 0 to 255 clock periods.

The period of the PWC clock can also be adjusted with a 1:1, 1:16, 1:64 or 1:256 prescaler, determined by the PWCPS<1:0> bits (RTCCON2L<7:6>).

In addition, certain values for the PWCSTABx and PWCSAMPx fields have specific control meanings in determining power control operations. If either bit field is 00h, the corresponding window is inactive. In addition, if the PWCSTABx field is FFh, the Stability Window remains active continuously, even if power control is disabled.

24.4 Event Timestamping

The RTCC includes two sets of Timestamp registers that may be used for the capture of Time and Date register values when an external input signal is received. The RTCC triggers the timestamps for two events:

- For Timestamp A, a falling edge on the $\overline{\text{TMPR}}$ pin
- For Timestamp B, when the devices transition from VDD to VBAT power

A Timestamp A event can be triggered while running the device in VBAT mode if the $\overline{\text{TMPR}}$ pin is pulled up to VBAT.

24.4.1 TIMESTAMP OPERATION

The event input is enabled for timestamping using the TSAEN bit (RTCCON1L<0>). When the timestamp event occurs, the present time and date values are stored in the TSATIMEL/H and TSADATEL/H registers, the TSAEVT status bit (RTCSTATL<3>) becomes set and an RTCC interrupt occurs. A new timestamp capture event cannot occur until the user clears the TSAEVT status bit.

Note 1: The TSATIMEL/H and TSADATEL/H register pairs can be used for data storage when TSAEN = 0. The values of TSATIMEL/H and TSADATEL/H will be maintained throughout all types of non-power Resets ($\overline{\text{MCLR}}$, WDT, etc).

24.4.2 MANUAL TIMESTAMP

The current time and date may be captured in the TSATIMEL/H and TSADATEL/H registers by writing a '1' to the TSAEVT bit location while the timestamp functionality is enabled (TSAEN = 1). This write will not set the TSAEVT bit, but it will initiate a timestamp capture. The TSAEVT bit will be set when the capture operation is complete. The user must poll the TSAEVT bit to determine when the capture operation is complete.

After the Timestamp registers have been read, the TSAEVT bit should be cleared to allow further hardware or software timestamp capture events.

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24.5.3 TIME/ALARM/TIMESTAMP VALUE REGISTERS

REGISTER 24-7: TIMEL/ALMTIMEL/TSATIMEL/TSBTIMEL: TIME REGISTER (LOW)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **SECTEN<2:0>:** Binary Coded Decimal Value of Seconds ‘10’ Digit bits
Contains a value from 0 to 5.

bit 11-8 **SECONE<3:0>:** Binary Coded Decimal Value of Seconds ‘1’ Digit bits
Contains a value from 0 to 9.

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 24-8: TIMEH/ALMTIMEH/TSATIMEH/TSBTIMEH: TIME REGISTER (HIGH)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-12 **HRTEN<1:0>:** Binary Coded Decimal Value of Hours ‘10’ Digit bits
Contains a value from 0 to 2.

bit 11-8 **HRONE<3:0>:** Binary Coded Decimal Value of Hours ‘1’ Digit bits
Contains a value from 0 to 9.

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **MINTEN<2:0>:** Binary Coded Decimal Value of Minutes ‘10’ Digit bits
Contains a value from 0 to 5.

bit 3-0 **MINONE<3:0>:** Binary Coded Decimal Value of Minutes ‘1’ Digit bits
Contains a value from 0 to 9.

FIGURE 27-2: EXAMPLE OF BUFFER ADDRESS GENERATION IN PIA MODE (4-WORD BUFFERS PER CHANNEL)

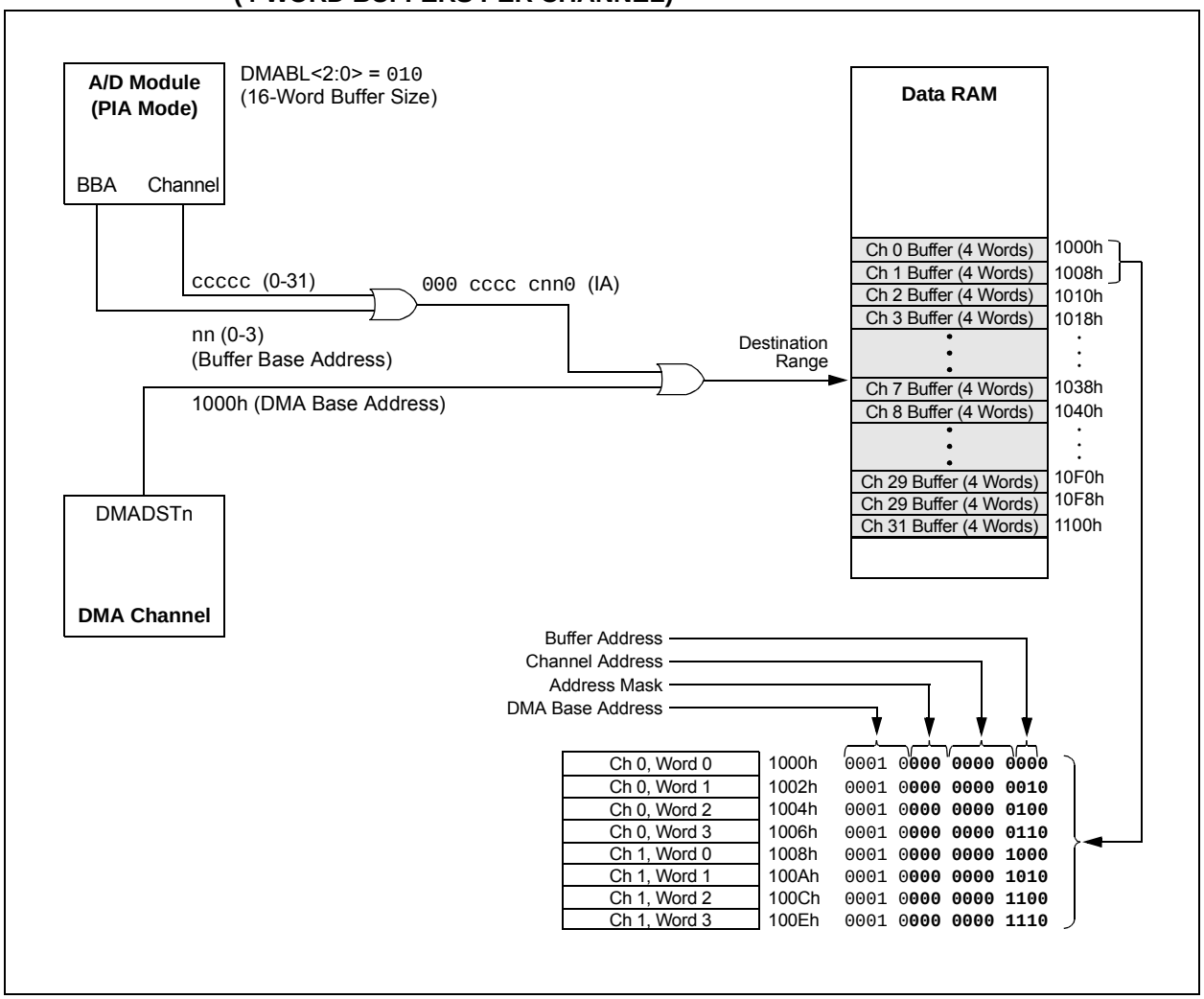

TABLE 27-1: INDIRECT ADDRESS GENERATION IN PIA MODE

DMABL<2:0>	Buffer Size per Channel (words)	Generated Offset Address (lower 11 bits)	Available Input Channels	Allowable DMADSTn Addresses
000	1	000 00cc ccc0	32	xxxx xxxx xx00 0000
001	2	000 0ccc ccn0	32	xxxx xxxx x000 0000
010	4	000 cccc cnn0	32	xxxx xxxx 0000 0000
011	8	00c cccc nnn0	32	xxxx xxx0 0000 0000
100	16	0cc cccn nnn0	32	xxxx xx00 0000 0000
101	32	ccc ccnn nnn0	32	xxxx x000 0000 0000
110	64	ccc cnnn nnn0	16	xxxx x000 0000 0000
111	128	ccc nnnn nnn0	8	xxxx x000 0000 0000

Legend: ccc = Channel number (three to five bits), n = Base buffer address (zero to seven bits), x = User-definable range of DMADSTn for base address, 0 = Masked bits of DMADSTn for IA.

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REGISTER 27-12: AD1CTMENH: A/D CTMU ENABLE REGISTER (HIGH WORD)

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
—	CTMEN<30:28>			—	—	CTMEN<25:24>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN<23:16>(1)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **CTMEN<30:28>:** CTMU Enabled During Conversion bits
1 = CTMU is enabled and connected to the selected internal channel during conversion
0 = CTMU is not connected to this channel

bit 11-10 **Unimplemented:** Read as '0'

bit 9-8 **CTMEN<25:24>:** CTMU Enabled During Conversion bits
1 = CTMU is enabled and connected to the selected internal channel during conversion
0 = CTMU is not connected to this channel

bit 7-0 **CTMEN<23:16>:** CTMU Enabled During Conversion bits(1)
1 = CTMU is enabled and connected to the selected A/D channel during conversion
0 = CTMU is not connected to this channel

Note 1: These bits are unimplemented in 64-pin devices, read as '0'.

REGISTER 27-13: AD1CTMENL: A/D CTMU ENABLE REGISTER (LOW WORD)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CTMEN<15:0>:** CTMU Enabled During Conversion bits
1 = CTMU is enabled and connected to the selected A/D channel during conversion
0 = CTMU is not connected to this channel

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Fax: 44-118-921-5820

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