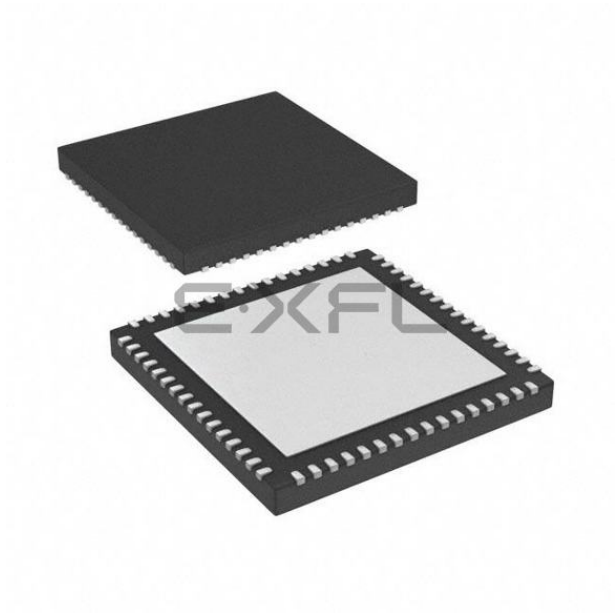
Microchip Technology - PIC24FJ256GA406T-I/MR Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256ga406t-i-mr

TABLE 6: COMPLETE PIN FUNCTION DESCRIPTIONS FOR PIC24FJXXXGB412 (CONTINUED)

Pin	Function	Pin	Function
J1	SEG4/AN3/C2INA/IOCB3/RB3	K7	SEG8/AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/IOCB14/RB14
J2	SEG5/AN2/CTCMP/C2INB/**RP13**/CTED13/IOCB2/RB2	K8	VDD
J3	PGED2/SEG63/AN7/**RP7**/U6TX/IOCB7/RB7	K9	SEG39/**RP5**/IOCD15/RD15
J4	AVDD	K10	SEG12/**RP16**/USBID/IOCF3/RF3
J5	IOCH7/RH7	K11	SEG40/**RP30**/IOCF2/RF2
J6	TCK/IOCA1/RA1	L1	PGEC2/LCDBIAS3/AN6/**RP6**/IOCB6/RB6
J7	SEG18/AN12/U6RX/CTED2/PMA11/IOCB12/RB12	L2	SEG36/VREF-/CVREF-/PMA7/IOCA9/RA9
J8	IOCH9/RH9	L3	AVSS
J9	IOCH10/RH10	L4	SEG30/AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/IOCB9/RB9
J10	SEG41/**RP15**/IOCF8/RF8	L5	IOCH6/RH6
J11	D-/IOCG3/RG3	L6	SEG53/**RP31**/IOCF13/RF13
K1	PGEC1/SEG6/VREF-/CVREF-/AN1/AN1-/**RP1**/CTED12/IOCB1/RB1	L7	SEG19/AN13/SDI4/CTED1/PMA10/IOCB13/RB13
K2	PGED1/SEG7/VREF+/CVREF+/DVREF+/AN0/**RP0**/IOCB0/RB0	L8	SEG9/AN15/**RP29**/CTED6/PMA0/PMALL/IOCB15/RB15
K3	SEG37/VREF+/CVREF+/DVREF+/PMA6/IOCA10/RA10	L9	SEG38/**RPI43**/IOCD14/RD14
K4	SEG31/AN8/**RP8**/PWRGT/IOCB8/RB8	L10	SEG10/**RP10**/PMA9/IOCF4/RF4
K5	AN11/REFI1/$\overline{\text{SS4}}$/FSYNC4/PMA12/IOCB11/RB11	L11	SEG11/**RP17**/PMA8/IOCF5/RF5
K6	SEG54/**RPI32**/CTED7/PMA18/IOCF12/RF12		

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
IOCD0	46	72	D9	I	ST	PORTD Interrupt-on-Change
IOCD1	49	76	A11	I	ST	
IOCD2	50	77	A10	I	ST	
IOCD3	51	78	B9	I	ST	
IOCD4	52	81	C8	I	ST	
IOCD5	53	82	B8	I	ST	
IOCD6	54	83	D7	I	ST	
IOCD7	55	84	C7	I	ST	
IOCD8	42	68	E9	I	ST	
IOCD9	43	69	E10	I	ST	
IOCD10	44	70	D11	I	ST	
IOCD11	45	71	C11	I	ST	
IOCD12	—	79	A9	I	ST	
IOCD13	—	80	D8	I	ST	
IOCD14	—	47	L9	I	ST	
IOCD15	—	48	K9	I	ST	
IOCE0	60	93	1E3	I	ST	PORTE Interrupt-on-Change
IOCE1	61	94	E15	I	ST	
IOCE2	62	98	E19	I	ST	
IOCE3	63	99	E30	I	ST	
IOCE4	64	100	E31	I	ST	
IOCE5	1	3	D3	I	ST	
IOCE6	2	4	C1	I	ST	
IOCE7	3	5	D2	I	ST	
IOCE8	—	18	G1	I	ST	
IOCE9	—	19	G2	I	ST	
IOCF0	58	87	B6	I	ST	PORTF Interrupt-on-Change
IOCF1	59	88	A6	I	ST	
IOCF2	34	52	K11	I	ST	
IOCF3	33	51	K10	I	ST	
IOCF4	31	49	L10	I	ST	
IOCF5	32	50	L11	I	ST	
IOCF6	35	55	H9	I	ST	
IOCF7	—	54	H8	I	ST	
IOCF8	—	53	J10	I	ST	
IOCF12	—	40	K6	I	ST	
IOCF13	—	39	L6	I	ST	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
RPI32	—	40	K6	I	ST	Remappable Peripherals (Input only)
RPI33	—	18	G1	I	ST	
RPI34	—	19	G2	I	ST	
RPI35	—	67	E8	I	ST	
RPI36	—	66	E11	I	ST	
RPI37	48	74	B11	I	ST	
RPI38	—	6	D1	I	ST	
RPI39	—	7	E4	I	ST	
RPI40	—	8	E2	I	ST	
RPI41	—	9	E1	I	ST	
RPI42	—	79	A9	I	ST	
RPI43	—	47	L9	I	ST	
RTCC	42	68	E9	O	DIGMV	Real-Time Clock Alarm/Seconds Pulse Output
SCK4	59	88	A6	I/O	DIG/ST	SPI4 Clock
SCL1	37	57	H10	I/O	DIG/I^2C/SMB	I2C1 Synchronous Serial Clock Input/Output
SCL2	32	58	H11	I/O	DIG/I^2C/SMB	I2C2 Synchronous Serial Clock Input/Output
SCL3	2	4	C1	I/O	DIG/I^2C/SMB	I2C3 Synchronous Serial Clock Input/Output
SDA1	36	56	J11	I/O	DIG/I^2C/SMB	I2C1 Data Input/Output
SDA2	31	59	G10	I/O	DIG/I^2C/SMB	I2C2 Data Input/Output
SDA3	3	5	D2	I/O	DIG/I^2C/SMB	I2C3 Data Input/Output
SDI4	28	42	L7	I	ST	SPI4 Data Input
SDO4	23	34	H5	O	DIG	SPI4 Data Output

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

TABLE 1-5: PIC24FJ256GB412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
RP0	16	25	K2	I/O	DIG/ST	Remappable Peripherals (Input or Output)
RP1	15	24	K1	I/O	DIG/ST	
RP2	42	68	E9	I/O	DIG/ST	
RP3	44	70	D11	I/O	DIG/ST	
RP4	43	69	E10	I/O	DIG/ST	
RP5	—	48	K9	I/O	DIG/ST	
RP6	17	26	L1	I/O	DIG/ST	
RP7	18	27	J3	I/O	DIG/ST	
RP8	21	32	K4	I/O	DIG/ST	
RP9	22	33	L4	I/O	DIG/ST	
RP10	31	49	L10	I/O	DIG/ST	
RP11	46	72	D9	I/O	DIG/ST	
RP12	45	71	C11	I/O	DIG/ST	
RP13	14	23	J2	I/O	DIG/ST	
RP14	29	43	K7	I/O	DIG/ST	
RP15	—	53	J10	I/O	DIG/ST	
RP16	33	51	K10	I/O	DIG/ST	
RP17	32	50	L11	I/O	DIG/ST	
RP18	11	20	H1	I/O	DIG/ST	
RP19	6	12	F2	I/O	DIG/ST	
RP20	53	82	B8	I/O	DIG/ST	
RP21	4	10	E3	I/O	DIG/ST	
RP22	51	78	B9	I/O	DIG/ST	
RP23	50	77	A10	I/O	DIG/ST	
RP24	49	76	A11	I/O	DIG/ST	
RP25	52	81	C8	I/O	DIG/ST	
RP26	5	11	F4	I/O	DIG/ST	
RP27	8	14	F3	I/O	DIG/ST	
RP28	12	21	H2	I/O	DIG/ST	
RP29	30	44	L8	I/O	DIG/ST	
RP30	—	52	K11	I/O	DIG/ST	
RP31	—	39	L6	I/O	DIG/ST	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

TABLE 5-1: DMA CHANNEL TRIGGER SOURCES

CHSEL<6:0>		Trigger (Interrupt)	CHSEL<6:0>		Trigger (Interrupt)	CHSEL<6:0>		Trigger (Interrupt)
0000000	00h	(Unimplemented)	0100110	26h	SPI1 Receive Event	1001100	4Ch	DMA Channel 4
0000001	01h	SCCP7 IC/OC Event	0100111	27h	SPI1 Transmit Event	1001101	4Dh	DMA Channel 3
0000010	02h	SCCP7 Timer	0101000	28h	SPI1 General Event	1001110	4Eh	DMA Channel 2
0000011	03h	SCCP6 IC/OC Event	0101001	29h	(Reserved, do not use)	1001111	4Fh	DMA Channel 1
0000100	04h	SCCP6 Timer	0101010	2Ah	(Reserved, do not use)	1010000	50h	DMA Channel 0
0000101	05h	SCCP5 IC/OC Event	0101011	2Bh	(Reserved, do not use)	1010001	51h	A/D Converter
0000110	06h	SCCP5 Timer	0101100	2Ch	I2C3 Slave Event	1010010	52h	USB
0000111	07h	SCCP4 IC/OC Event	0101101	2Dh	I2C3 Master Event	1010011	53h	EPMP
0001000	08h	SCCP4 Timer	0101110	2Eh	I2C3 Collision Event	1010100	54h	HLVD
0001001	09h	(Reserved, do not use)	0101111	2Fh	I2C2 Slave Event	1010101	55h	CRC Done
0001010	0Ah	(Reserved, do not use)	0110000	30h	I2C2 Master Event	1010110	56h	LCD
0001011	0Bh	SCCP3 IC/OC Event	0110001	31h	I2C2 Collision Event	1010111	57h	Crypto Done
0001100	0Ch	SCCP3 Timer	0110010	32h	I2C1 Slave Event	1011000	58h	Crypto OTP Done
0001101	0Dh	SCCP2 IC/OC Event	0110011	33h	I2C1 Master Event	1011001	59h	CLC4 Output
0001110	0Eh	SCCP2 Timer	0110100	34h	I2C1 Collision Event	1011010	5Ah	CLC3 Output
0001111	0Fh	MCCP1 IC/OC Event	0110101	35h	UART6 Transmit	1011011	5Bh	CLC2 Output
0010000	10h	MCCP1 Timer	0110110	36h	UART6 Receive	1011100	5Ch	CLC1 Output
0010001	11h	Output Compare 6	0110111	37h	UART6 Error	1011101	5Dh	(Reserved, do not use)
0010010	12h	Output Compare 5	0111000	38h	UART5 Transmit	1011110	5Eh	RTCC
0010011	13h	Output Compare 4	0111001	39h	UART5 Receive	1011111	5Fh	Timer5
0010100	14h	Output Compare 3	0111010	3Ah	UART5 Error	1100000	60h	Timer4
0010101	15h	Output Compare 2	0111011	3Bh	UART4 Transmit	1100001	61h	Timer3
0010110	16h	Output Compare 1	0111100	3Ch	UART4 Receive	1100010	62h	Timer2
0010111	17h	Input Capture 6	0111101	3Dh	UART4 Error	1100011	63h	Timer1
0011000	18h	Input Capture 5	0111110	3Eh	UART3 Transmit	1100100	64h	(Reserved, do not use)
0011001	19h	Input Capture 4	0111111	3Fh	UART3 Receive	1100101	65h	DAC
0011010	1Ah	Input Capture 3	1000000	40h	UART3 Error	1100110	66h	CTMU
0011011	1Bh	Input Capture 2	1000001	41h	UART2 Transmit	1100111	67h	Comparators Event
0011100	1Ch	Input Capture 1	1000010	42h	UART2 Receive	1101000	68h	External Interrupt 4
0011101	1Dh	SPI4 Receive Event	1000011	43h	UART2 Error	1101001	69h	External Interrupt 3
0011110	1Eh	SPI4 Transmit Event	1000100	44h	UART1 Transmit	1101010	6Ah	External Interrupt 2
0011111	1Fh	SPI4 General Event	1000101	45h	UART1 Receive	1101011	6Bh	External Interrupt 1
0100000	20h	SPI3 Receive Event	1000110	46h	UART1 Error	1101100	6Ch	External Interrupt 0
0100001	21h	SPI3 Transmit Event	1000111	47h	(Reserved, do not use)	1101101	6Dh	Interrupt-on-Change
0100010	22h	SPI3 General Event	1001000	48h	(Reserved, do not use)	1101110	6Eh	(Unimplemented)
0100011	23h	SPI2 Receive Event	1001001	49h	(Reserved, do not use)	•	•	
0100100	24h	SPI2 Transmit Event	1001010	4Ah	(Reserved, do not use)	•	•	
0100101	25h	SPI2 General Event	1001011	4Bh	DMA Channel 5	•	•	
						1111111	7Fh	

REGISTER 8-10: IFS4: INTERRUPT FLAG STATUS REGISTER 4

U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
—	DAC1IF	CTMUIF	—	—	—	CCP7IF	HLVDIF
bit 15							bit 8

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
MI2C3IF	SI2C3IF	—	—	CRCIF	U2ERIF	U1ERIF	CCP2IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **DAC1IF:** DAC Converter Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13 **CTMUIF:** CTMU Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CCP7IF:** SCCP7 Capture/Compare Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 8 **HLVDIF:** High/Low-Voltage Detect Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 7 **MI2C3IF:** Master I2C3 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6 **SI2C3IF:** Slave I2C3 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **CRCIF:** CRC Generator Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **U2ERIF:** UART2 Error Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **U1ERIF:** UART1 Error Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **CCP2IF:** SCCP2 Capture/Compare Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 8-13: IFS7: INTERRUPT FLAG STATUS REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	JTAGIF	U6ERIF	U6TXIF	U6RXIF	U5ERIF	U5TXIF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5 **JTAGIF:** JTAG Controller Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4 **U6ERIF:** UART6 Error Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **U6TXIF:** UART6 Transmitter Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **U6RXIF:** UART6 Receiver Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **U5ERIF:** UART5 Error Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **U5TXIF:** UART5 Transmitter Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 10-3: RCON2: RESET AND SYSTEM CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	r-0	R/CO-1	R/CO-1	R/CO-1	R/CO-0
—	—	—	—	VDDBOR(1)	VDDPOR(1,2)	VBPOR(1,3)	VBAT(1)
bit 7							bit 0

Legend:	r = Reserved bit	CO = Clearable Only bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4 **Reserved:** Maintain as '0'

bit 3 **VDDBOR:** VDD Brown-out Reset Flag bit(1)
- 1 = A VDD Brown-out Reset has occurred (set by hardware)
- 0 = A VDD Brown-out Reset has not occurred

bit 2 **VDDPOR:** VDD Power-on Reset Flag bit(1,2)
- 1 = A VDD Power-on Reset has occurred (set by hardware)
- 0 = A VDD Power-on Reset has not occurred

bit 1 **VBPOR:** VBAT Power-on Reset Flag bit(1,3)
- 1 = A VBAT POR has occurred (no battery connected to the VBAT pin or VBAT power is below Deep Sleep semaphore retention level, set by hardware)
- 0 = A VBAT POR has not occurred

bit 0 **VBAT:** VBAT Flag bit(1)
- 1 = A POR exit has occurred while power was applied to the VBAT pin (set by hardware)
- 0 = A POR exit from VBAT has not occurred

Note 1: This bit is set in hardware only; it can only be cleared in software.

2: This indicates a VDD POR. Setting the POR bit (RCON<0>) indicates a VCORE POR.

3: This bit is set when the device is originally powered up, even if power is present on VBAT.

TABLE 11-8: PORTG REGISTER MAP(1)

Register Name	Bit Range	Bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANSG	15:0	ANSG<15:12>				—	—	ANSG<9:6>				—	—	—	—	ANSG<1:0>	
TRISG	15:0	TRISG<15:12>				—	—	TRISG<9:6>				—	—	TRISG<3:0>			
PORTG	15:0	PORTG<15:12>				—	—	PORTG<9:6>				—	—	PORTG<3:0>			
LATG	15:0	LATG<15:12>				—	—	LATG<9:6>				—	—	LATG<3:0>			
ODCG	15:0	ODCG<15:12>				—	—	ODCG<9:6>				—	—	ODCG<3:0>			
IOCPG	15:0	IOCPG<15:12>				—	—	IOCPG<9:6>				—	—	IOCPG<3:0>			
IOCNG	15:0	IOCNG<15:12>				—	—	IOCNG<9:6>				—	—	IOCNG<3:0>			
IOCFG	15:0	IOCFG<15:12>				—	—	IOCFG<9:6>				—	—	IOCFG<3:0>			
IOCPUG	15:0	IOCPUG<15:12>				—	—	IOCPUG<9:6>				—	—	IOCPUG<3:0>			
IOCPDG	15:0	IOCPDG<15:12>				—	—	IOCPDG<9:6>				—	—	IOCPDG<3:0>			

Legend: — = unimplemented, read as '0'.

Note 1: PORT register maps show full pin count devices. Please refer to Table 1-4 and Table 1-5 for pin count-specific PORT I/O implementation.

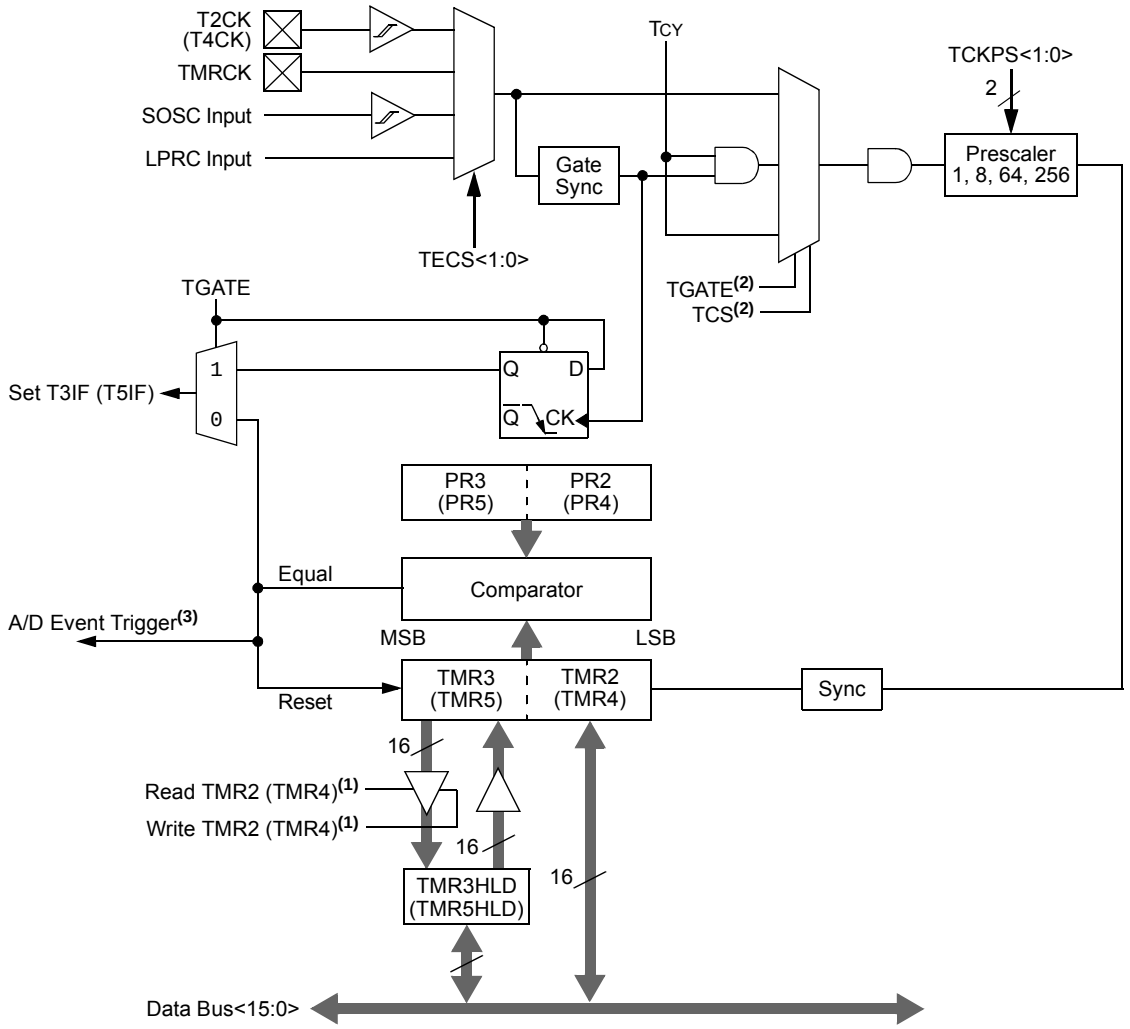
TABLE 11-9: PORTH REGISTER MAP(1)

Register Name	Bit Range	Bits															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANSH	15:0	—	—	—	—	—	—	—	—	—	—	—	ANSH<4:1>				—
TRISH	15:0	TRISH<15:1>															—
PORTH	15:0	PORTH<15:1>															—
LATH	15:0	LATH<15:1>															—
ODCH	15:0	ODCH<15:1>															—
IOCPH	15:0	IOCPH<15:1>															—
IOCNH	15:0	IOCNH<15:1>															—
IOCFH	15:0	IOCFH<15:1>															—
IOCPUH	15:0	IOCPUH<15:1>															—
IOCPDH	15:0	IOCPDH<15:1>															—

Legend: — = unimplemented, read as '0'.

Note 1: PORT register maps show full pin count devices. Please refer to Table 1-4 and Table 1-5 for pin count-specific PORT I/O implementation.

FIGURE 13-1: TIMER2/3 AND TIMER4/5 (32-BIT) BLOCK DIAGRAM



Note 1: The 32-Bit Timer Configuration bit, T32, must be set for 32-bit timer/counter operation. All control bits are respective to the T2CON and T4CON registers.

2: The timer clock input must be assigned to an available RPn/RPIn pin before use. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

3: The A/D Event Trigger is available only on Timer2/3 in 32-bit mode and Timer3 in 16-bit mode.

To set up the SPIx module for the Standard Master mode of operation:

1. If using interrupts:
   a) Clear the interrupt flag bits in the respective IFSx register.
   b) Set the interrupt enable bits in the respective IECx register.
   c) Write the SPIxIP bits in the respective IPCx register to set the interrupt priority.
2. Write the desired settings to the SPIxCON1L and SPIxCON1H registers with the MSTEN bit (SPIxCON1L<5>) = 1.
3. Clear the SPIROV bit (SPIxSTATL<6>).
4. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).
5. Write the data to be transmitted to the SPIxBUFL and SPIxBUFH registers. Transmission (and reception) will start as soon as data is written to the SPIxBUFL and SPIxBUFH registers.

To set up the SPIx module for the Standard Slave mode of operation:

1. Clear the SPIxBUF registers.
2. If using interrupts:
   a) Clear the SPIxBUFL and SPIxBUFH registers.
   b) Set the interrupt enable bits in the respective IECx register.
   c) Write the SPIxIP bits in the respective IPCx register to set the interrupt priority.
3. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with the MSTEN bit (SPIxCON1L<5>) = 0.
4. Clear the SMP bit.
5. If the CKE bit (SPIxCON1L<8>) is set, then the SSEN bit (SPIxCON1L<7>) must be set to enable the $\overline{SSx}$ pin.
6. Clear the SPIROV bit (SPIxSTATL<6>).
7. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).

FIGURE 17-1: SPIx MODULE BLOCK DIAGRAM (STANDARD MODE)

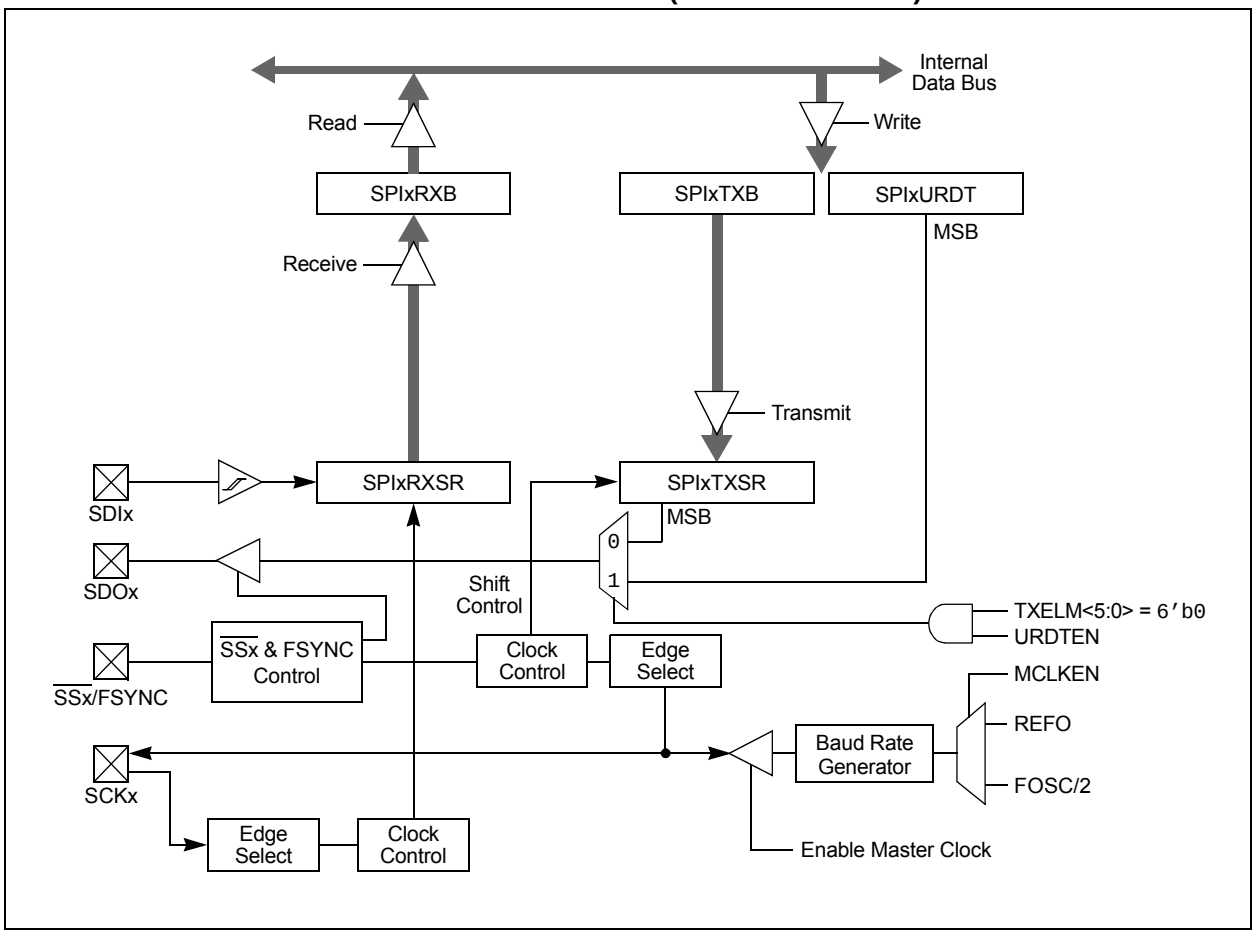


FIGURE 17-6: SPIx MASTER, FRAME SLAVE CONNECTION DIAGRAM

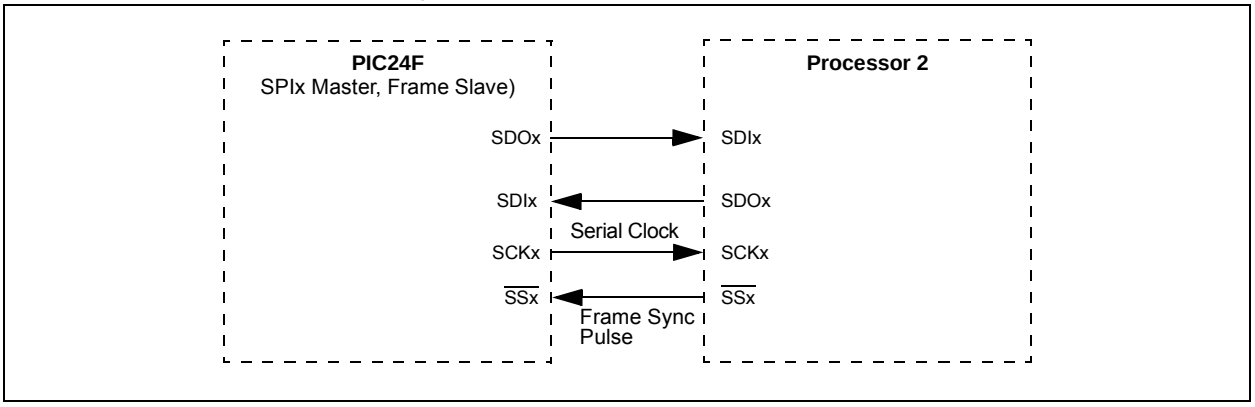


FIGURE 17-7: SPIx SLAVE, FRAME MASTER CONNECTION DIAGRAM

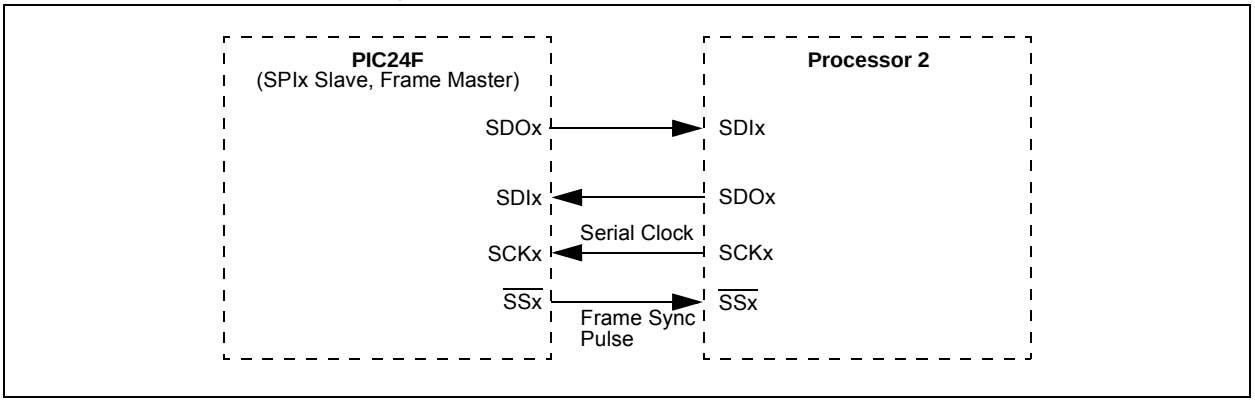
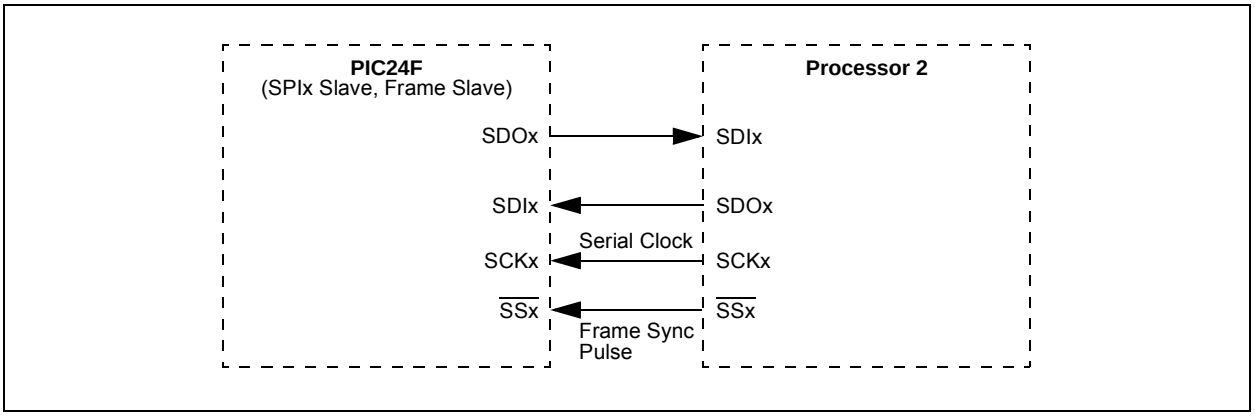


FIGURE 17-8: SPIx SLAVE, FRAME SLAVE CONNECTION DIAGRAM



EQUATION 17-1: RELATIONSHIP BETWEEN DEVICE AND SPIx CLOCK SPEED

$$\text{Baud Rate} = \frac{F_{PB}}{(2 * (\text{SPIxBRG} + 1))}$$

Where:

F_{PB} is the Peripheral Bus Clock Frequency.

19.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582). The information in this data sheet supersedes the information in the FRM.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the PIC24F device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins. The UART module includes IrDA® encoder/decoder unit.

The PIC24FJ256GA412/GB412 family devices are equipped with six UART modules, referred to as UART1 through UART6.

The primary features of the UARTx modules are:

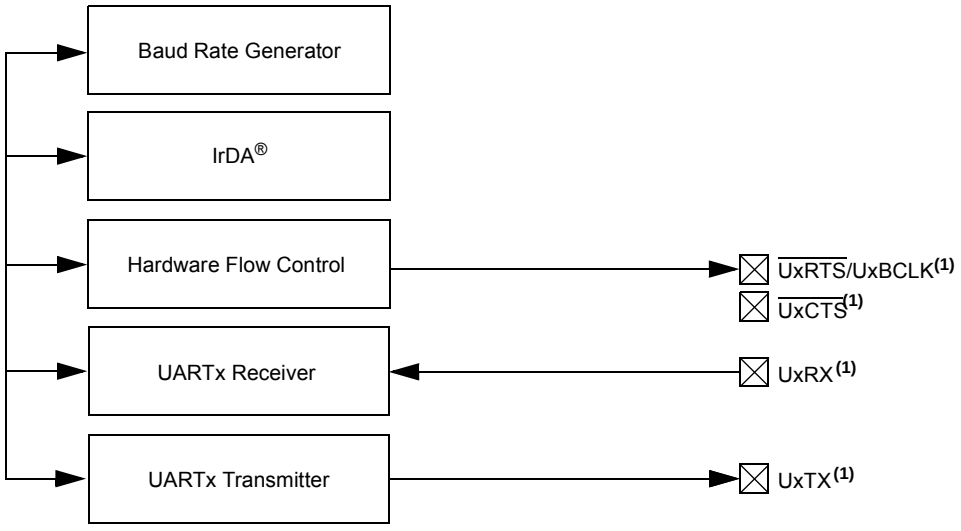
- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Range from up to 2.5 Mbps and Down to 38 Hz at 40 MIPS in 16x Mode
- Baud Rates Range from up to 10 Mbps and Down to 152 Hz at 40 MIPS in 4x Mode
- 4-Deep, First-In-First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-Bit Mode with Address Detect (9^{th} bit = 1)
- Separate Transmit and Receive Interrupts
- Loopback Mode for Diagnostic Support
- Polarity Control for Transmit and Receive Lines
- Support for Sync and Break Characters
- Supports Automatic Baud Rate Detection
- IrDA® Encoder and Decoder Logic
- Includes DMA Support
- 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UARTx module is shown in Figure 19-1. The UARTx module consists of these key important hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

Note: Throughout this section, references to register and bit names that may be associated with a specific UART module are referred to generically by the use of 'x' in place of the specific module number. Thus, "UxSTAL" might refer to the Status Low register for either UART1, UART2, UART3 or UART4.

FIGURE 19-1: UARTx SIMPLIFIED BLOCK DIAGRAM



Note 1: For UARTs that use Peripheral Pin Select (PPS), their inputs and outputs must all be assigned to available RPn/RPIn pins before use. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

REGISTER 21-9: PADCON: PAD CONFIGURATION CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
IOCON	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PMTTL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **IOCON:** Interrupt-on-Change Enable bit
Not used by the EPMP; see Register 11-1 for definition.

bit 14-1 **Unimplemented:** Read as ‘0’

bit 0 **PMTTL:** EPMP Module TTL Input Buffer Select bit
1 = EPMP module inputs (PMDx, PMCS1) use TTL input buffers
0 = EPMP module inputs use Schmitt Trigger input buffers

22.1 Registers

The LCD Controller has up to 40 registers:

- LCD Control Register (LCDCON)
- LCD Charge Pump Control Register (LCDREG)
- LCD Phase Register (LCDPS)
- LCD Voltage Ladder Control Register (LCDREF)
- Four LCD Segment Enable Registers (LCDSE3:LCDSE0)
- Up to 32 LCD Data Registers (LCDDATA31:LCDDATA0)

REGISTER 22-1: LCDCON: LCD CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
LCDEN	—	LCDSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/C-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SLPEN	WERR	CS1	CS0	LMUX2	LMUX1	LMUX0
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **LCDEN:** LCD Driver Enable bit
1 = LCD driver module is enabled
0 = LCD driver module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **LCDSIDL:** Stop LCD Drive in CPU Idle Mode Control bit
1 = LCD driver halts in CPU Idle mode
0 = LCD driver continues to operate in CPU Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **SLPEN:** LCD Driver Enable in Sleep Mode bit
1 = LCD driver module is disabled in Sleep mode
0 = LCD driver module is enabled in Sleep mode

bit 5 **WERR:** LCD Write Failed Error bit
1 = LCDDATAx register is written while WA (LCDPS<4>) = 0 (must be cleared in software)
0 = No LCD write error

bit 4-3 **CS<1:0>:** Clock Source Select bits
1x = SOSC
01 = LPRC
00 = FRC

bit 2-0 **LMUX<2:0>:** LCD Commons Select bits

LMUX<2:0>	Multiplex	Bias
111	1/8 MUX (COM<7:0>)(1)	1/3
110	1/7 MUX (COM<6:0>)(1)	1/3
101	1/6 MUX (COM<5:0>)(1)	1/3
100	1/5 MUX (COM<4:0>)(1)	1/3
011	1/4 MUX (COM<3:0>)	1/3
010	1/3 MUX (COM<2:0>)	1/2 or 1/3
001	1/2 MUX (COM<1:0>)	1/2 or 1/3
000	Static (COM0)	Static

Note 1: On 64-pin and 100-pin devices, COM4 through COM7 also have Segment functionality. If the COM is enabled in multiplexing, the Segment will not be available on that pin.

24.3 Power Control

The RTCC includes a power control feature that allows the device to periodically wake-up an external device, wait for the device to be stable before sampling wake-up events from that device and then shut down the external device. This can be done completely autonomously by the RTCC, without the need to wake from the current lower power mode.

To use this feature:

1. Enable the RTCC (RTCEN = 1).
2. Set the PWCEN bit (RTCCON1L<10>).
3. Configure the RTCC pin to drive the PWC control signal (RTCOE = 1 and OUTSEL<2:0> = 011).

The polarity of the PWC control signal is selected by the PWCPOL bit (RTCCON1L<9>). An active-low or active-high signal may be used with the appropriate external switch to turn on or off the power to one or more external devices. The active-low setting may also be used in conjunction with an open-drain setting on the RTCC pin, in order to drive the ground pin(s) of the external device directly (with the appropriate external VDD pull-up device), without the need for external switches. Finally, the CHIME bit should be set to enable the PWC periodicity.

Once the RTCC and PWC are enabled and running, the PWC logic will generate a control output and a sample gate output. The control output is driven out on the RTCC pin (when RTCOE = 1 and OUTSEL<2:0> = 011) and is used to power-up or power-down the device, as described above.

Once the control output is asserted, the Stability Window begins, in which the external device is given enough time to power-up and provide a stable output.

Once the output is stable, the RTCC provides a sample gate during the Sample Window. The use of this sample gate depends on the external device being used, but typically, it is used to mask out one or more wake-up signals from the external device.

Finally, both the Stability and the Sample Windows close after the expiration of the Sample Window, and the external device is powered down.

24.3.1 POWER CONTROL CLOCK SOURCE

The Stability and Sample Windows are controlled by the PWCSAMP<7:0> and PWCSTAB<7:0> bits field in the RTCCON3L register (RTCCON3L<15:8> and <7:0>, respectively). As both the Stability and Sample Windows are defined in terms of the RTCC clock, their absolute values vary by the value of the PWC clock base period. The 8-bit magnitude of PWCSTABx and PWCSAMPx allows for a window size of 0 to 255 clock periods.

The period of the PWC clock can also be adjusted with a 1:1, 1:16, 1:64 or 1:256 prescaler, determined by the PWCPS<1:0> bits (RTCCON2L<7:6>).

In addition, certain values for the PWCSTABx and PWCSAMPx fields have specific control meanings in determining power control operations. If either bit field is 00h, the corresponding window is inactive. In addition, if the PWCSTABx field is FFh, the Stability Window remains active continuously, even if power control is disabled.

24.4 Event Timestamping

The RTCC includes two sets of Timestamp registers that may be used for the capture of Time and Date register values when an external input signal is received. The RTCC triggers the timestamps for two events:

- For Timestamp A, a falling edge on the $\overline{\text{TMPR}}$ pin
- For Timestamp B, when the devices transition from VDD to VBAT power

A Timestamp A event can be triggered while running the device in VBAT mode if the $\overline{\text{TMPR}}$ pin is pulled up to VBAT.

24.4.1 TIMESTAMP OPERATION

The event input is enabled for timestamping using the TSAEN bit (RTCCON1L<0>). When the timestamp event occurs, the present time and date values are stored in the TSATIMEL/H and TSADATEL/H registers, the TSAEVT status bit (RTCSTATL<3>) becomes set and an RTCC interrupt occurs. A new timestamp capture event cannot occur until the user clears the TSAEVT status bit.

Note 1: The TSATIMEL/H and TSADATEL/H register pairs can be used for data storage when TSAEN = 0. The values of TSATIMEL/H and TSADATEL/H will be maintained throughout all types of non-power Resets ($\overline{\text{MCLR}}$, WDT, etc).

24.4.2 MANUAL TIMESTAMP

The current time and date may be captured in the TSATIMEL/H and TSADATEL/H registers by writing a '1' to the TSAEVT bit location while the timestamp functionality is enabled (TSAEN = 1). This write will not set the TSAEVT bit, but it will initiate a timestamp capture. The TSAEVT bit will be set when the capture operation is complete. The user must poll the TSAEVT bit to determine when the capture operation is complete.

After the Timestamp registers have been read, the TSAEVT bit should be cleared to allow further hardware or software timestamp capture events.

REGISTER 24-2: RTCCON1H: RTCC CONTROL REGISTER 1 (HIGH)

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ALRMEN	CHIME	—	—	AMASK3	AMASK2	AMASK1	AMASK0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALMRPT7	ALMRPT6	ALMRPT5	ALMRPT4	ALMRPT3	ALMRPT2	ALMRPT1	ALMRPT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ALRMEN:** Alarm Enable bit
1 = Alarm is enabled (cleared automatically after an alarm event whenever ALMRPT<7:0> = 00h and CHIME = 0)
0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit
1 = Chime is enabled; ALMRPT<7:0> bits roll over from 00h to FFh
0 = Chime is disabled; ALMRPT<7:0> bits stop once they reach 00h

bit 13-12 **Unimplemented:** Read as ‘0’

bit 11-8 **AMASK<3:0>:** Alarm Mask Configuration bits
11xx = Reserved, do not use
101x = Reserved, do not use
1001 = Once a year (or once every 4 years when configured for February 29th)
1000 = Once a month
0111 = Once a week
0110 = Once a day
0101 = Every hour
0100 = Every 10 minutes
0011 = Every minute
0010 = Every 10 seconds
0001 = Every second
0000 = Every half second

bit 7-0 **ALMRPT<7:0>:** Alarm Repeat Counter Value bits
11111111 = Alarm will repeat 255 more times
11111110 = Alarm will repeat 254 more times
• • •
00000010 = Alarm will repeat 2 more times
00000001 = Alarm will repeat 1 more time
00000000 = Alarm will not repeat

TABLE 35-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
<n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
bit4	4-bit Bit Selection field (used in word addressed instructions) ∈ {0...15}
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0000h...1FFFh}
lit1	1-bit unsigned literal ∈ {0,1}
lit4	4-bit unsigned literal ∈ {0...15}
lit5	5-bit unsigned literal ∈ {0...31}
lit8	8-bit unsigned literal ∈ {0...255}
lit10	10-bit unsigned literal ∈ {0...255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal ∈ {0...16383}
lit16	16-bit unsigned literal ∈ {0...65535}
lit23	23-bit unsigned literal ∈ {0...8388607}; LSB must be '0'
None	Field does not require an entry, may be blank
PC	Program Counter
Slit10	10-bit signed literal ∈ {-512...511}
Slit16	16-bit signed literal ∈ {-32768...32767}
Slit6	6-bit signed literal ∈ {-16...16}
Wb	Base W register ∈ {W0..W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor Working register pair (direct addressing)
Wn	One of 16 Working registers ∈ {W0..W15}
Wnd	One of 16 Destination Working registers ∈ {W0..W15}
Wns	One of 16 Source Working registers ∈ {W0..W15}
WREG	W0 (Working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws--], [++Ws], [--Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns--], [++Wns], [--Wns], [Wns+Wb] }

FIGURE 36-8: PWMx MODULE TIMING REQUIREMENTS

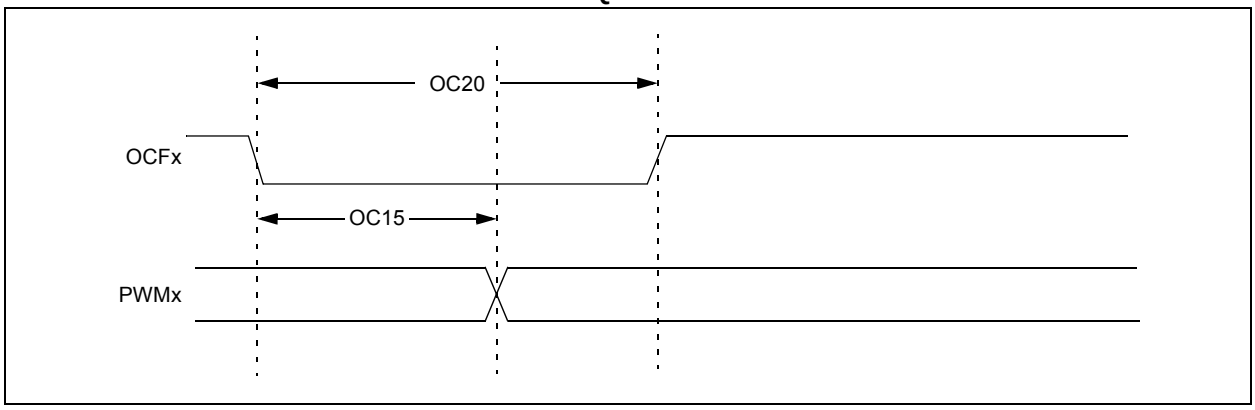


TABLE 36-29: PWMx TIMING REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Typ(1)	Max	Unit	Condition
OC15	TFD	Fault Input to PWM I/O Change	—	—	25	ns	VDD = 3.0V, -40°C to +85°C
OC20	TFH	Fault Input Pulse Width	50	—	—	ns	VDD = 3.0V, -40°C to +85°C

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 36-16: SPIx MODULE SLAVE MODE TIMING CHARACTERISTICS (CKE = 1)

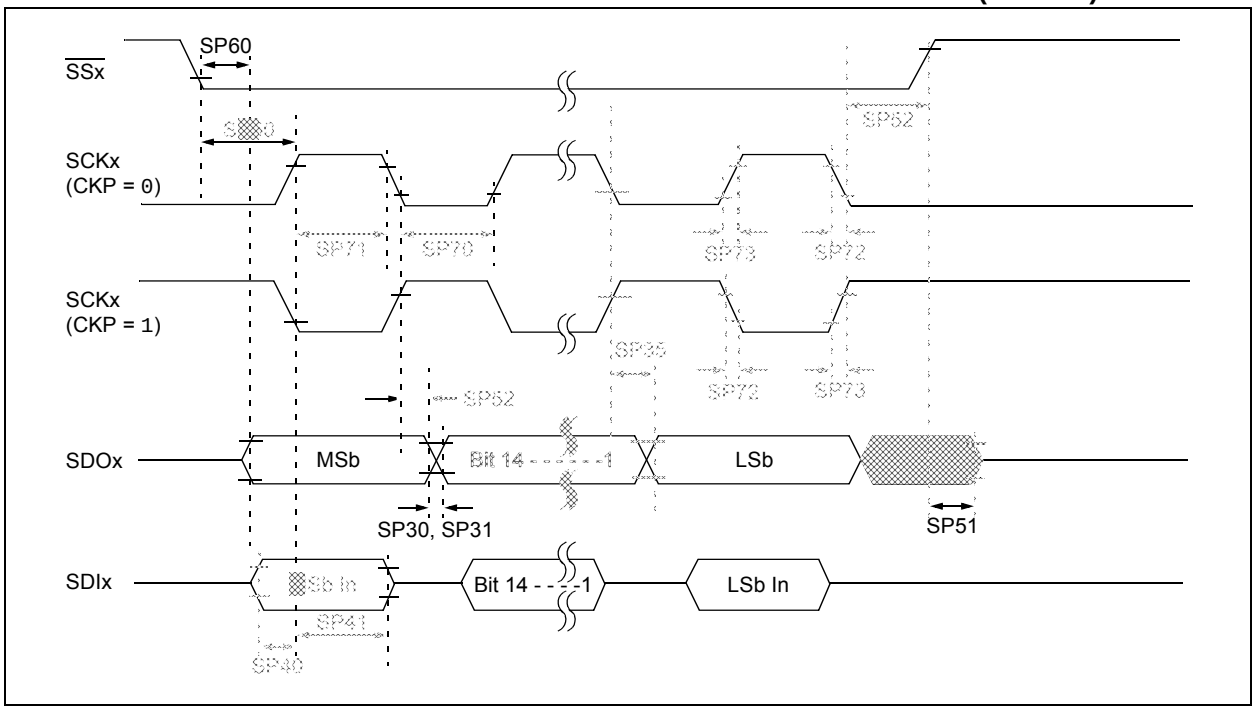


TABLE 36-37: SPIx MODULE SLAVE MODE TIMING REQUIREMENTS (CKE = 1)

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time	30	—	—	ns	
SP71	TscH	SCKx Input High Time	30	—	—	ns	
SP72	TscF	SCKx Input Fall Time(2)	—	10	25	ns	
SP73	TscR	SCKx Input Rise Time(2)	—	10	25	ns	
SP30	TdoF	SDOx Data Output Fall Time(2)	—	10	25	ns	
SP31	TdoR	SDOx Data Output Rise Time(2)	—	10	25	ns	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	—	30	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance(3)	10	—	50	ns	
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ After SCKx Edge	1.5 TCY + 40	—	—	ns	
SP60	TssL2doV	SDOx Data Output Valid After $\overline{SSx}$ Edge	—	—	50	ns	

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The minimum clock period for SCKx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

3: Assumes 50 pF load on all SPIx pins.