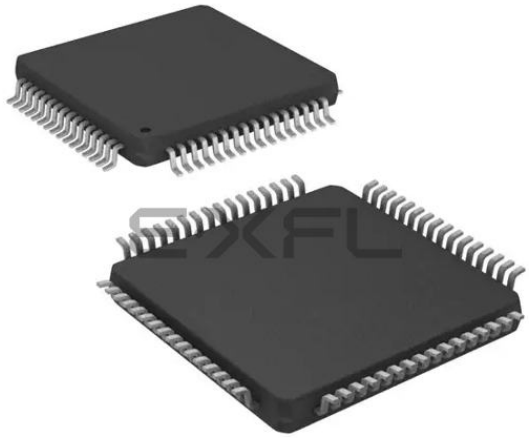

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256ga406t-i-pt

TABLE 6: COMPLETE PIN FUNCTION DESCRIPTIONS FOR PIC24FJXXXGB412

Pin	Function	Pin	Function
A1	SEG62/LVDIN/CTED8/PMD4/IOCE4/RE4	E1	SEG52/AN16/**RPI41**/PMCS2/IOCC4/RC4
A2	COM0/CTED9/PMD3/IOCE3/RE3	E2	SEG33/**RPI40**/IOCC3/RC3
A3	SEG61/CTED10/IOCG13/RG13	E3	SEG0/AN17/C1IND/**RP21**/ICM1/OCM1A/PMA5/IOCG6/RG6
A4	COM3/PMD0/IOCE0/RE0	E4	SEG51/**RPI39**/IOCC2/RC2
A5	SEG49/PMD8/IOCG0/RG0	E5	IOCJ1/RJ1
A6	SEG47/SCK4/PMD10/IOCF1/RF1	E6	SEG46/PMD9/IOCG1/RG1
A7	VBAT	E7	VDD
A8	IOCH14/RH14	E8	SEG43/**RPI35**/SDA1/PMBE1/IOCA15/RA15
A9	SEG44/**RPI42**/PMD12/IOCD12/RD12	E9	SEG13/CLC4OUT/**RP2**/RTCC/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/IOCD8/RD8
A10	SEG21/**RP23**/PMACK1/IOCD2/RD2	E10	SEG14/**RP4**/PMACK2/IOCD9/RD9
A11	SEG20/**RP24**/U5TX/ICM4/IOCD1/RD1	E11	SEG42/**RPI36**/SCL1/PMA22/IOCA14/RA14
B1	COM4/IOCH1/RH1	F1	$\overline{\text{MCLR}}$
B2	SEG50/OCM1C/CTED3/IOCG15/RG15	F2	VLCAP2/AN19/C2IND/**RP19**/ICM2/OCM2/PMA3/IOCG8/RG8
B3	COM1/PMD2/IOCE2/RE2	F3	SEG1/AN20/C1INC/C2INC/C3INC/**RP27**/DAC1/PMA2/PMALU/ IOCG9/RG9
B4	COM2/PMD1/IOCE1/RE1	F4	VLCAP1/AN18/C1INC/**RP26**/OCM1B/PMA4/IOCG7/RG7
B5	SEG58/AN22/OCM1F/PMA17/IOCA7/RA7	F5	VSS
B6	SEG27/$\overline{\text{U5CTS}}$/OC6/PMD11/IOCF0/RF0	F6	IOCH15/RH15
B7	VCAP	F7	IOCH12/RH12
B8	SEG24/**RP20**/PMRD/$\overline{\text{PMWR}}$/IOCD5/RD5	F8	VDD
B9	SEG22/**RP22**/ICM7/PMBE0/IOCD3/RD3	F9	OSCI/CLKI/IOCC12/RC12
B10	VSS	F10	VSS
B11	SOSCO/SCLKI/**RPI37**/PWRLCLK/IOCC14/RC14	F11	OSCO/CLKO/IOCC15/RC15
C1	LCDBIAS1/SCL3/IC5/PMD6/IOCE6/RE6	G1	SEG34/**RPI33**/PMCS1/IOCE8/RE8
C2	VDD	G2	SEG35/AN21/**RPI34**/PMA19/IOCE9/RE9
C3	SEG60/IOCG12/RG12	G3	TMS/SEG48/CTED14/IOCA0/RA0
C4	SEG59/CTED11/PMA16/IOCG14/RG14	G4	COM6/IOCH3/RH3
C5	SEG57/AN23/OCM1E/IOCA6/RA6	G5	VDD
C6	VSS	G6	VSS
C7	SEG26/C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/PMD15/IOCD7/RD7	G7	VSS
C8	SEG23/**RP25**/PMWR/PMENB/IOCD4/RD4	G8	IOCH11/RH11
C9	IOCH13/RH13	G9	TDO/SEG28/IOCA5/RA5
C10	SOSCI/IOCC13/RC13	G10	SEG56/SDA2/PMA20/IOCA3/RA3
C11	SEG16/C3INC/**RP12**/PMA14/PMCS/APMCS1/IOCD11/RD11	G11	TDI/PMA21/IOCA4/RA4
D1	SEG32/**RPI38**/OCM1D/IOCC1/RC1	H1	PGEC3/SEG2/AN5/C1INA/**RP18**/ICM3/OCM3/IOCB5/RB5
D2	LCDBIAS0/SDA3/IC6/PMD7/IOCE7/RE7	H2	PGED3/SEG3/AN4/C1INB/**RP28**/$\overline{\text{USBOE}}$/IOCB4/RB4
D3	LCDBIAS2/IC4/CTED4/PMD5/IOCE5/RE5	H3	COM7/IOCH4/RH4
D4	COM5/IOCH2/RH2	H4	IOCH5/RH5
D5	IOCJ0/RJ0	H5	SEG29/CVREF/AN10/SDO4/PMA13/IOCB10/RB10
D6	VDD	H6	VDD
D7	SEG25/C3INB/U5RX/OC4/PMD14/IOCD6/RD6	H7	IOCH8/RH8
D8	SEG45/PMD13/IOCD13/RD13	H8	VBUS/IOCF7/RF7
D9	SEG17/CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/IOCD0/RD0	H9	VUSB3V3
D10	VSS	H10	D+/IOCG2/RG2
D11	SEG15/C3IND/RP3/PMA15/APMCS2/IOCD10/RD10	H11	SEG55/SCL2/IOCA2/RA2

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
SEG0	4	10	E3	O	ANA	LCD Driver Segment Outputs
SEG1	8	14	F3	O	ANA	
SEG2	11	20	H1	O	ANA	
SEG3	12	21	H2	O	ANA	
SEG4	13	22	J1	O	ANA	
SEG5	14	23	J2	O	ANA	
SEG6	15	24	K1	O	ANA	
SEG7	16	25	K2	O	ANA	
SEG8	29	43	K7	O	ANA	
SEG9	30	44	L8	O	ANA	
SEG10	31	49	L10	O	ANA	
SEG11	32	50	L11	O	ANA	
SEG12	33	51	K10	O	ANA	
SEG13	42	68	E9	O	ANA	
SEG14	43	69	E10	O	ANA	
SEG15	44	70	D11	O	ANA	
SEG16	45	71	C11	O	ANA	
SEG17	46	72	D9	O	ANA	
SEG18	27	41	J7	O	ANA	
SEG19	28	42	L7	O	ANA	
SEG20	49	76	A11	O	ANA	
SEG21	50	77	A10	O	ANA	
SEG22	51	78	B9	O	ANA	
SEG23	52	81	C8	O	ANA	
SEG24	53	82	B8	O	ANA	
SEG25	54	83	D7	O	ANA	
SEG26	55	84	C7	O	ANA	
SEG27	58	87	B6	O	ANA	
SEG28	—	61	G9	O	ANA	
SEG29	23	34	H5	O	ANA	
SEG30	22	33	L4	O	ANA	
SEG31	21	32	K4	O	ANA	
SEG32	—	6	D1	O	ANA	
SEG33	—	8	E2	O	ANA	
SEG34	—	18	G1	O	ANA	
SEG35	—	19	G2	O	ANA	
SEG36	—	28	L2	O	ANA	
SEG37	—	29	K3	O	ANA	
SEG38	—	47	L9	O	ANA	
SEG39	—	48	K9	O	ANA	
SEG40	34	52	K11	O	ANA	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

TABLE 4-5: SFR BLOCK 000h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
Core			**Interrupt Controller**			IPC7	0B6	0100010001000100
WREG0	000	0000000000000000	INTCON1	080	0000000000000000	IPC8	0B8	0100010001000100
WREG1	002	0000000000000000	INTCON2	082	1000000000000000	IPC9	0BA	0100010001000100
WREG2	004	0000000000000000	INTCON4	086	0000000000000000	IPC10	0BC	0100010001000100
WREG3	006	0000000000000000	IFS0	088	0000000000000000	IPC11	0BE	0100010001000100
WREG4	008	0000000000000000	IFS1	08A	0000000000000000	IPC12	0C0	0100010001000100
WREG5	00A	0000000000000000	IFS2	08C	0000000000000000	IPC13	0C2	0100010001000000
WREG6	00C	0000000000000000	IFS3	08E	0000000000000000	IPC14	0C4	0100010001000100
WREG7	00E	0000000000000000	IFS4	090	0000000000000000	IPC15	0C6	0100010001000100
WREG8	010	0000000000000000	IFS5	092	0000000000000000	IPC16	0C8	0100010001000100
WREG9	012	0000000000000000	IFS6	094	0000000000000000	IPC17	0CA	0100010000000000
WREG10	014	0000000000000000	IFS7	096	0000000000000000	IPC18	0CC	0000000001000100
WREG11	016	0000000000000000	IEC0	098	0000000000000000	IPC19	0CE	0000010001000000
WREG12	018	0000000000000000	IEC1	09A	0000000000000000	IPC20	0D0	0100010001000000
WREG13	01A	0000000000000000	IEC2	09C	0000000000000000	IPC21	0D2	0100010001000100
WREG14	01C	0000000000000000	IEC3	09E	0000000000000000	IPC22	0D4	0100010001000100
WREG15	01E	0000000000000000	IEC4	0A0	0000000000000000	IPC23	0D6	0100010001000100
SPLIM	020	xxxxxxxxxxxxxxx0	IEC5	0A2	0000000000000000	IPC24	0D8	0100010001000100
PCL	02E	0000000000000000	IEC6	0A4	0000000000000000	IPC25	0DA	0000010001000100
PCH	030	0000000000000000	IEC7	0A6	0000000000000000	IPC26	0DC	0000010000000000
DSRPAG	032	0000000000000000	IPC0	0A8	0100010001000100	IPC27	0DE	0100010001000000
DSWPAG	034	0000000000000000	IPC1	0AA	0100010001000100	IPC28	0E0	0100010001000100
RCOUNT	036	xxxxxxxxxxxxxxxx	IPC2	0AC	0100010001000100	IPC29	0E2	0000000001000100
SR	042	0000000000000000	IPC3	0AE	0100010001000100	INTTREG	0E4	0000000000000000
CORCON	044	0000000000000100	IPC4	0B0	0100010001000100			
DISICNT	052	00xxxxxxxxxxxxxx	IPC5	0B2	0100010000000100			
TBLPAG	054	0000000000000000	IPC6	0B4	0100010001000100			

Legend: x = unknown or indeterminate value. Reset and address values are in hexadecimal.

4.3.5.2 Data Write into EDS

In order to write data to EDS space, such as in EDS reads, an Address Pointer is set up by loading the required EDS page number into the DSWPAG register and assigning the offset address to one of the W registers. Once the above assignment is done, then the EDS window is enabled by setting bit 15 of the Working register assigned with the offset address and the accessed location can be written.

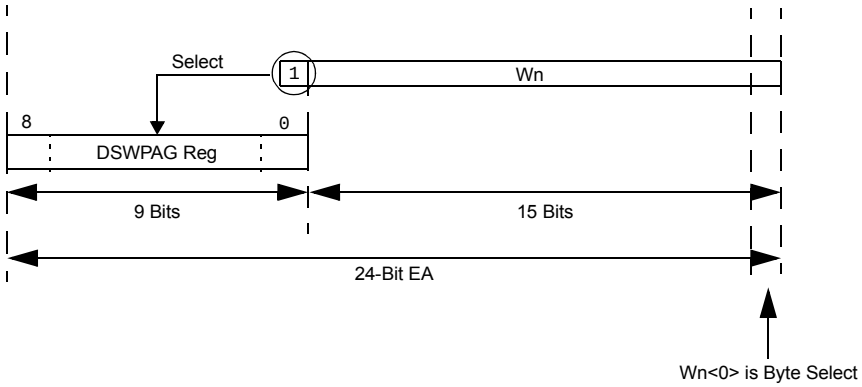
Figure 4-8 illustrates how the EDS space address is generated for write operations.

When the MSb of EA is '1', the lower 9 bits of DSWPAG are concatenated to the lower 15 bits of EA to form a 24-bit EDS address for write operations. Example 4-2 shows how to write a byte, word and double-word to EDS.

The DS Page registers (DSRPAG/DSWPAG) do not update automatically while crossing a page boundary when the rollover happens from 0xFFFF to 0x8000. While developing code in assembly, care must be taken to update the DS Page registers when an Address Pointer crosses the page boundary. The 'C' compiler keeps track of the addressing, and increments or decrements the DS Page registers accordingly, while accessing contiguous data memory locations.

Note 1:	All write operations to EDS are executed in a single cycle.
2:	Use of Read/Modify/Write operation on any EDS location under a REPEAT instruction is not supported. For example, BCLR, BSW, BTG, RLC f, RLNC f, RRC f, RRNC f, ADD f, SUB f, SUBR f, AND f, IOR f, XOR f, ASR f, ASL f.
3:	Use the DSRPAG register while performing Read/Modify/Write operations.

FIGURE 4-8: EDS ADDRESS GENERATION FOR WRITE OPERATIONS



EXAMPLE 4-2: EDS WRITE CODE IN ASSEMBLY

```
; Set the EDS page where the data to be written
    mov     #0x0002, w0
    mov     w0, DSWPAG      ;page 2 is selected for write
    mov     #0x0800, w1     ;select the location (0x800) to be written
    bset    w1, #15         ;set the MSB of the base address, enable EDS mode

;Write a byte to the selected location
    mov     #0x00A5, w2
    mov     #0x003C, w3
    mov.b   w2, [w1++]      ;write Low byte
    mov.b   w3, [w1++]      ;write High byte

;Write a word to the selected location
    mov     #0x1234, w2     ;
    mov     w2, [w1]        ;

;Write a Double - word to the selected location
    mov     #0x1122, w2
    mov     #0x4455, w3
    mov.d   w2, [w1]        ;2 EDS writes
```

REGISTER 5-1: DMACON: DMA ENGINE CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
DMAEN	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PRSSEL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **DMAEN:** DMA Module Enable bit
1 = Enables module
0 = Disables module and terminates all active DMA operation(s)

bit 14-1 **Unimplemented:** Read as '0'

bit 0 **PRSSEL:** Channel Priority Scheme Selection bit
1 = Round robin scheme
0 = Fixed priority scheme

TABLE 8-2: IMPLEMENTED INTERRUPT VECTORS (CONTINUED)

Interrupt Source	Vector Number	IRQ #	IVT Address	Interrupt Bit Locations		
				Flag	Enable	Priority
MCCP1 Capture/Compare	71	63	000092h	IFS3<15>	IEC3<15>	IPC15<14:12>
MCCP1 Timer	109	101	0000DEh	IFS6<5>	IEC6<5>	IPC25<6:4>
SCCP2 Capture/Compare	72	64	000094h	IFS4<0>	IEC4<0>	IPC16<2:0>
SCCP2 Timer	110	102	0000E0h	IFS6<6>	IEC6<6>	IPC25<10:8>
SCCP3 Capture/Compare	102	94	0000D0h	IFS5<14>	IEC5<14>	IPC23<10:8>
SCCP3 Timer	51	43	00006Ah	IFS2<11>	IEC2<11>	IPC10<14:12>
SCCP4 Capture/Compare	103	95	0000D2h	IFS5<15>	IEC5<15>	IPC23<14:12>
SCCP4 Timer	52	44	00006Ch	IFS2<12>	IEC2<12>	IPC11<2:0>
Output Compare 1	10	2	000018h	IFS0<2>	IEC0<2>	IPC0<10:8>
Output Compare 2	14	6	000020h	IFS0<6>	IEC0<6>	IPC1<10:8>
Output Compare 3	33	25	000046h	IFS1<9>	IEC1<9>	IPC6<6:4>
Output Compare 4	34	26	000048h	IFS1<10>	IEC1<10>	IPC6<10:8>
Output Compare 5	49	41	000066h	IFS2<9>	IEC2<9>	IPC10<6:4>
Output Compare 6	50	42	000068h	IFS2<10>	IEC2<10>	IPC10<10:8>
Real-Time Clock and Calendar (RTCC)	70	62	000090h	IFS3<14>	IEC3<14>	IPC15<10:8>
RTCC Timestamp	118	110	0000F0h	IFS6<14>	IEC6<14>	IPC27<10:8>
SCCP5 Capture/Compare	30	22	000040h	IFS1<6>	IEC1<6>	IPC5<10:8>
SCCP6 Capture/Compare	31	23	000042h	IFS1<7>	IEC1<7>	IPC5<14:12>
SCCP7 Capture/Compare	81	73	0000A6h	IFS4<9>	IEC4<9>	IPC18<6:4>
SCCP5 Timer	55	47	000072h	IFS2<15>	IEC2<15>	IPC11<14:12>
SCCP6 Timer	56	48	000074h	IFS3<0>	IEC3<0>	IPC12<2:0>
SCCP7 Timer	59	51	00007Ah	IFS3<3>	IEC3<3>	IPC12<14:12>
SPI1 General	17	9	000026h	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 Receive	66	58	000088h	IFS3<10>	IEC3<10>	IPC14<10:8>
SPI1 Transmit	18	10	000028h	IFS0<10>	IEC0<10>	IPC2<10:8>
SPI2 General	40	32	000054h	IFS2<0>	IEC2<0>	IPC8<2:0>
SPI2 Receive	67	59	00008Ah	IFS3<11>	IEC3<11>	IPC14<14:12>
SPI2 Transmit	41	33	000056h	IFS2<1>	IEC2<1>	IPC8<6:4>
SPI3 General	98	90	0000C8h	IFS5<10>	IEC5<10>	IPC22<10:8>
SPI3 Receive	68	60	00008Ch	IFS3<12>	IEC3<12>	IPC15<2:0>
SPI3 Transmit	99	91	0000CAh	IFS5<11>	IEC5<11>	IPC22<14:12>
SPI3 Transmit	101	93	0000CEh	IFS5<13>	IEC5<13>	IPC23<6:4>
SPI4 General	100	92	0000CCh	IFS5<12>	IEC5<12>	IPC23<2:0>
SPI4 Receive	65	57	000086h	IFS3<9>	IEC3<9>	IPC14<6:4>
Timer1	11	3	00001Ah	IFS0<3>	IEC0<3>	IPC0<14:12>
Timer2	15	7	000022h	IFS0<7>	IEC0<7>	IPC1<14:12>
Timer3	16	8	000024h	IFS0<8>	IEC0<8>	IPC2<2:0>
Timer4	35	27	00004Ah	IFS1<11>	IEC1<11>	IPC6<14:12>
Timer5	36	28	00004Ch	IFS1<12>	IEC1<12>	IPC7<2:0>
UART1 Error	73	65	000096h	IFS4<1>	IEC4<1>	IPC16<6:4>
UART1 Receiver	19	11	00002Ah	IFS0<11>	IEC0<11>	IPC2<14:12>
UART1 Transmitter	20	12	00002Ch	IFS0<12>	IEC0<12>	IPC3<2:0>
UART2 Error	74	66	000098h	IFS4<2>	IEC4<2>	IPC16<10:8>
UART2 Receiver	38	30	000050h	IFS1<14>	IEC1<14>	IPC7<10:8>
UART2 Transmitter	39	31	000052h	IFS1<15>	IEC1<15>	IPC7<14:12>

REGISTER 8-38: IPC16: INTERRUPT PRIORITY CONTROL REGISTER 16

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CRCIP2	CRCIP1	CRCIP0	—	U2ERIP2	U2ERIP1	U2ERIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U1ERIP2	U1ERIP1	U1ERIP0	—	CCP2IP2	CCP2IP1	CCP2IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **CRCIP<2:0>:** CRC Generator Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **U2ERIP<2:0>:** UART2 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **U1ERIP<2:0>:** UART1 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **CCP2IP<2:0>:** SCCP2 Capture/Compare Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

NOTES:

11.5.5 CONSIDERATIONS FOR PERIPHERAL PIN SELECTION

The ability to control Peripheral Pin Selection introduces several considerations into application design that could be overlooked. This is particularly true for several common peripherals that are available only as remappable peripherals.

The main consideration is that the Peripheral Pin Selects are not available on default pins in the device's default (Reset) state. Since all RPINRx registers reset to '111111' and all RPORx registers reset to '000000', all Peripheral Pin Select inputs are tied to Vss, and all Peripheral Pin Select outputs are disconnected.

This situation requires the user to initialize the device with the proper peripheral configuration before any other application code is executed. Since the IOLOCK bit resets in the unlocked state, it is not necessary to execute the unlock sequence after the device has come out of Reset. For application safety, however, it is best to set IOLOCK and lock the configuration after writing to the control registers.

Because the unlock sequence is timing-critical, it must be executed as an assembly language routine in the same manner as changes to the oscillator configuration. If the bulk of the application is written in 'C', or another high-level language, the unlock sequence should be performed by writing in-line assembly.

Choosing the configuration requires the review of all Peripheral Pin Selects and their pin assignments, especially those that will not be used in the application. In all cases, unused pin-selectable peripherals should be disabled completely. Unused peripherals should have their inputs assigned to an unused RPn/RPIn pin function. I/O pins with unused RPn functions should be configured with the null peripheral output.

The assignment of a peripheral to a particular pin does not automatically perform any other configuration of the pin's I/O circuitry. In theory, this means adding a pin-selectable output to a pin may mean inadvertently driving an existing peripheral input when the output is driven. Users must be familiar with the behavior of other fixed peripherals that share a remappable pin and know when to enable or disable them. To be safe, fixed digital peripherals that share the same pin should be disabled when not in use.

Along these lines, configuring a remappable pin for a specific peripheral does not automatically turn that feature on. The peripheral must be specifically configured for operation and enabled as if it were tied to a fixed pin. Where this happens in the application code (immediately following a device Reset and peripheral configuration or inside the main application routine) depends on the peripheral and its use in the application.

A final consideration is that Peripheral Pin Select functions neither override analog inputs nor reconfigure pins with analog functions for digital I/O. If a pin is configured as an analog input on device Reset, it must be explicitly reconfigured as a digital I/O when used with a Peripheral Pin Select.

Example 11-4 shows a configuration for bidirectional communication with flow control using UART1. The following input and output functions are used:

- Input Functions: U1RX, $\overline{\text{U1CTS}}$
- Output Functions: U1TX, $\overline{\text{U1RTS}}$

EXAMPLE 11-4: CONFIGURING UART1 INPUT AND OUTPUT FUNCTIONS

```
// Unlock Registers
__builtin_write_OSCCONL(OSCCON & 0xbf);

// Configure Input Functions (Table 11-11)
    // Assign U1RX To Pin RP0
    RPINR18bits.U1RXR = 0;

    // Assign U1CTS To Pin RP1
    RPINR18bits.U1CTSR = 1;

// Configure Output Functions (Table 11-12)
    // Assign U1TX To Pin RP2
    RPOR1bits.RP2R = 3;

    // Assign U1RTS To Pin RP3
    RPOR1bits.RP3R = 4;

// Lock Registers
asm volatile   ("MOV   #OSCCON, w1   \n"
               "MOV   #0x46, w2     \n"
               "MOV   #0x57, w3     \n"
               "MOV.b  w2, [w1]     \n"
               "MOV.b  w3, [w1]     \n"
               "BSET   OSCCON, #6");

// or use the XC16 built-in macro:
// __builtin_write_OSCCONL(OSCCON | 0x40);
```

REGISTER 17-1: SPIxCON1L: SPIx CONTROL REGISTER 1 LOW (CONTINUED)

bit 9 **SMP:** SPIx Data Input Sample Phase bit
Master Mode:
1 = Input data is sampled at the end of data output time
0 = Input data is sampled at the middle of data output time
Slave Mode:
Input data is always sampled at the middle of data output time, regardless of the SMP setting.

bit 8 **CKE:** SPIx Clock Edge Select bit(1)
1 = Transmit happens on transition from active clock state to Idle clock state
0 = Transmit happens on transition from Idle clock state to active clock state

bit 7 **SSEN:** Slave Select Enable bit (Slave mode)(2)
1 = $\overline{SSx}$ pin is used by the macro in Slave mode; $\overline{SSx}$ pin is used as the slave select input
0 = $\overline{SSx}$ pin is not used by the macro ($\overline{SSx}$ pin will be controlled by the port I/O)

bit 6 **CKP:** Clock Polarity Select bit
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

bit 4 **DISSDI:** Disable SDIx Input Port bit
1 = SDIx pin is not used by the module; pin is controlled by port function
0 = SDIx pin is controlled by the module

bit 3 **DISSCK:** Disable SCKx Output Port bit
1 = SCKx pin is not used by the module; pin is controlled by port function
0 = SCKx pin is controlled by the module

bit 2 **MCLKEN:** Master Clock Enable bit(3)
1 = REFO is used by the BRG
0 = FOSC/2 is used by the BRG

bit 1 **SPIFE:** Frame Sync Pulse Edge Select bit
1 = Frame Sync pulse (Idle-to-active edge) coincides with the first bit clock
0 = Frame Sync pulse (Idle-to-active edge) precedes the first bit clock

bit 0 **ENHBUF:** Enhanced Buffer Enable bit
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

Note 1: When AUDEN (SPIxCON1H<15>) = 1, this module functions as if CKE = 0, regardless of its actual value.
2: When FRMEN = 1, SSEN is not used.
3: MCLKEN can only be written when the SPIEN bit = 0.
4: This channel is not meaningful for DSP/PCM mode as LRC follows FRMSYPW.

FIGURE 17-6: SPIx MASTER, FRAME SLAVE CONNECTION DIAGRAM

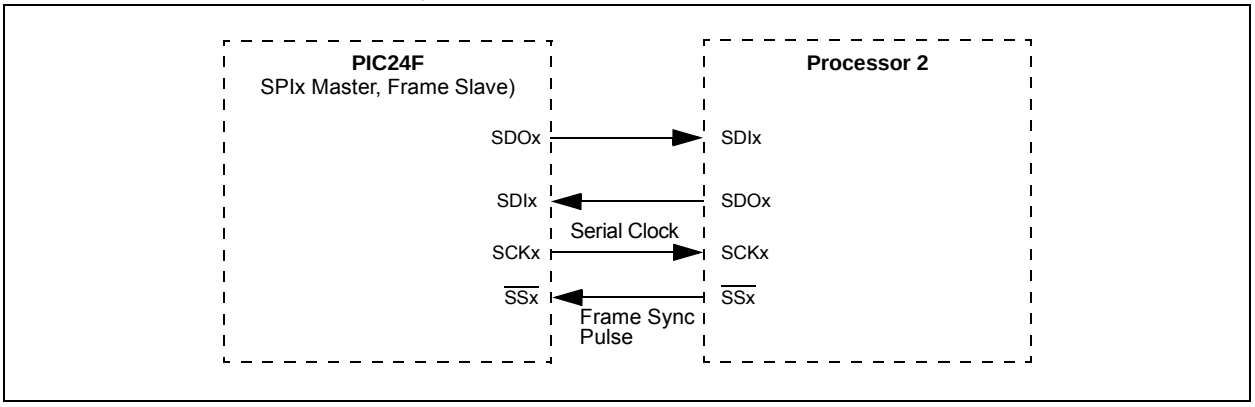


FIGURE 17-7: SPIx SLAVE, FRAME MASTER CONNECTION DIAGRAM

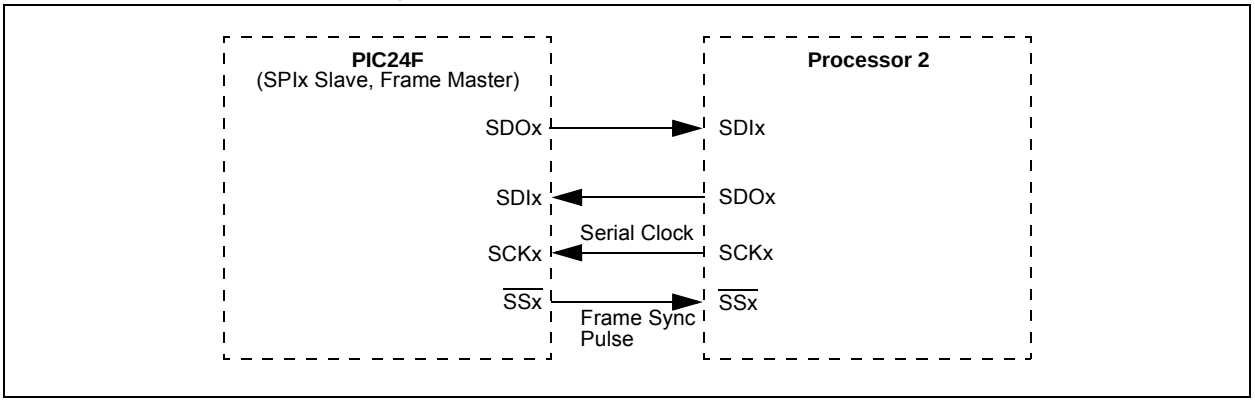
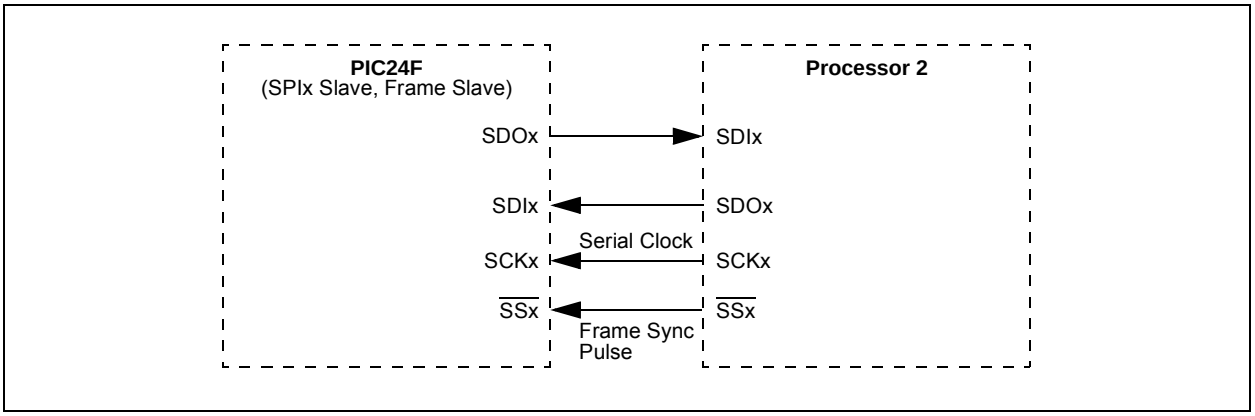


FIGURE 17-8: SPIx SLAVE, FRAME SLAVE CONNECTION DIAGRAM



EQUATION 17-1: RELATIONSHIP BETWEEN DEVICE AND SPIx CLOCK SPEED

$$\text{Baud Rate} = \frac{F_{PB}}{(2 * (\text{SPIxBRG} + 1))}$$

Where:

F_{PB} is the Peripheral Bus Clock Frequency.

19.2 Transmitting in 8-Bit Data Mode

1. Set up the UARTx:
   a) Write appropriate values for data, parity and Stop bits.
   b) Write appropriate baud rate value to the UxBRG register.
   c) Set up transmit and receive interrupt enable and priority bits.
2. Enable the UARTx.
3. Set the UTXEN bit (causes a transmit interrupt, two cycles after being set).
4. Write a data byte to the lower byte of the UxTXREG word. The value will be immediately transferred to the Transmit Shift Register (TSR) and the serial bit stream will start shifting out with the next rising edge of the baud clock.
5. Alternatively, the data byte may be transferred while UTXEN = 0 and then the user may set UTXEN. This will cause the serial bit stream to begin immediately because the baud clock will start from a cleared state.
6. A transmit interrupt will be generated as per interrupt control bits, UTXISEL<1:0>.

19.3 Transmitting in 9-Bit Data Mode

1. Set up the UARTx (as described in **Section 19.2 "Transmitting in 8-Bit Data Mode"**).
2. Enable the UARTx.
3. Set the UTXEN bit (causes a transmit interrupt).
4. Write UxTXREG as a 16-bit value only.
5. A word write to UxTXREG triggers the transfer of the 9-bit data to the TSR. The serial bit stream will start shifting out with the first rising edge of the baud clock.
6. A transmit interrupt will be generated as per the setting of control bits, UTXISELx.

19.4 Break and Sync Transmit Sequence

The following sequence will send a message frame header, made up of a Break, followed by an auto-baud Sync byte.

1. Configure the UARTx for the desired mode.
2. Set UTXEN and UTXBRK to set up the Break character.
3. Load the UxTXREG with a dummy character to initiate transmission (value is ignored).
4. Write 55h to UxTXREG; this loads the Sync character into the transmit FIFO.
5. After the Break has been sent, the UTXBRK bit is reset by hardware. The Sync character now transmits.

19.5 Receiving in 8-Bit or 9-Bit Data Mode

1. Set up the UARTx (as described in **Section 19.2 "Transmitting in 8-Bit Data Mode"**).
2. Enable the UARTx.
3. Set the URXEN bit (UxSTAL<12>).
4. A receive interrupt will be generated when one or more data characters have been received as per interrupt control bits, URXISEL<1:0>.
5. Read the OERR bit to determine if an overrun error has occurred. The OERR bit must be reset in software.
6. Read UxRXREG.

The act of reading the UxRXREG character will move the next character to the top of the receive FIFO, including a new set of PERR and FERR values.

19.6 Operation of $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Control Pins

UARTx Clear-to-Send ($\overline{\text{UxCTS}}$) and Request-to-Send ($\overline{\text{UxRTS}}$) are the two hardware controlled pins that are associated with the UARTx modules. These two pins allow the UARTx to operate in Simplex and Flow Control mode. They are implemented to control the transmission and reception between the Data Terminal Equipment (DTE). The UEN<1:0> bits in the UxMODE register configure these pins.

19.7 Infrared Support

The UARTx module provides two types of infrared UART support: one is the IrDA clock output to support an external IrDA encoder and decoder device (legacy module support), and the other is the full implementation of the IrDA encoder and decoder. Note that because the IrDA modes require a 16x baud clock, they will only work when the BRGH bit (UxMODE<3>) is '0'.

19.7.1 IrDA CLOCK OUTPUT FOR EXTERNAL IrDA SUPPORT

To support external IrDA encoder and decoder devices, the UxBCLK pin (same as the $\overline{\text{UxRTS}}$ pin) can be configured to generate the 16x baud clock. With UEN<1:0> = 11, the UxBCLK pin will output the 16x baud clock if the UARTx module is enabled. It can be used to support the IrDA codec chip.

19.7.2 BUILT-IN IrDA ENCODER AND DECODER

The UARTx has full implementation of the IrDA encoder and decoder as part of the UARTx module. The built-in IrDA encoder and decoder functionality is enabled using the IREN bit (UxMODE<12>). When enabled (IREN = 1), the receive pin (UxRX) acts as the input from the infrared receiver. The transmit pin (UxTX) acts as the output to the infrared transmitter.

REGISTER 23-1: CLCxCONL: CLCx CONTROL REGISTER (LOW) (CONTINUED)

bit 2-0 **MODE<2:0>:** CLCx Mode bits
111 = Single input transparent latch with S and R
110 = JK flip-flop with R
101 = Two-input D flip-flop with R
100 = Single input D flip-flop with S and R
011 = SR latch
010 = Four-input AND
001 = Four-input OR-XOR
000 = Four-input AND-OR

REGISTER 23-2: CLCxCONH: CLCx CONTROL REGISTER (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	G4POL	G3POL	G2POL	G1POL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **G4POL:** Gate 4 Polarity Control bit
1 = Channel 4 logic output is inverted when applied to the logic cell
0 = Channel 4 logic output is not inverted

bit 2 **G3POL:** Gate 3 Polarity Control bit
1 = Channel 3 logic output is inverted when applied to the logic cell
0 = Channel 3 logic output is not inverted

bit 1 **G2POL:** Gate 2 Polarity Control bit
1 = Channel 2 logic output is inverted when applied to the logic cell
0 = Channel 2 logic output is not inverted

bit 0 **G1POL:** Gate 1 Polarity Control bit
1 = Channel 1 logic output is inverted when applied to the logic cell
0 = Channel 1 logic output is not inverted

REGISTER 24-6: RTCSTATL: RTCC STATUS REGISTER (LOW)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/C-0, HSC	R/W-0, HSC	R/W-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
—	—	ALMEVT	TSBEVT(1)	TSAEVT(1)	SYNC	ALMSYNC	HALFSEC(2)
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5 **ALMEVT:** Alarm Event bit
1 = An alarm event has occurred
0 = An alarm event has not occurred

bit 4 **TSBEVT:** Timestamp B Event bit(1)
1 = A Timestamp B event has occurred
0 = A Timestamp B event has not occurred

bit 3 **TSAEVT:** Timestamp A Event bit(1)
1 = A Timestamp A event has occurred
0 = A Timestamp A event has not occurred

bit 2 **SYNC:** Synchronization Status bit
1 = Time registers may change during software read
0 = Time registers may be read safely

bit 1 **ALMSYNC:** Alarm Synchronization Status bit
1 = Alarm registers (ALMTIME, ALMDATE) and AMASKx bits should not be modified and Alarm Control registers (ALRMEN, ALMRPT<7:0>) may change during software read
0 = Alarm registers and Alarm Control registers may be written/modified safely

bit 0 **HALFSEC:** Half Second Status bit(2)
1 = Second half of 1-second period
0 = First half of 1-second period

Note 1: User software may write a '1' to this location to initiate a Timestamp A event; timestamp capture is not valid until TSAEVT reads as '1'.

2: This bit is read-only; it is cleared to '0' on a write to the SECONE<3:0> bits in Register 24-7.

REGISTER 27-5: AD1CON5: A/D CONTROL REGISTER 5

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
ASEN	LPEN	CTMREQ	BGREQ	—	—	ASINT1	ASINT0
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	WM1	WM0	CM1	CM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ASEN:** Auto-Scan Enable bit
1 = Auto-scan is enabled
0 = Auto-scan is disabled

bit 14 **LPEN:** Low-Power Enable bit
1 = Low power is enabled after scan
0 = Full power is enabled after scan

bit 13 **CTMREQ:** CTMU Request bit
1 = CTMU is enabled when the A/D is enabled and active
0 = CTMU is not enabled by the A/D

bit 12 **BGREQ:** Band Gap Request bit
1 = Band gap is enabled when the A/D is enabled and active
0 = Band gap is not enabled by the A/D

bit 11-10 **Unimplemented:** Read as '0'

bit 9-8 **ASINT<1:0>:** Auto-Scan (Threshold Detect) Interrupt Mode bits
11 = Interrupt after Threshold Detect sequence has completed and valid compare has occurred
10 = Interrupt after valid compare has occurred
01 = Interrupt after Threshold Detect sequence has completed
00 = No interrupt

bit 7-4 **Unimplemented:** Read as '0'

bit 3-2 **WM<1:0>:** Write Mode bits
11 = Reserved
10 = Auto-compare only (conversion results are not saved, but interrupts are generated when a valid match occurs, as defined by the CMx and ASINTx bits)
01 = Convert and save (conversion results are saved to locations as determined by the register bits when a match occurs, as defined by the CMx bits)
00 = Legacy operation (conversion data is saved to a location determined by the buffer register bits)

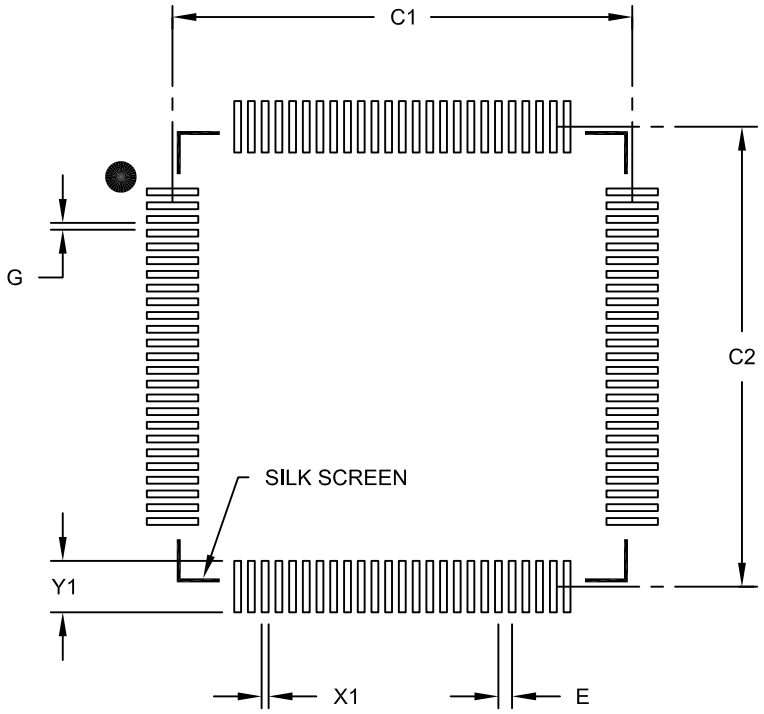
bit 1-0 **CM<1:0>:** Compare Mode bits
11 = Outside Window mode (valid match occurs if the conversion result is outside of the window defined by the corresponding buffer pair)
10 = Inside Window mode (valid match occurs if the conversion result is inside the window defined by the corresponding buffer pair)
01 = Greater Than mode (valid match occurs if the result is greater than the value in the corresponding buffer register)
00 = Less Than mode (valid match occurs if the result is less than the value in the corresponding buffer register)

TABLE 35-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
<n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
bit4	4-bit Bit Selection field (used in word addressed instructions) ∈ {0...15}
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0000h...1FFFh}
lit1	1-bit unsigned literal ∈ {0,1}
lit4	4-bit unsigned literal ∈ {0...15}
lit5	5-bit unsigned literal ∈ {0...31}
lit8	8-bit unsigned literal ∈ {0...255}
lit10	10-bit unsigned literal ∈ {0...255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal ∈ {0...16383}
lit16	16-bit unsigned literal ∈ {0...65535}
lit23	23-bit unsigned literal ∈ {0...8388607}; LSB must be '0'
None	Field does not require an entry, may be blank
PC	Program Counter
Slit10	10-bit signed literal ∈ {-512...511}
Slit16	16-bit signed literal ∈ {-32768...32767}
Slit6	6-bit signed literal ∈ {-16...16}
Wb	Base W register ∈ {W0..W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor Working register pair (direct addressing)
Wn	One of 16 Working registers ∈ {W0..W15}
Wnd	One of 16 Destination Working registers ∈ {W0..W15}
Wns	One of 16 Source Working registers ∈ {W0..W15}
WREG	W0 (Working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws--], [++Ws], [--Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns--], [++Wns], [--Wns], [Wns+Wb] }

100-Lead Plastic Thin Quad Flatpack (PT) - 12x12x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100B

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