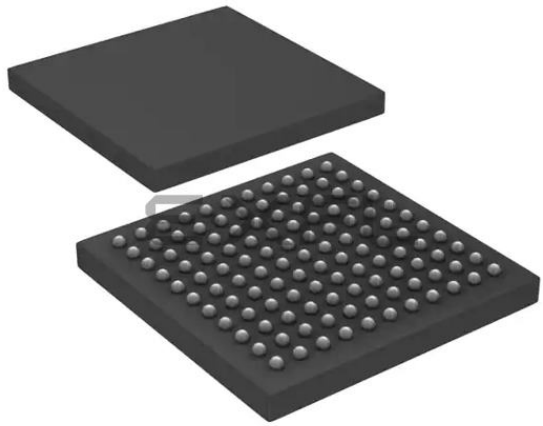
Microchip Technology - PIC24FJ256GA412T-I/BG Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	102
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256ga412t-i-bg

TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS FOR PIC24FJXXXGA410 DEVICES

Pin	Function	Pin	Function
1	SEG50/OCM1C/CTED3/IOCG15/RG15	51	SEG12/**RP16**/IOCF3/RF3
2	VDD	52	SEG40/**RP30**/IOCF2/RF2
3	LCDBIAS2/IC4/CTED4/PMD5/IOCE5/RE5	53	SEG41/**RP15**/IOCF8/RF8
4	LCDBIAS1/SCL3/IC5/PMD6/IOCE6/RE6	54	IOCF7/RF7
5	LCDBIAS0/SDA3/IC6/PMD7/IOCE7/RE7	55	IOCF6/RF6
6	SEG32/**RPI38**/OCM1D/IOCC1/RC1	56	SDA1/IOCG3/RG3
7	SEG51/**RPI39**/IOCC2/RC2	57	SCL1/IOCG2/RG2
8	SEG33/**RPI40**/IOCC3/RC3	58	SEG55/SCL2/IOCA2/RA2
9	SEG52/AN16/**RPI41**/PMCS2/IOCC4/RC4	59	SEG56/SDA2/PMA20/IOCA3/RA3
10	SEG0/AN17/C1IND/**RP21**/ICM1/OCM1A/PMA5/IOCG6/RG6	60	TDI/PMA21/IOCA4/RA4
11	VLCAP1/AN18/C1INC/**RP26**/OCM1B/PMA4/IOCG7/RG7	61	TDO/SEG28/IOCA5/RA5
12	VLCAP2/AN19/C2IND/**RP19**/ICM2/OCM2/PMA3/IOCG8/RG8	62	VDD
13	$\overline{\text{MCLR}}$	63	OSCI/CLKI/IOCC12/RC12
14	SEG1/AN20/C1INC/C2INC/C3INC/**RP27**/DAC1/PMA2/PMALU/IOCG9/RG9	64	OSCO/CLKO/IOCC15/RC15
15	VSS	65	VSS
16	VDD	66	SEG42/**RPI36**/SCL1/PMA22/IOCA14/RA14
17	TMS/SEG48/CTED14/IOCA0/RA0	67	SEG43/**RPI35**/SDA1/PMBE1/IOCA15/RA15
18	SEG34/**RPI33**/PMCS1/IOCE8/RE8	68	SEG13/CLC4OUT/**RP2**/RTCC/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/IOCD8/RD8
19	SEG35/AN21/**RPI34**/PMA19/IOCE9/RE9	69	SEG14/**RP4**/PMACK2/IOCD9/RD9
20	PGEC3/SEG2/AN5/C1INA/**RP18**/ICM3/OCM3/IOCB5/RB5	70	SEG15/C3IND/**RP3**/PMA15/APMCS2/IOCD10/RD10
21	PGED3/SEG3/AN4/C1INB/**RP28**/IOCB4/RB4	71	SEG16/C3INC/**RP12**/PMA14/PMCS/APMCS1/IOCD11/RD11
22	SEG4/AN3/C2INA/IOCB3/RB3	72	SEG17/CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/IOCD0/RD0
23	SEG5/AN2/CTCMP/C2INB/**RP13**/CTED13/IOCB2/RB2	73	SOSCI/IOCC13/RC13
24	PGEC1/SEG6/VREF-/CVREF-/AN1/AN1-/**RP1**/CTED12/IOCB1/RB1	74	SOSCO/SCLKI/**RPI37**/PWRLCLK/IOCC14/RC14
25	PGED1/SEG7/VREF+/CVREF+/DVREF+/AN0/**RP0**/IOCB0/RB0	75	VSS
26	PGEC2/LCDBIAS3/AN6/**RP6**/IOCB6/RB6	76	SEG20/**RP24**/U5TX/ICM4/IOCD1/RD1
27	PGED2/SEG63/AN7/**RP7**/U6TX/IOCB7/RB7	77	SEG21/**RP23**/PMACK1/IOCD2/RD2
28	SEG36/VREF-/CVREF-/PMA7/IOCA9/RA9	78	SEG22/**RP22**/ICM7/PMBE0/IOCD3/RD3
29	SEG37/VREF+/CVREF+/DVREF+/PMA6/IOCA10/RA10	79	SEG44/**RPI42**/PMD12/IOCD12/RD12
30	AVDD	80	SEG45/PMD13/IOCD13/RD13
31	AVSS	81	SEG23/**RP25**/PMWR/PMENB/IOCD4/RD4
32	COM7/SEG31/AN8/**RP8**/PWRGT/IOCB8/RB8	82	SEG24/**RP20**/PMRD/$\overline{\text{PMWR}}$/IOCD5/RD5
33	COM6/SEG30/AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/IOCB9/RB9	83	SEG25/C3INB/U5RX/OC4/PMD14/IOCD6/RD6
34	COM5/SEG29/CVREF/AN10/SDO4/PMA13/IOCB10/RB10	84	SEG26/C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/PMD15/IOCD7/RD7
35	AN11/REFI1/$\overline{\text{SS4}}$/FSYNC4/PMA12/IOCB11/RB11	85	VCAP
36	VSS	86	VBAT
37	VDD	87	SEG27/$\overline{\text{U5CTS}}$/OC6/PMD11/IOCF0/RF0
38	TCK/IOCA1/RA1	88	COM4/SEG47/SCK4/PMD10/IOCF1/RF1
39	SEG53/**RP31**/IOCF13/RF13	89	SEG46/PMD9/IOCG1/RG1
40	SEG54/**RPI32**/CTED7/PMA18/IOCF12/RF12	90	SEG49/PMD8/IOCG0/RG0
41	SEG18/AN12/U6RX/CTED2/PMA11/IOCB12/RB12	91	SEG57/AN23/OCM1E/IOCA6/RA6
42	SEG19/AN13/SDI4/CTED1/PMA10/IOCB13/RB13	92	SEG58/AN22/OCM1F/PMA17/IOCA7/RA7
43	SEG8/AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/IOCB14/RB14	93	COM3/PMD0/IOCE0/RE0
44	SEG9/AN15/**RP29**/CTED6/PMA0/PMALL/IOCB15/RB15	94	COM2/PMD1/IOCE1/RE1
45	VSS	95	SEG59/CTED11/PMA16/IOCG14/RG14
46	VDD	96	SEG60/IOCG12/RG12
47	SEG38/**RPI43**/IOCD14/RD14	97	SEG61/CTED10/IOCG13/RG13
48	SEG39/**RP5**/IOCD15/RD15	98	COM1/PMD2/IOCE2/RE2
49	SEG10/**RP10**/PMA9/IOCF4/RF4	99	COM0/CTED9/PMD3/IOCE3/RE3
50	SEG11/**RP17**/PMA8/IOCF5/RF5	100	SEG62/LVDIN/CTED8/PMD4/IOCE4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

1.1.4 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC24FJ256GA412/GB412 family offer five different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes
- Two External Clock modes
- A Phase-Locked Loop (PLL) frequency multiplier, which allows clock speeds of up to 32 MHz
- A Fast Internal Oscillator (FRC) – nominal 8 MHz output with multiple frequency divider options and automatic frequency self-calibration during run time
- A separate Low-Power Internal RC Oscillator (LPRC) – 31 kHz nominal for low-power, timing-insensitive applications.

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor (FSCM). This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

1.1.5 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve. This extends the ability of applications to grow from the relatively simple, to the powerful and complex, while still selecting a Microchip device.

1.2 Cryptographic Engine

The Cryptographic Engine provides a new set of data security options. Using its own free-standing math engine, the module can independently perform NIST standard encryption and decryption of data, independently of the CPU. The Cryptographic Engine supports AES and DES/3DES encryption ciphers in up to 5 modes, and supports key lengths from 128 to 256 bits. Additional features include True Random Number Generation (TRNG) within the engine, multiple encryption/decryption key storage options and secure data handling that prevents data in the engine from being compromised by external reads.

1.3 USB On-The-Go (OTG)

USB On-The-Go provides on-chip functionality as a target device compatible with the USB 2.0 standard, as well as limited stand-alone functionality as a USB embedded host. By implementing USB Host Negotiation Protocol (HNP), the module can also dynamically switch between device and host operation, allowing for a much wider range of versatile USB-enabled applications on a microcontroller platform.

PIC24FJ256GA412/GB412 family devices also incorporate an integrated USB transceiver and precision oscillator, minimizing the required complexity of implementing a complete USB device, embedded host, dual role or On-The-Go application.

1.4 DMA Controller

PIC24FJ256GA412/GB412 family devices also add a Direct Memory Access (DMA) Controller to the existing PIC24F architecture. The DMA acts in concert with the CPU, allowing data to move between data memory and peripherals without the intervention of the CPU, increasing data throughput and decreasing execution time overhead. Six independently programmable channels make it possible to service multiple peripherals at virtually the same time, with each channel peripheral performing a different operation. Many types of data transfer operations are supported.

1.5 LCD Controller

The versatile on-chip LCD Controller includes many features that make the integration of displays in low-power applications easier. These include an integrated voltage regulator with charge pump and an integrated internal resistor ladder that allows contrast control in software, and display operation above device V_{DD}.

TABLE 1-3: DEVICE FEATURES FOR THE PIC24FJ256GA412/GB412 FAMILY: 121-PIN

Features	PIC24FJXXXGA/GB412					
	64GA	128GA	256GA	64GB	128GB	256GB
Operating Frequency	DC – 32 MHz					
Program Memory (bytes)	64K	128K	256K	64K	128K	256K
Program Memory (instructions)	22,016	44,032	88,064	22,016	44,032	88,064
Data Memory (bytes)	8K	16K		8K	16K	
Interrupt Sources (soft vectors/ NMI traps)	113 (107/6)					
I/O Ports	Ports A, B, C, D, E, F, G, H, J					
Total I/O Pins	102			101		
Remappable Pins	44 (32 I/O, 12 input only)					
Timers:						
Total Number (16-bit)	19(1,2)					
32-Bit (from paired 16-bit timers)	9					
Input Capture w/Timer Channels	6(2)					
Output Compare/PWM Channels	6(2)					
Single Output CCP (SCCP)	6					
Multiple Output CCP (MCCP)	1					
Serial Communications:						
UART	6(2)					
SPI (3-wire/4-wire)	4(2)					
I^2C	3					
USB On-The-Go	No			Yes		
Cryptographic Engine	Yes					
Parallel Communications (EPMP/PSP)	Yes					
10/12-Bit Analog-to-Digital Converter (A/D) (input channels)	24					
Digital-to-Analog Converter (DAC)	1					
Analog Comparators	3					
CTMU Interface	Yes					
LCD Controller (available pixels)	512 (64 SEG x 8 COM)					
JTAG Boundary Scan	Yes					
Resets (and delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)					
Instruction Set	77 Base Instructions, Multiple Addressing Mode Variations					
Packages	121-Pin TFBGA					

Note 1: Includes the Timer modes of SCCP and MCCP modules.

2: Some instantiations of these modules are only available through remappable pins.

TABLE 1-5: PIC24FJ256GB412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
SEG0	4	10	E3	O	ANA	LCD Driver Segment Outputs
SEG1	8	14	F3	O	ANA	
SEG2	11	20	H1	O	ANA	
SEG3	12	21	H2	O	ANA	
SEG4	13	22	J1	O	ANA	
SEG5	14	23	J2	O	ANA	
SEG6	15	24	K1	O	ANA	
SEG7	16	25	K2	O	ANA	
SEG8	29	43	K7	O	ANA	
SEG9	30	44	L8	O	ANA	
SEG10	31	49	L10	O	ANA	
SEG11	32	50	L11	O	ANA	
SEG12	33	51	K10	O	ANA	
SEG13	42	68	E9	O	ANA	
SEG14	43	69	E10	O	ANA	
SEG15	44	70	D11	O	ANA	
SEG16	45	71	C11	O	ANA	
SEG17	46	72	D9	O	ANA	
SEG18	27	41	J7	O	ANA	
SEG19	28	42	L7	O	ANA	
SEG20	49	76	A11	O	ANA	
SEG21	50	77	A10	O	ANA	
SEG22	51	78	B9	O	ANA	
SEG23	52	81	C8	O	ANA	
SEG24	53	82	B8	O	ANA	
SEG25	54	83	D7	O	ANA	
SEG26	55	84	C7	O	ANA	
SEG27	58	87	B6	O	ANA	
SEG28	—	61	G9	O	ANA	
SEG29	23	34	H5	O	ANA	
SEG30	22	33	L4	O	ANA	
SEG31	21	32	K4	O	ANA	
SEG32	—	6	D1	O	ANA	
SEG33	—	8	E2	O	ANA	
SEG34	—	18	G1	O	ANA	
SEG35	—	19	G2	O	ANA	
SEG36	—	28	L2	O	ANA	
SEG37	—	29	K3	O	ANA	
SEG38	—	47	L9	O	ANA	
SEG39	—	48	K9	O	ANA	
SEG40	—	52	K11	O	ANA	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

3.3 Arithmetic Logic Unit (ALU)

The PIC24F ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. Depending on the operation, the ALU may affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array, or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

The PIC24F CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.3.1 MULTIPLIER

The ALU contains a high-speed, 17-bit x 17-bit multiplier. It supports unsigned, signed or mixed sign operation in several multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.3.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

1. 32-bit signed/16-bit signed divide
2. 32-bit unsigned/16-bit unsigned divide
3. 16-bit signed/16-bit signed divide
4. 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. The 16-bit signed and unsigned `DIV` instructions can specify any W register for both the 16-bit divisor (Wn), and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.3.3 MULTIBIT SHIFT SUPPORT

The PIC24F ALU supports both single bit and single-cycle, multibit arithmetic and logic shifts. Multibit shifts are implemented using a shifter block, capable of performing up to a 15-bit arithmetic right shift, or up to a 15-bit left shift, in a single cycle. All multibit shift instructions only support Register Direct Addressing for both the operand source and result destination.

A full summary of instructions that use the shift operation is provided in Table 3-2.

TABLE 3-2: INSTRUCTIONS THAT USE THE SINGLE BIT AND MULTIBIT SHIFT OPERATION

Instruction	Description
ASR	Arithmetic Shift Right Source register by one or more bits.
SL	Shift Left Source register by one or more bits.
LSR	Logical Shift Right Source register by one or more bits.

4.0 MEMORY ORGANIZATION

As Harvard architecture devices, PIC24F microcontrollers feature separate program and data memory spaces and buses. This architecture also allows direct access of program memory from the Data Space (DS) during code execution.

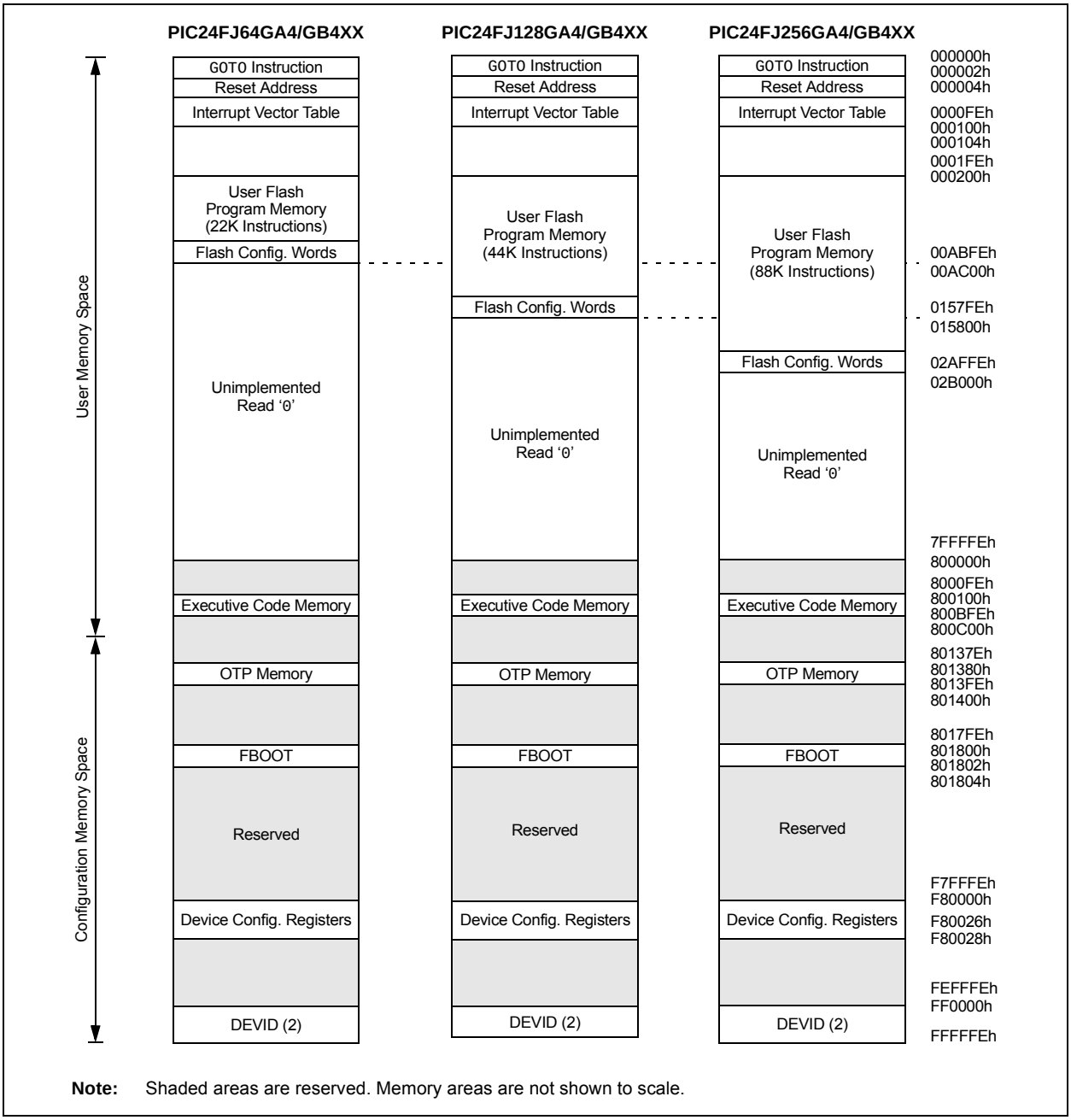
4.1 Program Memory Space

The program address memory space of the PIC24FJ256GA412/GB412 family devices is 4M instructions. The space is addressable by a 24-bit value derived from either the 23-bit Program Counter (PC) during program execution, or from table operation or Data Space remapping, as described in **Section 4.4 "Interfacing Program and Data Memory Spaces"**.

User access to the program memory space is restricted to the lower half of the address range (000000h to 7FFFFFh). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

Memory maps for PIC24FJ256GA412/GB412 family devices are shown in Figure 4-1.

FIGURE 4-1: DEFAULT PROGRAM MEMORY MAPS FOR PIC24FJ256GA412/GB412 FAMILY



Note: Shaded areas are reserved. Memory areas are not shown to scale.

4.4.3 READING DATA FROM PROGRAM MEMORY USING EDS

The upper 32 Kbytes of Data Space may optionally be mapped into any 16K word page of the program space. This provides transparent access of stored constant data from the Data Space without the need to use special instructions (i.e., TBLRDL/H).

Program space access through the Data Space occurs when the MSb of EA is '1' and the DSRPAG<9> is also '1'. The lower 8 bits of DSRPAG are concatenated to the Wn<14:0> bits to form a 23-bit EA to access program memory. The DSRPAG<8> decides which word should be addressed; when the bit is '0', the lower word and when '1', the upper word of the program memory is accessed.

The entire program memory is divided into 512 EDS pages, from 200h to 3FFh, each consisting of 16K words of data. Pages, 200h to 2FFh, correspond to the lower words of the program memory, while 300h to 3FFh correspond to the upper words of the program memory.

Using this EDS technique, the entire program memory can be accessed. Previously, the access to the upper word of the program memory was not supported.

Table 4-16 provides the corresponding 23-bit EDS address for program memory with EDS page and source addresses.

For operations that use PSV, and are executed outside a REPEAT loop, the MOV and MOV.D instructions will require one instruction cycle in addition to the specified execution time. All other instructions will require two instruction cycles in addition to the specified execution time.

For operations that use PSV, which are executed inside a REPEAT loop, there will be some instances that require two instruction cycles in addition to the specified execution time of the instruction:

- Execution in the first iteration
- Execution in the last iteration
- Execution prior to exiting the loop due to an interrupt
- Execution upon re-entering the loop after an interrupt is serviced

Any other iteration of the REPEAT loop will allow the instruction accessing data, using PSV, to execute in a single cycle.

TABLE 4-16: EDS PROGRAM ADDRESS WITH DIFFERENT PAGES AND ADDRESSES

DSRPAG (Data Space Read Register)	Source Address While Indirect Addressing	23-Bit EA Pointing to EDS	Comment
200h • • • 2FFh	8000h to FFFFh	000000h to 007FFEh • • • 7F8000h to 7FFFFEh	Lower words of 4M program instructions; (8 Mbytes) for read operations only
300h • • • 3FFh		000001h to 007FFFh • • • 7F8001h to 7FFFFFh	Upper words of 4M program instructions (4 Mbytes remaining, 4 Mbytes are phantom bytes); for read operations only
000h		Invalid Address	Address error trap(1)

Note 1: When the source/destination address is above 8000h and DSRPAG/DSWPAG are '0', an address error trap will occur.

EXAMPLE 4-3: EDS READ CODE FROM PROGRAM MEMORY IN ASSEMBLY

```
; Set the EDS page from where the data to be read
    mov     #0x0202, w0
    mov     w0, DSRPAG                ;page 0x202, consisting lower words, is selected for read
    mov     #0x000A, w1               ;select the location (0x0A) to be read
    bset    w1, #15                   ;set the MSB of the base address, enable EDS mode
;Read a byte from the selected location
    mov.b   [w1++], w2                ;read Low byte
    mov.b   [w1++], w3                ;read High byte
;Read a word from the selected location
    mov     [w1], w2                  ;
;Read Double - word from the selected location
    mov.d   [w1], w2                  ;two word read, stored in w2 and w3
```

REGISTER 8-33: IPC11: INTERRUPT PRIORITY CONTROL REGISTER 11

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CCT5IP2	CCT5IP1	CCT5IP0	—	DMA4IP2	DMA4IP1	DMA4IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	PMIP2	PMIP1	PMIP0	—	CCT4IP2	CCT4IP1	CCT4IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **CCT5IP<2:0>:** SCCP5 Timer Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 10-8 **DMA4IP<2:0>:** DMA Channel 4 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **PMIP<2:0>:** Parallel Master Port Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **CCT4IP<2:0>:** SCCP4 Timer Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-36: IPC14: INTERRUPT PRIORITY CONTROL REGISTER 14

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPI2RXIP2	SPI2RXIP1	SPI2RXIP0	—	SPI1RXIP2	SPI1RXIP1	SPI1RXIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPI4RXIP2	SPI4RXIP1	SPI4RXIP0	—	KEYSTRIP2	KEYSTRIP1	KEYSTRIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **SPI2RXIP<2:0>:** SPI2 Receive Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **SPI1RXIP<2:0>:** SPI1 Receive Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SPI4RXIP<2:0>:** SPI4 Receive Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **KEYSTRIP<2:0>:** Cryptographic Key Store Program Done Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 10-11: PMD8: PERIPHERAL MODULE DISABLE REGISTER 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
U6MD	U5MD	CLC4MD	CLC3MD	CLC2MD	CLC1MD	—	CRYMD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **U6MD:** UART6 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 6 **U5MD:** UART5 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 5 **CLC4MD:** CLC4 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 4 **CLC3MD:** CLC3 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 3 **CLC2MD:** CLC2 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 2 **CLC1MD:** CLC1 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **CRYMD:** Cryptographic Engine Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

REGISTER 11-1: PADCON: PORT CONFIGURATION REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
IOCON	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PMTTL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **IOCON:** Interrupt-on-Change Enable bit
1 = Interrupt-on-change functionality is enabled
0 = Interrupt-on-change functionality is disabled

bit 14-1 **Unimplemented:** Read as ‘0’

bit 0 **PMTTL:** EPMP Module TTL Input Buffer Select bit (unused by the GPIO module)
Not used by IOC; see Register 21-9 for definition.

REGISTER 17-2: SPIxCON1H: SPIx CONTROL REGISTER 1 HIGH (CONTINUED)

bit 6 **FRMSYNC:** Frame Sync Pulse Direction Control bit
1 = Frame Sync pulse input (slave)
0 = Frame Sync pulse output (master)

bit 5 **FRMPOL:** Frame Sync/Slave Select Polarity bit
1 = Frame Sync pulse/slave select is active-high
0 = Frame Sync pulse/slave select is active-low

bit 4 **MSSEN:** Master Mode Slave Select Enable bit
1 = SPIx slave select support is enabled with polarity determined by FRMPOL ($\overline{SSx}$ pin is automatically driven during transmission in Master mode)
0 = Slave select SPIx support is disabled ($\overline{SSx}$ pin will be controlled by port IO)

bit 3 **FRMSYPW:** Frame Sync Pulse-Width bit
1 = Frame Sync pulse is one serial word length wide (as defined by MODE<32,16>/WLENGTH<4:0>)
0 = Frame Sync pulse is one clock (SCK) wide

bit 2-0 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits
Controls the number of serial words transmitted per Sync pulse.
111 = Reserved
110 = Reserved
101 = Generates a Frame Sync pulse on every 32 serial words
100 = Generates a Frame Sync pulse on every 16 serial words
011 = Generates a Frame Sync pulse on every 8 serial words
010 = Generates a Frame Sync pulse on every 4 serial words
001 = Generates a Frame Sync pulse on every 2 serial words (value used by audio protocols)
000 = Generates a Frame Sync pulse on each serial word

Note 1: AUDEN can only be written when the SPIEN bit = 0.
2: AUDMONO can only be written when the SPIEN bit = 0 and is only valid for AUDEN = 1.
3: URDTEN is only valid when IGNTUR = 1.
4: AUDMOD<1:0> can only be written when the SPIEN bit = 0 and is only valid when AUDEN = 1. When NOT in PCM/DSP mode, this module functions as if FRMSYPW = 1, regardless of its actual value.

NOTES:

24.0 REAL-TIME CLOCK AND CALENDAR (RTCC) WITH TIMESTAMP

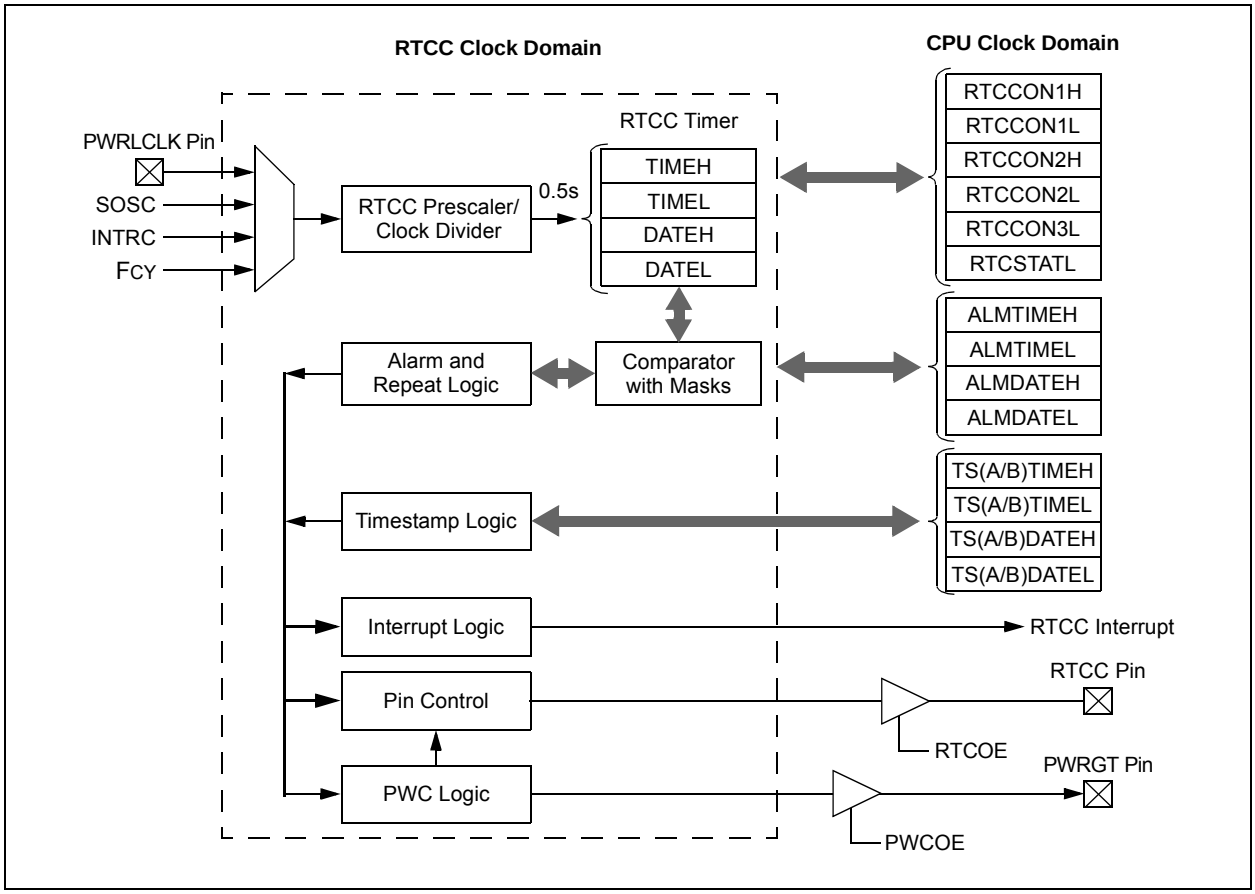
Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Real-Time Clock and Calendar, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"RTCC with Timestamp"** (DS70005193). The information in this data sheet supersedes the information in the FRM.

The RTCC provides the user with a Real-Time Clock and Calendar (RTCC) function that can be calibrated.

Key features of the RTCC module are:

- Time (Hours, Minutes and Seconds) in 24-Hour (Military Time) Format
- Calendar (Weekday, Date, Month and Year)
  - Year range from 2000 to 2099 with automatic Leap Year correction
- Alarm with Configurable Mask and Repeat Options
- BCD Format for Compact Firmware
- Optimized for Low-Power Operation
- Multiple Clock Input Options, Including:
  - 32.768 kHz crystal
  - External Real-Time Clock (RTC)
  - 50/60 Hz power line clock
  - 31.25 kHz LPRC clock
  - System clock, up to 32 MHz
- User Calibration with a Range of 2 ppm when using 32 kHz Source
- Interrupt on Alarm and Timestamp Events
- Optional Timestamp Capture for Tamper Pin or Other Events
- User-Configurable Power Control with Dedicated Output Pin to Periodically Wake External Devices

FIGURE 24-1: RTCC HIGH-LEVEL BLOCK DIAGRAM



REGISTER 26-2: CRCCON2: CRC CONTROL REGISTER 2

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DWIDTH4	DWIDTH3	DWIDTH2	DWIDTH1	DWIDTH0
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	PLEN4	PLEN3	PLEN2	PLEN1	PLEN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-8 **DWIDTH<4:0>:** Data Word Width Configuration bits
Configures the width of the data word (Data Word Width – 1).

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **PLEN<4:0>:** Polynomial Length Configuration bits
Configures the length of the polynomial (Polynomial Length – 1).

REGISTER 27-1: AD1CON1: A/D CONTROL REGISTER 1 (CONTINUED)

bit 7-4 **SSRC<3:0>:** Sample Clock Source Select bits
1xxx = Unimplemented, do not use
0111 = Internal counter ends sampling and starts conversion (auto-convert); do not use in Auto-Scan mode
0110 = Timer1 (also triggers in Sleep mode)
0101 = Timer1 (does not trigger in Sleep mode)
0100 = CTMU
0011 = Timer5
0010 = Timer3
0001 = INT0
0000 = The SAMP bit must be cleared by software to start conversion

bit 3 **Unimplemented:** Read as '0'

bit 2 **ASAM:** A/D Sample Auto-Start bit
1 = Sampling begins immediately after the last conversion; SAMP bit is auto-set
0 = Sampling begins when SAMP bit is manually set

bit 1 **SAMP:** A/D Sample Enable bit
1 = A/D Sample-and-Hold amplifiers are sampling
0 = A/D Sample-and-Hold amplifiers are holding

bit 0 **DONE:** A/D Conversion Status bit
1 = A/D conversion cycle has completed
0 = A/D conversion cycle has not started or is in progress

Note 1: This bit is only available when Extended DMA/Buffer features are available (DMAEN = 1).

TABLE 35-2: INSTRUCTION SET OVERVIEW

Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
ADD	ADD	f	f = f + WREG	1	1	C, DC, N, OV, Z
	ADD	f,WREG	WREG = f + WREG	1	1	C, DC, N, OV, Z
	ADD	#lit10,Wn	Wd = lit10 + Wd	1	1	C, DC, N, OV, Z
	ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1	C, DC, N, OV, Z
	ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C, DC, N, OV, Z
ADDC	ADDC	f	f = f + WREG + (C)	1	1	C, DC, N, OV, Z
	ADDC	f,WREG	WREG = f + WREG + (C)	1	1	C, DC, N, OV, Z
	ADDC	#lit10,Wn	Wd = lit10 + Wd + (C)	1	1	C, DC, N, OV, Z
	ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C, DC, N, OV, Z
	ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C, DC, N, OV, Z
AND	AND	f	f = f .AND. WREG	1	1	N, Z
	AND	f,WREG	WREG = f .AND. WREG	1	1	N, Z
	AND	#lit10,Wn	Wd = lit10 .AND. Wd	1	1	N, Z
	AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N, Z
	AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N, Z
ASR	ASR	f	f = Arithmetic Right Shift f	1	1	C, N, OV, Z
	ASR	f,WREG	WREG = Arithmetic Right Shift f	1	1	C, N, OV, Z
	ASR	Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C, N, OV, Z
	ASR	Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N, Z
	ASR	Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N, Z
BCLR	BCLR	f,#bit4	Bit Clear f	1	1	None
	BCLR	Ws,#bit4	Bit Clear Ws	1	1	None
BRA	BRA	C,Expr	Branch if Carry	1	1 (2)	None
	BRA	GE,Expr	Branch if Greater than or Equal	1	1 (2)	None
	BRA	GEU,Expr	Branch if Unsigned Greater than or Equal	1	1 (2)	None
	BRA	GT,Expr	Branch if Greater than	1	1 (2)	None
	BRA	GTU,Expr	Branch if Unsigned Greater than	1	1 (2)	None
	BRA	LE,Expr	Branch if Less than or Equal	1	1 (2)	None
	BRA	LEU,Expr	Branch if Unsigned Less than or Equal	1	1 (2)	None
	BRA	LT,Expr	Branch if Less than	1	1 (2)	None
	BRA	LTU,Expr	Branch if Unsigned Less than	1	1 (2)	None
	BRA	N,Expr	Branch if Negative	1	1 (2)	None
	BRA	NC,Expr	Branch if Not Carry	1	1 (2)	None
	BRA	NN,Expr	Branch if Not Negative	1	1 (2)	None
	BRA	NOV,Expr	Branch if Not Overflow	1	1 (2)	None
	BRA	NZ,Expr	Branch if Not Zero	1	1 (2)	None
	BRA	OV,Expr	Branch if Overflow	1	1 (2)	None
	BRA	Expr	Branch Unconditionally	1	2	None
	BRA	Z,Expr	Branch if Zero	1	1 (2)	None
	BRA	Wn	Computed Branch	1	2	None
BSET	BSET	f,#bit4	Bit Set f	1	1	None
	BSET	Ws,#bit4	Bit Set Ws	1	1	None
BSW	BSW.C	Ws,Wb	Write C bit to Ws<Wb>	1	1	None
	BSW.Z	Ws,Wb	Write Z bit to Ws<Wb>	1	1	None
BTG	BTG	f,#bit4	Bit Toggle f	1	1	None
	BTG	Ws,#bit4	Bit Toggle Ws	1	1	None
BTSC	BTSC	f,#bit4	Bit Test f, Skip if Clear	1	1 (2 or 3)	None
	BTSC	Ws,#bit4	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None

FIGURE 36-6: INPUT CAPTURE x TIMINGS

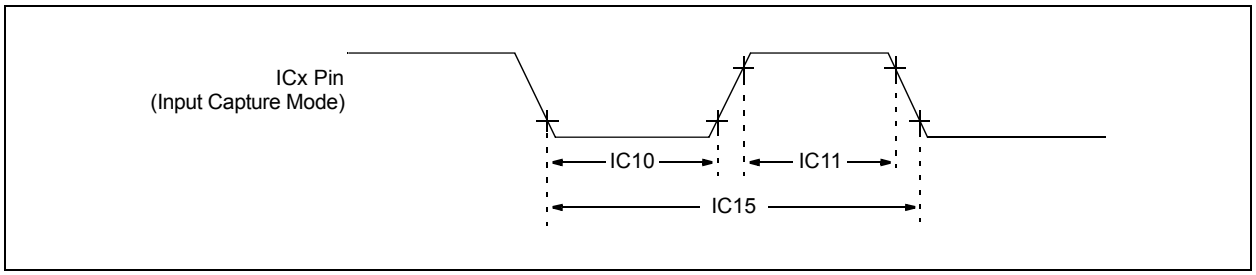


TABLE 36-27: INPUT CAPTURE x TIMINGS REQUIREMENTS

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
IC10	TccL	ICx Input Low Time – Synchronous Timer	No Prescaler	TCY + 20	—	ns	Must also meet Parameter IC15
			With Prescaler	20	—	ns	
IC11	TccH	ICx Input Low Time – Synchronous Timer	No Prescaler	TCY + 20	—	ns	Must also meet Parameter IC15
			With Prescaler	20	—	ns	
IC15	TccP	ICx Input Period – Synchronous Timer		$\frac{2 * T_{CY} + 40}{N}$	—	ns	N = Prescale Value (1, 4, 16)

FIGURE 36-7: OUTPUT COMPARE x TIMINGS

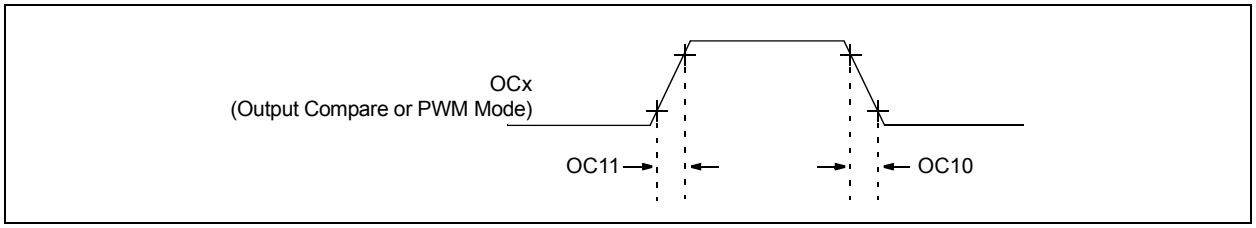


TABLE 36-28: OUTPUT COMPARE 1 TIMINGS

Param. No.	Symbol	Characteristic	Min	Max	Unit	Condition
OC11	TccR	OC1 Output Rise Time	—	10	ns	
			—	—	ns	
OC10	TccF	OC1 Output Fall Time	—	10	ns	
			—	—	ns	

FIGURE 36-16: SPIx MODULE SLAVE MODE TIMING CHARACTERISTICS (CKE = 1)

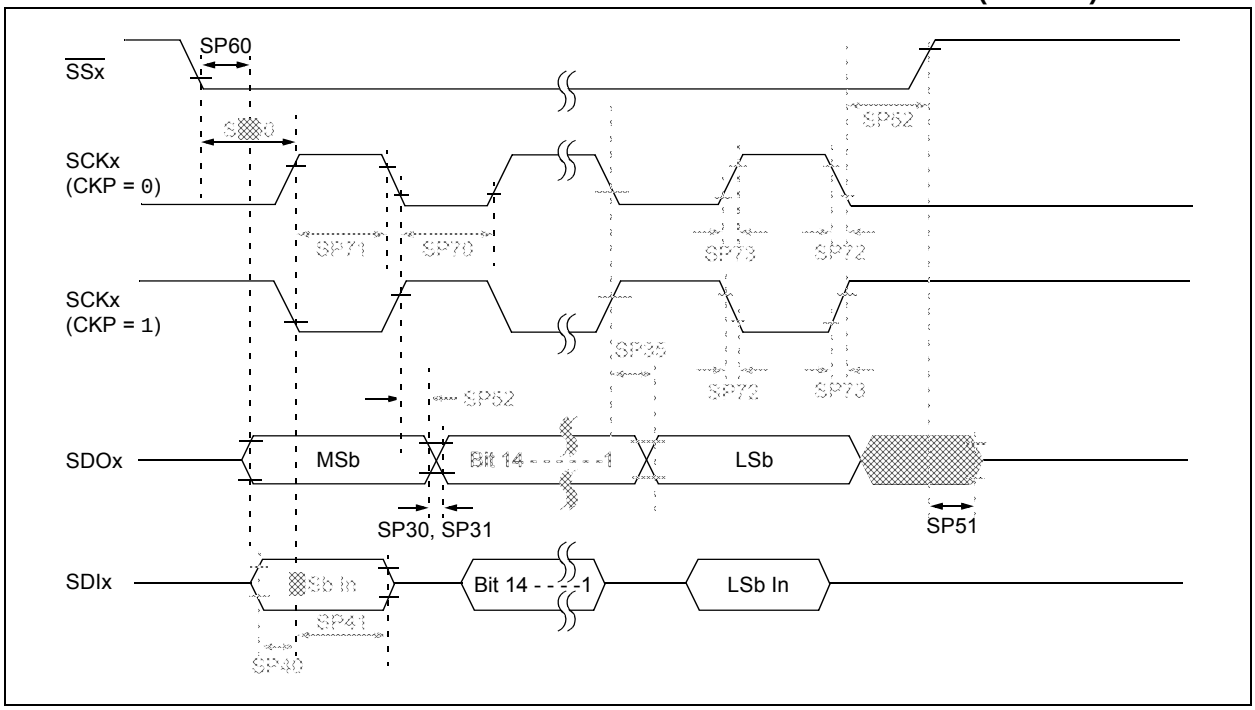


TABLE 36-37: SPIx MODULE SLAVE MODE TIMING REQUIREMENTS (CKE = 1)

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time	30	—	—	ns	
SP71	TscH	SCKx Input High Time	30	—	—	ns	
SP72	TscF	SCKx Input Fall Time(2)	—	10	25	ns	
SP73	TscR	SCKx Input Rise Time(2)	—	10	25	ns	
SP30	TdoF	SDOx Data Output Fall Time(2)	—	10	25	ns	
SP31	TdoR	SDOx Data Output Rise Time(2)	—	10	25	ns	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	—	30	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance(3)	10	—	50	ns	
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ After SCKx Edge	1.5 TCY + 40	—	—	ns	
SP60	TssL2doV	SDOx Data Output Valid After $\overline{SSx}$ Edge	—	—	50	ns	

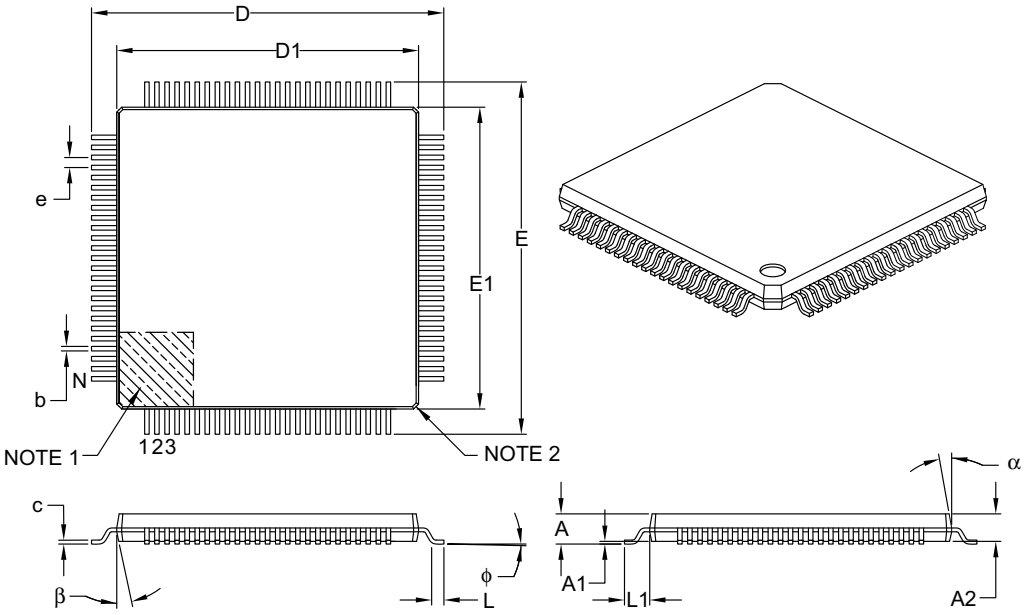
Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The minimum clock period for SCKx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

3: Assumes 50 pF load on all SPIx pins.

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		100	
Lead Pitch	e		0.40 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.13	0.18	0.23
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B