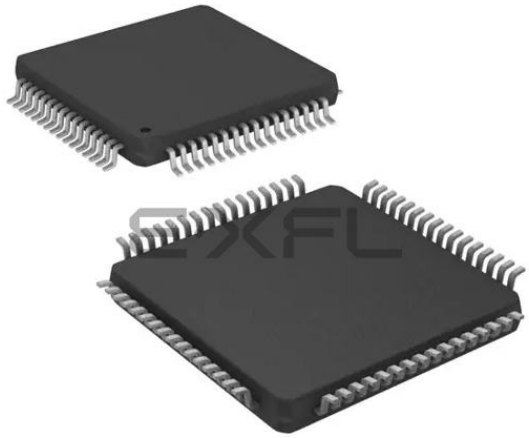

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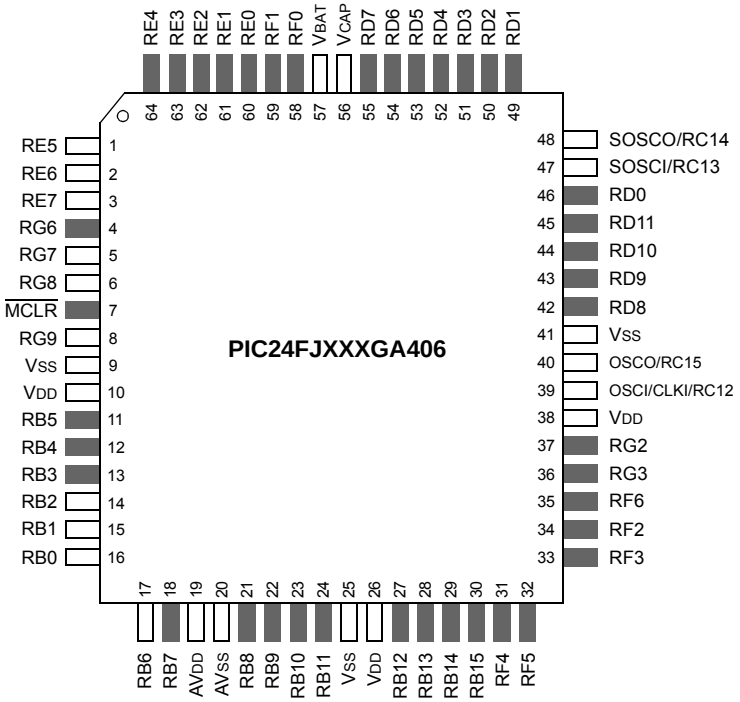
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256gb406t-i-pt

Pin Diagrams

64-Pin TQFP
64-Pin QFN(1)



Legend: **Shaded pins** indicate pins tolerant to up to +5.5 VDC. See Table 1 for a complete description of pin functions.
Note 1: It is recommended to connect the metal pad on the bottom of the 64-pin QFN package to VSS.

TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS FOR PIC24FJXXXGB406 DEVICES

Pin	Function	Pin	Function
1	LCDBIAS2/IC4/CTED4/PMD5/IOCE5/RE5	33	SEG12/**RP16**/USBID/IOCF3/RF3
2	LCDBIAS1/SCL3/IC5/PMD6/IOCE6/RE6	34	VBUS/IOCF7/RF7
3	LCDBIAS0/SDA3/IC6/PMD7/IOCE7/RE7	35	VUSB3V3
4	SEG0/C1IND/**RP21**/ICM1/OCM1A/PMA5/IOCG6/RG6	36	D-/IOCG3/RG3
5	VLCAP1/C1INC/**RP26**/OCM1B/PMA4/IOCG7/RG7	37	D+/IOCG2/RG2
6	VLCAP2/C2IND/**RP19**/ICM2/OCM2/PMA3/IOCG8/RG8	38	VDD
7	$\overline{\text{MCLR}}$	39	OSCI/CLKI/IOCC12/RC12
8	SEG1/C1INC/C2INC/C3INC/**RP27**/DAC1/PMA2/PMALU/IOCG9/RG9	40	OSCO/CLKO/IOCC15/RC15
9	VSS	41	VSS
10	VDD	42	SEG13/CLC4OUT/**RP2**/RTCC/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/IOCD8/RD8
11	PGEC3/SEG2/AN5/C1INA/**RP18**/ICM3/OCM3/IOCB5/RB5	43	SEG14/**RP4**/SDA1/PMACK2/IOCD9/RD9
12	PGED3/SEG3/AN4/C1INB/**RP28**/$\overline{\text{USBOEN}}$/IOCB4/RB4	44	SEG15/C3IND/**RP3**/SCL1/PMA15/APMCS2/IOCD10/RD10
13	SEG4/AN3/C2INA/IOCB3/RB3	45	SEG16/C3INC/**RP12**/PMA14/PMCS/APMCS1/IOCD11/RD11
14	SEG5/AN2/CTCMP/C2INB/**RP13**/CTED13/IOCB2/RB2	46	SEG17/CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/IOCD0/RD0
15	PGEC1/SEG6/VREF-/CVREF-/AN1/AN1-/**RP1**/CTED12/IOCB1/RB1	47	SOSCI/IOCC13/RC13
16	PGED1/SEG7/VREF+/CVREF+/DVREF+/AN0/**RP0**/PMA6/IOCB0/RB0	48	SOSCO/SCLKI/**RPI37**/PWRLCLK/IOCC14/RC14
17	PGEC2/LCDBIAS3/AN6/**RP6**/IOCB6/RB6	49	SEG20/**RP24**/U5TX/ICM4/IOCD1/RD1
18	PGED2/SEG63/AN7/**RP7**/U6TX/IOCB7/RB7	50	SEG21/**RP23**/PMACK1/IOCD2/RD2
19	AVDD	51	SEG22/**RP22**/ICM7/PMBE0/IOCD3/RD3
20	AVSS	52	SEG23/**RP25**/PMWR/PMENB/IOCD4/RD4
21	COM7/SEG31/AN8/**RP8**/PWRGT/IOCB8/RB8	53	SEG24/**RP20**/PMRD/$\overline{\text{PMWR}}$/IOCD5/RD5
22	COM6/SEG30/AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/PMA7/IOCB9/RB9	54	SEG25/C3INB/U5RX/OC4/IOCD6/RD6
23	TMS/COM5/SEG29/CVREF/AN10/SDO4/PMA13/IOCB10/RB10	55	SEG26/C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/IOCD7/RD7
24	TDO/AN11/REFI1/$\overline{\text{SS4}}$/FSYNC4/PMA12/IOCB11/RB11	56	VCAP
25	VSS	57	VBAT
26	VDD	58	SEG27/$\overline{\text{U5CTS}}$/OC6/IOCF0/RF0
27	TCK/SEG18/AN12/U6RX/CTED2/PMA11/IOCB12/RB12	59	COM4/SEG47/SCK4/IOCF1/RF1
28	TDI/SEG19/AN13/SDI4/CTED1/PMA10/IOCB13/RB13	60	COM3/PMD0/IOCE0/RE0
29	SEG8/AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/IOCB14/RB14	61	COM2/PMD1/IOCE1/RE1
30	SEG9/AN15/**RP29**/CTED6/PMA0/PMALL/IOCB15/RB15	62	COM1/PMD2/IOCE2/RE2
31	SEG10/**RP10**/SDA2/PMA9/IOCF4/RF4	63	COM0/CTED9/PMD3/IOCE3/RE3
32	SEG11/SCL2/PMA8/IOCF5/RF5	64	SEG62/LVDIN/CTED8/PMD4/IOCE4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

FIGURE 3-1: PIC24F CPU CORE BLOCK DIAGRAM

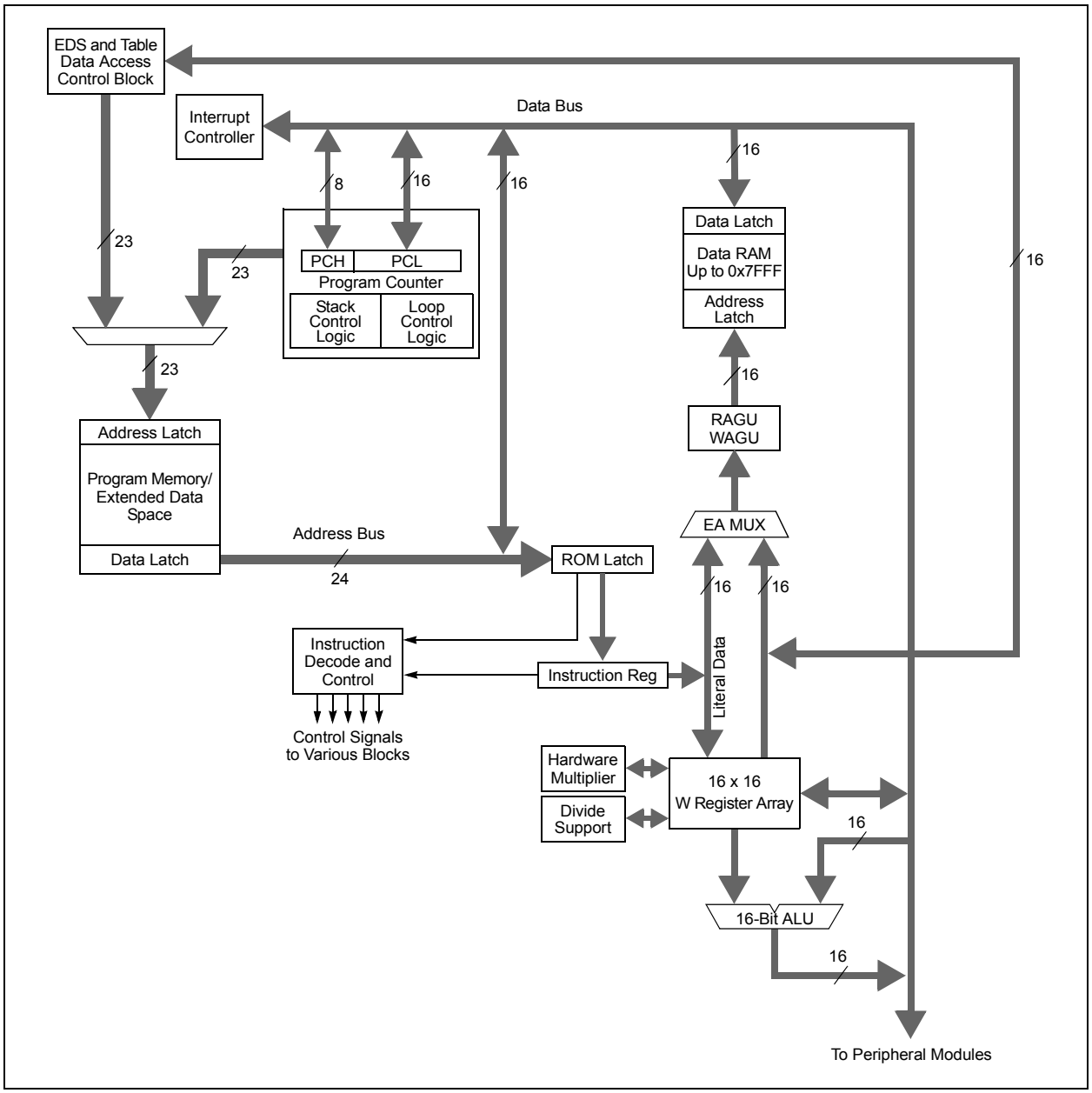
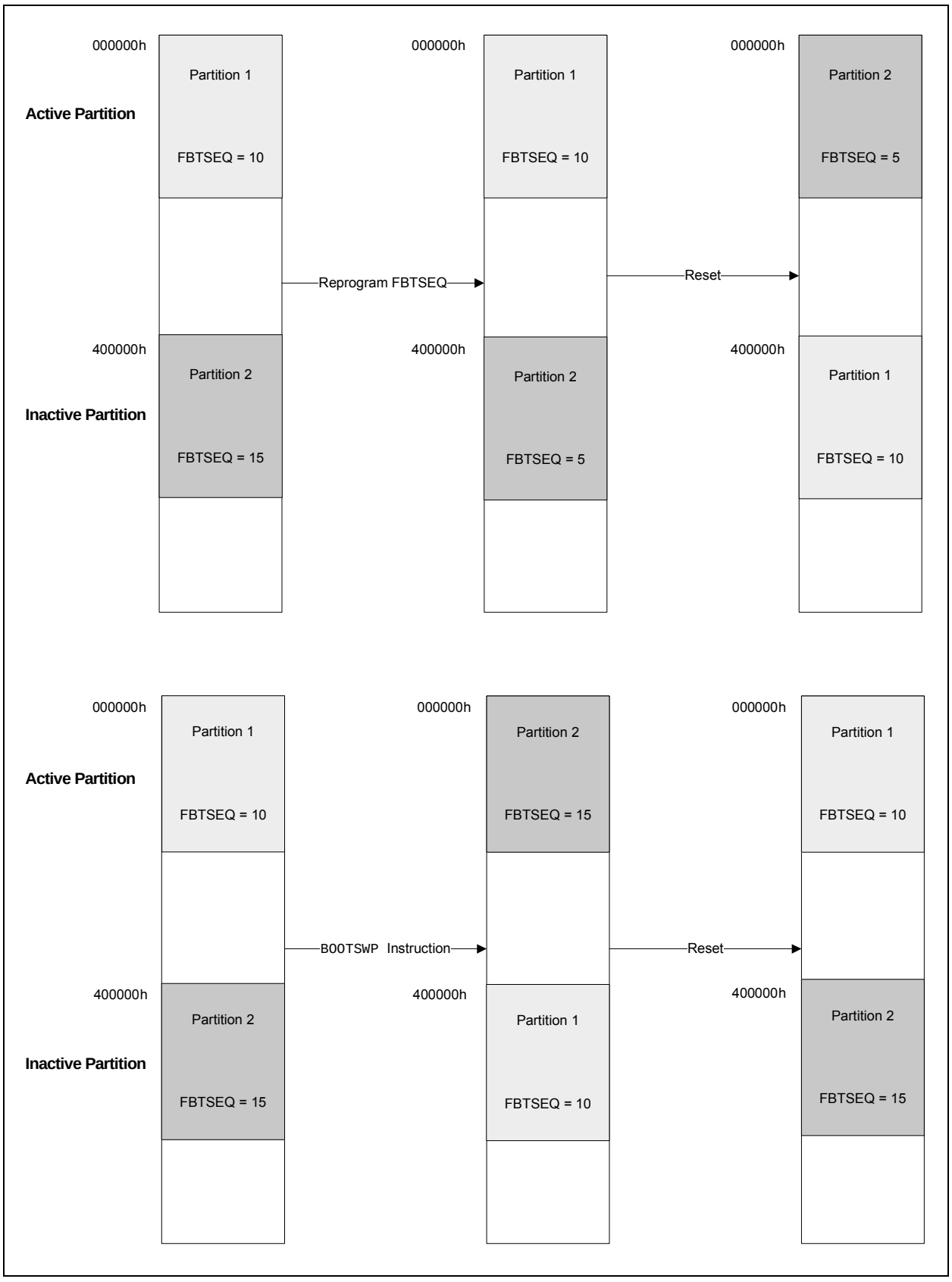


TABLE 3-1: CPU CORE REGISTERS

Register(s) Name	Description
W0 through W15	Working Register Array
PC	23-Bit Program Counter
SR	ALU STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
RCOUNT	REPEAT Loop Counter Register
CORCON	CPU Control Register
DISICNT	Disable Interrupt Count Register
DSRPAG	Data Space Read Page Register
DSWPAG	Data Space Write Page Register

FIGURE 4-4: RELATIONSHIP BETWEEN PARTITIONS 1 AND 2 AND ACTIVE/INACTIVE PARTITIONS



4.3.5.1 Data Read from EDS

In order to read the data from the EDS space, first, an Address Pointer is set up by loading the required EDS page number into the DSRPAG register and assigning the offset address to one of the W registers. Once the above assignment is done, the EDS window is enabled by setting bit 15 of the Working register assigned with the offset address; then, the contents of the pointed EDS location can be read.

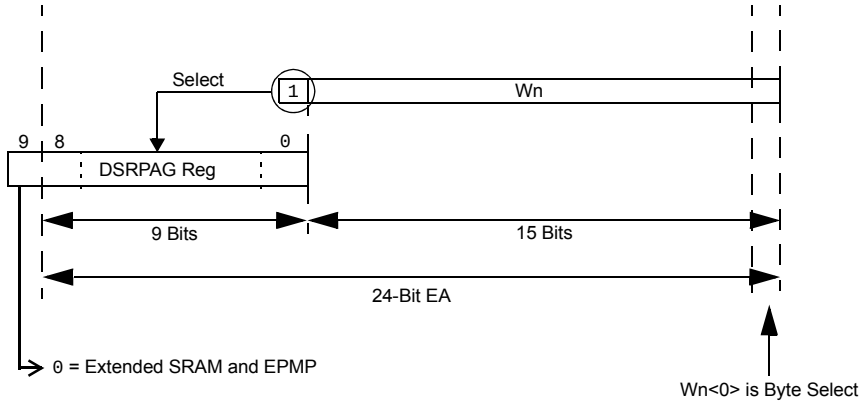
Figure 4-7 illustrates how the EDS space address is generated for read operations.

When the Most Significant bit (MSb) of EA is '1' and DSRPAG<9> = 0, the lower 9 bits of DSRPAG are concatenated to the lower 15 bits of the EA to form a 24-bit EDS space address for read operations.

Example 4-1 shows how to read a byte, word and double-word from EDS.

Note:	All read operations from EDS space have an overhead of one instruction cycle. Therefore, a minimum of two instruction cycles is required to complete an EDS read. EDS reads under the REPEAT instruction; the first two accesses take three cycles and the subsequent accesses take one cycle.

FIGURE 4-7: EDS ADDRESS GENERATION FOR READ OPERATIONS



EXAMPLE 4-1: EDS READ CODE IN ASSEMBLY

```
; Set the EDS page from where the data to be read
    mov        #0x0002, w0
    mov        w0, DSRPAG     ;page 2 is selected for read
    mov        #0x0800, w1    ;select the location (0x800) to be read
    bset       w1, #15        ;set the MSB of the base address, enable EDS mode

;Read a byte from the selected location
    mov.b      [w1++], w2     ;read Low byte
    mov.b      [w1++], w3     ;read High byte

;Read a word from the selected location
    mov        [w1], w2       ;

;Read Double - word from the selected location
    mov.d      [w1], w2       ;two word read, stored in w2 and w3
```

4.4 Interfacing Program and Data Memory Spaces

The PIC24F architecture uses a 24-bit wide program space and 16-bit wide Data Space. The architecture is also a modified Harvard scheme, meaning that data can also be present in the program space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the PIC24F architecture provides two methods by which program space can be accessed during operation:

- Using table instructions to access individual bytes or words anywhere in the program space
- Remapping a portion of the program space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This makes the method ideal for accessing data tables that need to be updated from time to time. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. It can only access the least significant word of the program word.

4.4.1 ADDRESSING PROGRAM SPACE

Since the address ranges for the data and program spaces are 16 and 24 bits, respectively, a method is needed to create a 23-bit or 24-bit program address from 16-bit data registers. The solution depends on the interface method to be used.

For table operations, the 8-bit Table Memory Page Address (TBLPAG) register is used to define a 32K word region within the program space. This is concatenated with a 16-bit EA to arrive at a full 24-bit program space address. In this format, the MSBs of TBLPAG are used to determine if the operation occurs in the user memory (TBLPAG<7> = 0) or the configuration memory (TBLPAG<7> = 1).

For remapping operations, the 10-bit Extended Data Space Read (DSRPAG) register is used to define a 16K word page in the program space. When the Most Significant bit (MSb) of the EA is '1', and the MSb (bit 9) of DSRPAG is '1', the lower 8 bits of DSRPAG are concatenated with the lower 15 bits of the EA to form a 23-bit program space address. The DSRPAG<8> bit decides whether the lower word (when the bit is '0') or the higher word (when the bit is '1') of program memory is mapped. Unlike table operations, this strictly limits remapping operations to the user memory area.

Table 4-15 and Figure 4-10 show how the program EA is created for table operations, and remapping accesses from the data EA. Here, P<23:0> refer to a program space word, whereas D<15:0> refer to a Data Space word.

TABLE 4-15: PROGRAM SPACE ADDRESS CONSTRUCTION

Access Type	Access Space	Program Space Address				
		<23>	<22:16>	<15>	<14:1>	<0>
Instruction Access (Code Execution)	User	0	PC<22:1>			0
		0xx xxxx xxxx xxxx xxxx xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG<7:0>		Data EA<15:0>		
		0xxx xxxx		xxxx xxxx xxxx xxxx		
	Configuration	TBLPAG<7:0>		Data EA<15:0>		
		1xxx xxxx		xxxx xxxx xxxx xxxx		
Program Space Visibility (Block Remap/Read)	User	0	DSRPAG<7:0>(2)		Data EA<14:0>(1)	
		0	xxxx xxxx		xxx xxxx xxxx xxxx	

Note 1: Data EA<15> is always '1' in this case, but is not used in calculating the program space address. Bit 15 of the address is DSRPAG<0>.

2: DSRPAG<9> is always '1' in this case. DSRPAG<8> decides whether the lower word or higher word of program memory is read. When DSRPAG<8> is '0', the lower word is read and when it is '1', the higher word is read.

REGISTER 5-3: DMAINTn: DMA CHANNEL n INTERRUPT REGISTER

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DBUFWF(1)	CHSEL6	CHSEL5	CHSEL4	CHSEL3	CHSEL2	CHSEL1	CHSEL0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
HIGHIF(1,2)	LOWIF(1,2)	DONEIF(1)	HALFIF(1)	OVRUNIF(1)	—	—	HALFEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **DBUFWF:** DMA Buffered Data Write Flag bit(1)
- 1 = The content of the DMA buffer has not been written to the location specified in DMADSTn or DMASRCn in Null Write mode
- 0 = The content of the DMA buffer has been written to the location specified in DMADSTn or DMASRCn in Null Write mode

bit 14-8 **CHSEL<6:0>:** DMA Channel Trigger Selection bits

See Table 5-1 for a complete list.

bit 7 **HIGHIF:** DMA High Address Limit Interrupt Flag bit(1,2)
- 1 = The DMA channel has attempted to access an address higher than DMAH or the upper limit of the data RAM space
- 0 = The DMA channel has not invoked the high address limit interrupt

bit 6 **LOWIF:** DMA Low Address Limit Interrupt Flag bit(1,2)
- 1 = The DMA channel has attempted to access the DMA SFR address lower than DMAL, but above the SFR range (07FFh)
- 0 = The DMA channel has not invoked the low address limit interrupt

bit 5 **DONEIF:** DMA Complete Operation Interrupt Flag bit(1)

If CHEN = 1:
- 1 = The previous DMA session has ended with completion
- 0 = The current DMA session has not yet completed

If CHEN = 0:
- 1 = The previous DMA session has ended with completion
- 0 = The previous DMA session has ended without completion

bit 4 **HALFIF:** DMA 50% Watermark Level Interrupt Flag bit(1)
- 1 = DMACNTn has reached the halfway point to 0000h
- 0 = DMACNTn has not reached the halfway point

bit 3 **OVRUNIF:** DMA Channel Overrun Flag bit(1)
- 1 = The DMA channel is triggered while it is still completing the operation based on the previous trigger
- 0 = The overrun condition has not occurred

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **HALFEN:** Halfway Completion Watermark bit
- 1 = Interrupts are invoked when DMACNTn has reached its halfway point and at completion
- 0 = An interrupt is invoked only at the completion of the transfer

Note 1: Setting these flags in software does not generate an interrupt.

2: Testing for address limit violations (DMASRCn or DMADSTn is either greater than DMAH or less than DMAL) is NOT done before the actual access.

REGISTER 8-50: IPC28: INTERRUPT PRIORITY CONTROL REGISTER 28

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U6TXIP2	U6TXIP1	U6TXIP0	—	U6RXIP2	U6RXIP1	U6RXIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U5ERIP2	U5ERIP1	U5ERIP0	—	U5TXIP2	U5TXIP1	U5TXIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **U6TXIP<2:0>:** UART6 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **U6RXIP<2:0>:** UART6 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **U5ERIP<2:0>:** UART5 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **U5TXIP<2:0>:** UART5 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

9.4 Clock Switching Operation

With few limitations, applications are free to switch between any of the four clock sources (POSC, SOSC, FRC and LPRC) under software control and at any time. To limit the possible side effects that could result from this flexibility, PIC24F devices have a safeguard lock built into the switching process.

Note:	The Primary Oscillator mode has three different submodes (XT, HS and EC) which are determined by the POSCMODx Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

9.4.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSMx Configuration bits in the FOSC Configuration Word must be programmed. (Refer to **Section 33.1 "Configuration Bits"** for further details.) If the bits are unmodified, the clock switching function and Fail-Safe Clock Monitor function are disabled; this is the default setting.

The NOSCx control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSC<2:0> bits (OSCCON<14:12>) will reflect the clock source selected by the FNOSCx Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled; it is held at '0' at all times.

9.4.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires this basic sequence:

1. If desired, read the COSC<2:0> bits (OSCCON<14:12>) to determine the current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
3. Write the appropriate value to the NOSCx bits (OSCCON<10:8>) for the new oscillator source.
4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
5. Set the OSWEN bit to initiate the oscillator switch.

Once the basic sequence is completed, the system clock hardware responds automatically as follows:

1. The clock switching hardware compares the COSCx bits with the new value of the NOSCx bits. If they are the same, then the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.
2. If a valid clock switch has been initiated, the LOCK (OSCCON<5>) and CF (OSCCON<3>) bits are cleared.
3. The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware will wait until the OST expires. If the new source is using the PLL, then the hardware waits until a PLL lock is detected (LOCK = 1).
4. The hardware waits for 10 clock cycles from the new clock source and then performs the clock switch.
5. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSCx bits value is transferred to the COSCx bits.
6. The old clock source is turned off at this time, with the exception of LPRC (if WDT or FSCM is enabled) or SOSC (if SOSCEN remains set).

Note 1:	The processor will continue to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.
2:	Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

REGISTER 10-2: DSWAKE: DEEP SLEEP WAKE-UP SOURCE REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS
—	—	—	—	—	—	—	DSINT0
bit 15							bit 8

R/W-0, HS	U-0	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	U-0	U-0
DSFLT	—	—	DSWDT	DSRTCC	DSMCLR	—	—
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **DSINT0:** Deep Sleep Interrupt-on-Change bit
1 = Interrupt-on-change was asserted during Deep Sleep
0 = Interrupt-on-change was not asserted during Deep Sleep

bit 7 **DSFLT:** Deep Sleep Fault Detect bit
1 = A Fault occurred during Deep Sleep and some Deep Sleep configuration settings may have been corrupted
0 = No Fault was detected during Deep Sleep

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **DSWDT:** Deep Sleep Watchdog Timer Time-out bit
1 = The Deep Sleep Watchdog Timer timed out during Deep Sleep
0 = The Deep Sleep Watchdog Timer did not time out during Deep Sleep

bit 3 **DSRTCC:** Deep Sleep Real-Time Clock and Calendar Alarm bit
1 = The Real-Time Clock and Calendar triggered an alarm during Deep Sleep
0 = The Real-Time Clock and Calendar did not trigger an alarm during Deep Sleep

bit 2 **DSMCLR:** Deep Sleep $\overline{\text{MCLR}}$ Event bit
1 = The $\overline{\text{MCLR}}$ pin was active and was asserted during Deep Sleep
0 = The $\overline{\text{MCLR}}$ pin was not active, or was active, but not asserted during Deep Sleep

bit 1-0 **Unimplemented:** Read as '0'

Note 1: All register bits are cleared when the DSEN (DSCON<15>) bit is set.

REGISTER 11-9: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	IC3R5	IC3R4	IC3R3	IC3R2	IC3R1	IC3R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **IC3R<5:0>:** Assign Input Capture 3 (IC3) to Corresponding RPn or RPIn Pin bits

REGISTER 11-10: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	OCFBR5	OCFBR4	OCFBR3	OCFBR2	OCFBR1	OCFBR0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	OCFAR5	OCFAR4	OCFAR3	OCFAR2	OCFAR1	OCFAR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **OCFBR<5:0>:** Assign Output Compare Fault B (OCFB) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **OCFAR<5:0>:** Assign Output Compare Fault A (OCFA) to Corresponding RPn or RPIn Pin bits

REGISTER 17-1: SPIxCON1L: SPIx CONTROL REGISTER 1 LOW (CONTINUED)

bit 9 **SMP:** SPIx Data Input Sample Phase bit
Master Mode:
1 = Input data is sampled at the end of data output time
0 = Input data is sampled at the middle of data output time
Slave Mode:
Input data is always sampled at the middle of data output time, regardless of the SMP setting.

bit 8 **CKE:** SPIx Clock Edge Select bit(1)
1 = Transmit happens on transition from active clock state to Idle clock state
0 = Transmit happens on transition from Idle clock state to active clock state

bit 7 **SSEN:** Slave Select Enable bit (Slave mode)(2)
1 = $\overline{SSx}$ pin is used by the macro in Slave mode; $\overline{SSx}$ pin is used as the slave select input
0 = $\overline{SSx}$ pin is not used by the macro ($\overline{SSx}$ pin will be controlled by the port I/O)

bit 6 **CKP:** Clock Polarity Select bit
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

bit 4 **DISSDI:** Disable SDIx Input Port bit
1 = SDIx pin is not used by the module; pin is controlled by port function
0 = SDIx pin is controlled by the module

bit 3 **DISSCK:** Disable SCKx Output Port bit
1 = SCKx pin is not used by the module; pin is controlled by port function
0 = SCKx pin is controlled by the module

bit 2 **MCLKEN:** Master Clock Enable bit(3)
1 = REFO is used by the BRG
0 = FOSC/2 is used by the BRG

bit 1 **SPIFE:** Frame Sync Pulse Edge Select bit
1 = Frame Sync pulse (Idle-to-active edge) coincides with the first bit clock
0 = Frame Sync pulse (Idle-to-active edge) precedes the first bit clock

bit 0 **ENHBUF:** Enhanced Buffer Enable bit
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

Note 1: When AUDEN (SPIxCON1H<15>) = 1, this module functions as if CKE = 0, regardless of its actual value.
2: When FRMEN = 1, SSEN is not used.
3: MCLKEN can only be written when the SPIEN bit = 0.
4: This channel is not meaningful for DSP/PCM mode as LRC follows FRMSYPW.

REGISTER 20-5: U1PWRC: USB POWER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-x, HSC	U-0	U-0	R/W-0	U-0	U-0	R/W-0, HC	R/W-0
UACTPND	—	—	USLPGRD	—	—	USUSPND	USBPWR
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit
1 = Module should not be suspended at the moment (requires the USLPGRD bit to be set)
0 = Module may be suspended or powered down

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep/Suspend Guard bit
1 = Indicates to the USB module that it is about to be suspended or powered down
0 = No suspend

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **USUSPND:** USB Suspend Mode Enable bit
1 = USB OTG module is in Suspend mode; USB clock is gated and the transceiver is placed in a low-power state
0 = Normal USB OTG operation

bit 0 **USBPWR:** USB Operation Enable bit
1 = USB OTG module is enabled
0 = USB OTG module is disabled(1)

Note 1: Do not clear this bit unless the HOSTEN, USBEN and OTGEN bits (U1CON<3,0> and U1OTGCON<2>) are all cleared.

REGISTER 20-13: U1CNFG2: USB CONFIGURATION REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	U-0	U-0	r-0	r-0
—	—	—	PUVBUS(1)	—	—	—	—
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4 **PUVBUS:** VBUS Pull-Up Enable bit(1)
1 = Pull-up on VBUS pin is enabled
0 = Pull-up on VBUS pin is disabled

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **Reserved:** Maintain as '0'

Note 1: Never change this bit while the USBPWR bit is set (U1PWRC<0> = 1).

REGISTER 25-5: CFGPAGE: SECURE ARRAY CONFIGURATION BITS (OTP PAGE 0) REGISTER

r-x	R/PO-x	R/P-x	R/P-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x
—	TSTPGM(1)	KEYSZRAM1	KEYSZRAM0	KEY4TYPE1	KEY4TYPE0	KEY3TYPE1	KEY3TYPE0
bit 31							bit 24

R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x
KEY2TYPE1	KEY2TYPE0	KEY1TYPE1	KEY1TYPE0	SKEYEN	LKYSRC7	LKYSRC6	LKYSRC5
bit 23							bit 16

R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x
LKYSRC4	LKYSRC3	LKYSRC2	LKYSRC1	LKYSRC0	SRCLCK	WRLOCK8	WRLOCK7
bit 15							bit 8

R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x
WRLOCK6	WRLOCK5	WRLOCK74	WRLOCK3	WRLOCK2	WRLOCK1	WRLOCK0	SWKYDIS
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	PO = Program Once bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** Do not modify

bit 30 **TSTPGM:** Customer Program Test bit(1)
1 = CFGPAGE has been programmed
0 = CFGPAGE has not been programmed

bit 29-28 **KEYSZRAM<1:0>:** Key Type Selection bits (Key RAM Pages)
11 = Keys in these pages are 192/256-bit AES operations only
10 = Keys in these pages are 128-bit AES operations only
01 = Keys in these pages are DES3 operations only
00 = Keys in these pages are DES/DES2 operations only

bit 27-26 **KEY4TYPE<1:0>:** Key Type for OTP Pages 7 and 8 bits
11 = Keys in these pages are for 192-bit/256-bit AES operations only
10 = Keys in these pages are for 128-bit AES operations only
01 = Keys in these pages are for 3DES operations only
00 = Keys in these pages are for DES/2DES operations only

bit 25-24 **KEY3TYPE<1:0>:** Key Type for OTP Pages 5 and 6 bits
11 = Keys in these pages are for 192-bit/256-bit AES operations only
10 = Keys in these pages are for 128-bit AES operations only
01 = Keys in these pages are for 3DES operations only
00 = Keys in these pages are for DES/2DES operations only

bit 23-22 **KEY2TYPE<1:0>:** Key Type for OTP Pages 3 and 4 bits
11 = Keys in these pages are for 192-bit/256-bit AES operations only
10 = Keys in these pages are for 128-bit AES operations only
01 = Keys in these pages are for 3DES operations only
00 = Keys in these pages are for DES/2DES operations only

Note 1: This bit’s state is mirrored by the PGMTST bit (CRYOTP<7>).

TABLE 25-2: AES KEY MODE/SOURCE SELECTION

Mode of Operation	KEYMOD<1:0>	KEYSRC<3:0>	Key Source		OTP Address
			SKEYEN = 0	SKEYEN = 1	
128-Bit AES	00	0000(1)	CRYKEY<127:0>		—
		0001	AES Key #1	Key Config Error(2)	<127:0>
		0010	AES Key #2		<255:128>
		0011	AES Key #3		<383:256>
		0100	AES Key #4		<511:384>
		1001	AES Key #5 (RAM)		<127:0>
		1010	AES Key #6 (RAM)		<255:128>
		1011	AES Key #7 (RAM)		<383:256>
		1100	AES Key #8 (RAM)		<511:384>
		1111	Reserved(2)		—
		All Others	Key Config Error(2)		—
192-Bit AES	01	0000(1)	CRYKEY<191:0>		—
		0001	AES Key #1	Key Config Error(2)	<191:0>
		0010	AES Key #2		<383:192>
		1001	AES Key #3 (RAM)		<191:0>
		1010	AES Key #4 (RAM)		<383:192>
		1111	Reserved(2)		—
		All Others	Key Config Error(2)		—
256-Bit AES	10	0000(1)	CRYKEY<255:0>		—
		0001	AES Key #1	Key Config Error(2)	<255:0>
		0010	AES Key #2		<511:256>
		1001	AES Key #3 (RAM)		<255:0>
		1010	AES Key #4 (RAM)		<511:256>
		1111	Reserved(2)		—
		All Others	Key Config Error(2)		—
(Reserved)	11	xxxx	Key Config Error(2)		—

Note 1: This configuration is considered a key configuration error (KEYFAIL bit is set) if SWKYDIS is also set.

2: The KEYFAIL bit (CRYSTAT<1>) is set when these configurations are selected and remains set until a valid configuration is selected.

NOTES:

32.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

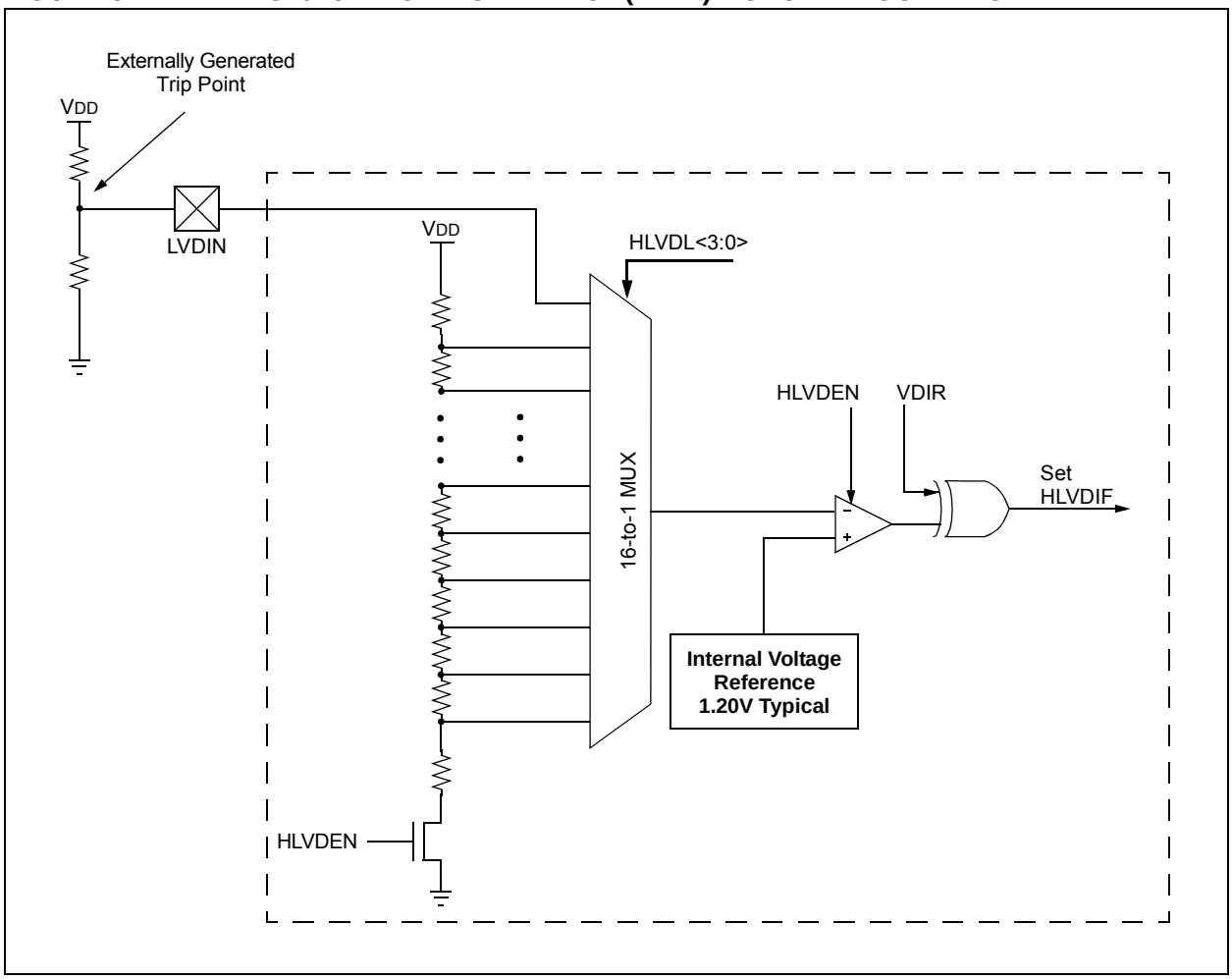
Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the High/Low-Voltage Detect, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"High-Level Integration with Programmable High/Low-Voltage Detect (HLVD)"** (DS39725). The information in this data sheet supersedes the information in the FRM.

The High/Low-Voltage Detect (HLVD) module is a programmable circuit that allows the user to specify both the device voltage trip point and the direction of change.

An interrupt flag is set if the device experiences an excursion past the trip point in the direction of change. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to the interrupt.

The HLVD Control register (see Register 32-1) completely controls the operation of the HLVD module. This allows the circuitry to be "turned off" by the user under software control, which minimizes the current consumption for the device.

FIGURE 32-1: HIGH/LOW-VOLTAGE DETECT (HLVD) MODULE BLOCK DIAGRAM



36.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC24FJ256GA412/GB412 family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC24FJ256GA412/GB412 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +100°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on any general purpose digital or analog pin (not 5.5V tolerant) with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any general purpose digital or analog pin (5.5V tolerant, including $\overline{MCLR}$) with respect to V_{SS}:
When V_{DD} = 0V: ..... -0.3V to + 4.0V
When $V_{DD} \geq$ 2.0V: ..... -0.3V to +6.0V
Voltage on AV_{DD} with respect to V_{SS} ..... (V_{DD} – 0.3V) to (lesser of: 4.0V or (V_{DD} + 0.3V))
Voltage on AV_{SS} with respect to V_{SS} ..... -0.3V to +0.3V
Voltage on V_{BAT} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on V_{USB3V3} with respect to V_{SS} ..... (V_{CAP} – 0.3V) to +4.0V
Voltage on V_{BUS} with respect to V_{SS} ..... -0.3V to +6.0V
Voltage on D+ or D- with respect to V_{SS}:
(0Ω source impedance) **(Note 1)** ..... -0.5V to (V_{USB3V3} + 0.5V)
(Source Impedance ≥ 28Ω, $V_{USB3V3} \geq$ 3.0V) ..... -1.0V to +4.6V
Maximum current out of V_{SS} pin ..... 300 mA
Maximum current into V_{DD} pin **(Note 2)** ..... 250 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by all ports ..... 200 mA
Maximum current sourced by all ports **(Note 2)** ..... 200 mA

Note 1: The original *"USB 2.0 Specification"* indicated that USB devices should withstand 24-hour short circuits of D+ or D- to V_{BUS} voltages. This requirement was later removed in an Engineering Change Notice (ECN) supplement to the USB specifications, which supersedes the original specifications. PIC24FJ256GA412/GB412 family devices will typically be able to survive this short-circuit test, but it is recommended to adhere to the absolute maximum specified here to avoid damaging the device.

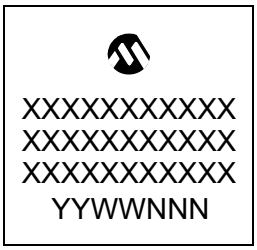
2: Maximum allowable current is a function of device maximum power dissipation (see Table 36-1).

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

37.0 PACKAGING INFORMATION

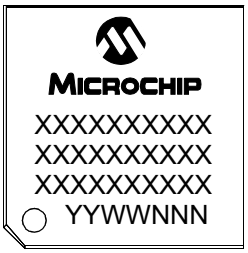
37.1 Package Marking Information

64-Lead QFN (9x9x0.9 mm)

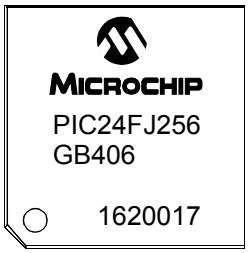


Example

64-Lead TQFP (10x10x1 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.