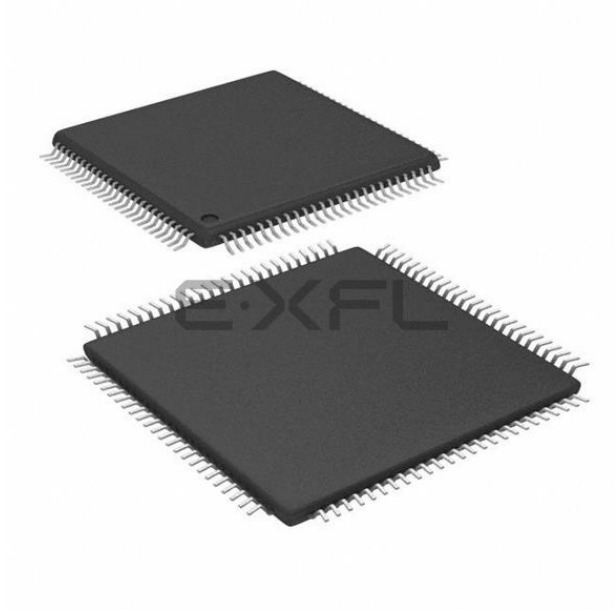
Microchip Technology - PIC24FJ256GB410T-I/PT Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256gb410t-i-pt

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
IOCD0	46	72	D9	I	ST	PORTD Interrupt-on-Change
IOCD1	49	76	A11	I	ST	
IOCD2	50	77	A10	I	ST	
IOCD3	51	78	B9	I	ST	
IOCD4	52	81	C8	I	ST	
IOCD5	53	82	B8	I	ST	
IOCD6	54	83	D7	I	ST	
IOCD7	55	84	C7	I	ST	
IOCD8	42	68	E9	I	ST	
IOCD9	43	69	E10	I	ST	
IOCD10	44	70	D11	I	ST	
IOCD11	45	71	C11	I	ST	
IOCD12	—	79	A9	I	ST	
IOCD13	—	80	D8	I	ST	
IOCD14	—	47	L9	I	ST	
IOCD15	—	48	K9	I	ST	
IOCE0	60	93	1E3	I	ST	PORTE Interrupt-on-Change
IOCE1	61	94	E15	I	ST	
IOCE2	62	98	E19	I	ST	
IOCE3	63	99	E30	I	ST	
IOCE4	64	100	E31	I	ST	
IOCE5	1	3	D3	I	ST	
IOCE6	2	4	C1	I	ST	
IOCE7	3	5	D2	I	ST	
IOCE8	—	18	G1	I	ST	
IOCE9	—	19	G2	I	ST	
IOCF0	58	87	B6	I	ST	PORTF Interrupt-on-Change
IOCF1	59	88	A6	I	ST	
IOCF2	34	52	K11	I	ST	
IOCF3	33	51	K10	I	ST	
IOCF4	31	49	L10	I	ST	
IOCF5	32	50	L11	I	ST	
IOCF6	35	55	H9	I	ST	
IOCF7	—	54	H8	I	ST	
IOCF8	—	53	J10	I	ST	
IOCF12	—	40	K6	I	ST	
IOCF13	—	39	L6	I	ST	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

TABLE 1-5: PIC24FJ256GB412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
PMA8	32	50	L11	I/O	DIG/ST/TTL	Parallel Master Port Address (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMA9	31	49	L10	I/O	DIG/ST/TTL	
PMA10	28	42	L7	I/O	DIG/ST/TTL	
PMA11	27	41	J7	I/O	DIG/ST/TTL	
PMA12	24	35	K5	I/O	DIG/ST/TTL	
PMA13	23	34	H5	I/O	DIG/ST/TTL	
PMA16	—	95	C4	O	DIG	
PMA17	—	92	B5	O	DIG	
PMA18	—	40	K6	O	DIG	
PMA19	—	19	G2	O	DIG	
PMA2/PMALU	8	14	F3	O	DIG	Parallel Master Port Address<2>/Address Latch Upper
PMA3	6	12	F2	O	DIG	Parallel Master Port Address
PMA4	5	11	F4	O	DIG	
PMA5	4	10	E3	O	DIG	
PMA20	—	59	G10	O	DIG	Parallel Master Port Address (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMA21	—	60	G11	O	DIG	
PMA22	—	66	E11	O	DIG	
PMACK1	50	77	A10	I	ST/TTL	Parallel Master Port Acknowledge Input 1
PMACK2	43	69	E10	I	ST/TTL	Parallel Master Port Acknowledge Input 2
PMBE0	51	78	B9	O	DIG	Parallel Master Port Byte Enable 0 Strobe
PMBE1	—	67	E8	O	DIG	Parallel Master Port Byte Enable 1 Strobe
PMCS1	—	18	G1	O	DIG	Parallel Master Port Chip Select 1 Strobe
PMCS2	—	9	E!	O	DIG	Parallel Master Port Chip Select 2 Strobe
PMD0	60	93	A4	I/O	DIG/ST/TTL	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMD1	61	94	B4	I/O	DIG/ST/TTL	
PMD2	62	98	B3	I/O	DIG/ST/TTL	
PMD3	63	99	A2	I/O	DIG/ST/TTL	
PMD4	64	100	A1	I/O	DIG/ST/TTL	
PMD5	1	3	D3	I/O	DIG/ST/TTL	
PMD6	2	4	C1	I/O	DIG/ST/TTL	
PMD7	3	5	D2	I/O	DIG/ST/TTL	
PMD8	—	90	A5	I/O	DIG/ST/TTL	
PMD9	—	89	E6	I/O	DIG/ST/TTL	
PMD10	—	88	A6	I/O	DIG/ST/TTL	
PMD11	—	87	B6	I/O	DIG/ST/TTL	
PMD12	—	79	A9	I/O	DIG/ST/TTL	
PMD13	—	80	D8	I/O	DIG/ST/TTL	
PMD14	—	83	D7	I/O	DIG/ST/TTL	
PMD15	—	84	C7	I/O	DIG/ST/TTL	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
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XCVR = Dedicated transceiver

4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-2).

Program memory addresses are always word-aligned on the lower word and addresses are incremented or decremented by two during code execution. This arrangement also provides compatibility with data memory space addressing and makes it possible to access data in the program memory space.

4.1.2 HARD MEMORY VECTORS

All PIC24F devices reserve the addresses between 000000h and 000200h for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user at 000000h with the actual address for the start of code at 000002h.

PIC24F devices also have two Interrupt Vector Tables (IVTs). The main IVT has a static location, from 000004h to 0000FFh. The Alternate IVT has a configurable location and is optionally enabled. A more detailed discussion of the Interrupt Vector Tables is provided in **Section 8.0 "Interrupt Controller"**.

4.1.3 SINGLE AND DUAL PARTITION MEMORY ORGANIZATION

The PIC24FJ256GA412/GB412 family of devices supports a Single Partition Flash mode and two Dual Partition Flash modes. The Dual Partition modes allow the device to be programmed with two separate applications to facilitate bootloading or to allow an application to be programmed at run-time without stalling the CPU.

In the Dual Partition modes, the device's memory is divided evenly into two physical sections, known as Partition 1 and Partition 2. Each of these partitions contains its own program memory and Configuration Words. During program execution, the code on only one of these panels is executed; this is the Active Partition. The other partition, or the Inactive Partition, is not used, but can be programmed.

The Active Partition is always mapped to logical address, 000000h, while the Inactive Partition will always be mapped to logical address, 400000h. Note that even when the code partitions are switched between active and inactive by the user, the address of the Active Partition will still be 000000h and the address of the Inactive Partition will still be at 400000h. Figure 4-3 compares the mapping of the user memory space in Single and Dual Partition devices.

FIGURE 4-2: PROGRAM MEMORY ORGANIZATION

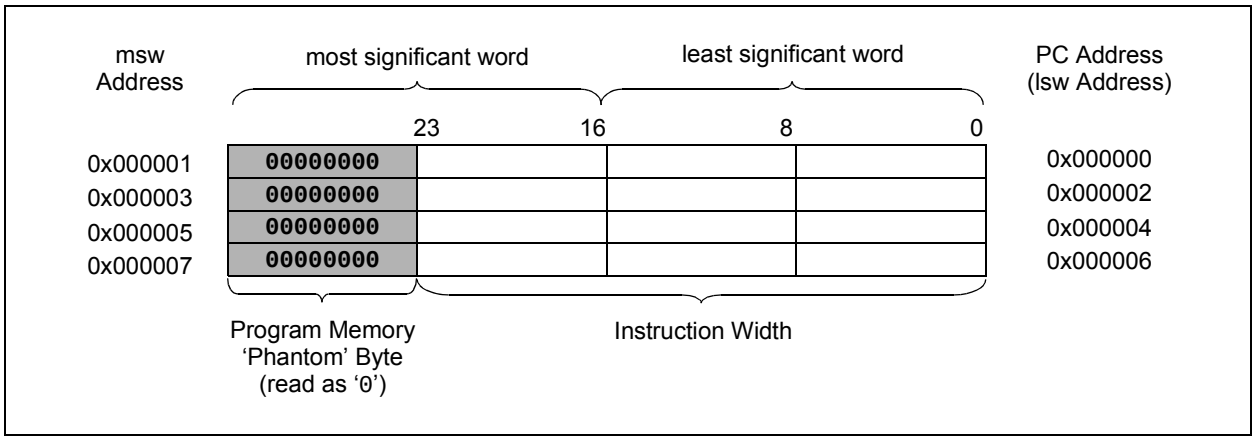


TABLE 4-10: SFR BLOCK 500h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
DMA (Continued)			CRYTXTB6	564	xxxxxxxxxxxxxxxx	U1EP8(1)	5B2	0000000000000000
DMAINT5	500	0000000000000000	CRYTXTB7	566	xxxxxxxxxxxxxxxx	U1EP9(1)	5B4	0000000000000000
DMASRC5	502	0000000000000000	CRYTXTC0	558	xxxxxxxxxxxxxxxx	U1EP10(1)	5B6	0000000000000000
DMADST5	504	0000000000000000	CRYTXTC1	56A	xxxxxxxxxxxxxxxx	U1EP11(1)	5B8	0000000000000000
DMACNT5	506	0000000000000001	CRYTXTC2	56C	xxxxxxxxxxxxxxxx	U1EP12(1)	5BA	0000000000000000
Cryptographic Engine			CRYTXTC3	56E	xxxxxxxxxxxxxxxx	U1EP13(1)	5BC	0000000000000000
CRYCONL	51C	x0xxxx0xxxxxxxxx	CRYTXTC4	570	xxxxxxxxxxxxxxxx	U1EP14(1)	5BE	0000000000000000
CRYCONH	51E	0xxxxxxxxxx0xxxx	CRYTXTC5	572	xxxxxxxxxxxxxxxx	U1EP15(1)	5C0	0000000000000000
CRYSTAT	520	00000000xxxx0xxx	CRYTXTC6	574	xxxxxxxxxxxxxxxx	**LCD Controller**		
CRYOTP	524	00000000xxxxxxxx	CRYTXTC7	576	xxxxxxxxxxxxxxxx	LCDCON	5C2	0000000000000000(2)
CRYKEY0	528	xxxxxxxxxxxxxxxx	**USB**			LCDREF	5C4	0000000000000000(2)
CRYKEY1	52A	xxxxxxxxxxxxxxxx	U1OTGIR(1)	578	0000000000000000	LCDPS	5C6	0000000000000000(2)
CRYKEY2	52C	xxxxxxxxxxxxxxxx	U1OTGIE(1)	57A	0000000000000000	LCDDATA0	5C8	0000000000000000(2)
CRYKEY3	52E	xxxxxxxxxxxxxxxx	U1OTGSTAT(1)	57C	0000000000000000	LCDDATA1	5CA	0000000000000000(2)
CRYKEY4	530	xxxxxxxxxxxxxxxx	U1OTGCON(1)	57E	0000000000000000	LCDDATA2	5CC	0000000000000000(2)
CRYKEY5	532	xxxxxxxxxxxxxxxx	U1PWRC(1)	580	00000000x0000000	LCDDATA3	5CE	0000000000000000(2)
CRYKEY6	534	xxxxxxxxxxxxxxxx	U1IR(1)	582	0000000000000000	LCDDATA4	5D0	0000000000000000(2)
CRYKEY7	536	xxxxxxxxxxxxxxxx	U1IE(1)	584	0000000000000000	LCDDATA5	5D2	0000000000000000(2)
CRYKEY8	538	xxxxxxxxxxxxxxxx	U1EIR(1)	586	0000000000000000	LCDDATA6	5D4	0000000000000000(2)
CRYKEY9	53A	xxxxxxxxxxxxxxxx	U1EIE(1)	588	0000000000000000	LCDDATA7	5D6	0000000000000000(2)
CRYKEY10	53C	xxxxxxxxxxxxxxxx	U1STAT(1)	58A	0000000000000000	LCDDATA8	5D8	0000000000000000(2)
CRYKEY11	53E	xxxxxxxxxxxxxxxx	U1CON(1)	58C	00000000xx000000	LCDDATA9	5DA	0000000000000000(2)
CRYKEY12	540	xxxxxxxxxxxxxxxx	U1ADDR(1)	58E	000000000xxxxxxx	LCDDATA10	5DC	0000000000000000(2)
CRYKEY13	542	xxxxxxxxxxxxxxxx	U1BDTP1(1)	590	0000000000000000	LCDDATA11	5DE	0000000000000000(2)
CRYKEY14	544	xxxxxxxxxxxxxxxx	U1FRML(1)	592	0000000000000000	LCDDATA12	5E0	0000000000000000(2)
CRYKEY15	546	xxxxxxxxxxxxxxxx	U1FRMH(1)	594	0000000000000000	LCDDATA13	5E2	0000000000000000(2)
CRYTXTA0	548	xxxxxxxxxxxxxxxx	U1TOK(1)	596	0000000000000000	LCDDATA14	5E4	0000000000000000(2)
CRYTXTA1	54A	xxxxxxxxxxxxxxxx	U1SOF(1)	598	0000000000000000	LCDDATA15	5E6	0000000000000000(2)
CRYTXTA2	54C	xxxxxxxxxxxxxxxx	U1BDTP2(1)	59A	0000000000000000	LCDDATA16	5E8	0000000000000000(2)
CRYTXTA3	54E	xxxxxxxxxxxxxxxx	U1BDTP3(1)	59C	0000000000000000	LCDDATA17	5EA	0000000000000000(2)
CRYTXTA4	550	xxxxxxxxxxxxxxxx	U1CNFG1(1)	59E	0000000000000000	LCDDATA18	5EC	0000000000000000(2)
CRYTXTA5	552	xxxxxxxxxxxxxxxx	U1CNFG2(1)	5A0	0000000000000000	LCDDATA19	5EE	0000000000000000(2)
CRYTXTA6	554	xxxxxxxxxxxxxxxx	U1EP0(1)	5A2	0000000000000000	LCDDATA20	5F0	0000000000000000(2)
CRYTXTA7	556	xxxxxxxxxxxxxxxx	U1EP1(1)	5A4	0000000000000000	LCDDATA21	5F2	0000000000000000(2)
CRYTXTB0	558	xxxxxxxxxxxxxxxx	U1EP2(1)	5A6	0000000000000000	LCDDATA22	5F4	0000000000000000(2)
CRYTXTB1	55A	xxxxxxxxxxxxxxxx	U1EP3(1)	5A8	0000000000000000	LCDDATA23	5F6	0000000000000000(2)
CRYTXTB2	55C	xxxxxxxxxxxxxxxx	U1EP4(1)	5AA	0000000000000000	LCDDATA24	5F8	0000000000000000(2)
CRYTXTB3	55E	xxxxxxxxxxxxxxxx	U1EP5(1)	5AC	0000000000000000	LCDDATA25	5FA	0000000000000000(2)
CRYTXTB4	560	xxxxxxxxxxxxxxxx	U1EP6(1)	5AE	0000000000000000	LCDDATA26	5FC	0000000000000000(2)
CRYTXTB5	562	xxxxxxxxxxxxxxxx	U1EP7(1)	5B0	0000000000000000	LCDDATA27	5FE	0000000000000000(2)

Legend: x = unknown or indeterminate value. Reset and address values are in hexadecimal.

Note 1: Implemented in PIC24FJXXXGB4XX devices only.

2: LCD registers are only reset on a device POR.

REGISTER 8-2: CORCON: CPU CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/C-0	r-1	U-0	U-0
—	—	—	—	IPL3(1)	—	—	—
bit 7							bit 0

Legend:	r = Reserved bit	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit(1)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

bit 2 **Reserved:** Read as '1'

bit 1-0 **Unimplemented:** Read as '0'

Note 1: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level; see Register 3-2 for bit description.

REGISTER 8-39: IPC17: INTERRUPT PRIORITY CONTROL REGISTER 17

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	MI2C3IP2	MI2C3IP1	MI2C3IP0	—	SI2C3IP2	SI2C3IP1	SI2C3IP0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **MI2C3IP<2:0>:** Master I2C3 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **SI2C3IP<2:0>:** Slave I2C3 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 8-44: IPC22: INTERRUPT PRIORITY CONTROL REGISTER 22

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPI3TXIP2	SPI3TXIP1	SPI3TXIP0	—	SPI3IP2	SPI3IP1	SPI3IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U4TXIP2	U4TXIP1	U4TXIP0	—	U4RXIP2	U4RXIP1	U4RXIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **SPI3TXIP<2:0>:** SPI3 Transmit Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **SPI3IP<2:0>:** SPI3 General Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **U4TXIP<2:0>:** UART4 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **U4RXIP<2:0>:** UART4 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 11-21: RPINR28: PERIPHERAL PIN SELECT INPUT REGISTER 28

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SCK3R5	SCK3R4	SCK3R3	SCK3R2	SCK3R1	SCK3R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SDI3R5	SDI3R4	SDI3R3	SDI3R2	SDI3R1	SDI3R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **SCK3R<5:0>:** Assign SPI3 Clock Input (SCK3IN) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **SDI3R<5:0>:** Assign SPI3 Data Input (SDI3) to Corresponding RPn or RPIn Pin bits

REGISTER 11-22: RPINR29: PERIPHERAL PIN SELECT INPUT REGISTER 29

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SS3R5	SS3R4	SS3R3	SS3R2	SS3R1	SS3R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **SS3R<5:0>:** Assign SPI3 Slave Select Input (SS3IN) to Corresponding RPn or RPIn Pin bits

REGISTER 14-2: CCPxCON1H: CCPx CONTROL 1 HIGH REGISTERS

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
OPSSRC(1)	RTRGEN(2)	—	—	OPS3(3)	OPS2(3)	OPS1(3)	OPS0(3)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRIGEN	ONESHOT	ALTSYNC	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OPSSRC:** Output Postscaler Source Select bit(1)
1 = Output postscaler scales module trigger output events
0 = Output postscaler scales time base interrupt events

bit 14 **RTRGEN:** Retrigger Enable bit(2)
1 = Time base can be retriggered when TRIGEN bit = 1
0 = Time base may not be retriggered when TRIGEN bit = 1

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **OPS3<3:0>:** CCPx Interrupt Output Postscale Select bits(3)
1111 = Interrupt every 16th time base period match
1110 = Interrupt every 15th time base period match
...
0100 = Interrupt every 5th time base period match
0011 = Interrupt every 4th time base period match or 4th input capture event
0010 = Interrupt every 3rd time base period match or 3rd input capture event
0001 = Interrupt every 2nd time base period match or 2nd input capture event
0000 = Interrupt after each time base period match or input capture event

bit 7 **TRIGEN:** CCPx Trigger Enable bit
1 = Trigger operation of time base is enabled
0 = Trigger operation of time base is disabled

bit 6 **ONESHOT:** One-Shot Mode Enable bit
1 = One-Shot Trigger mode is enabled; trigger duration is set by OSCNT<2:0>
0 = One-Shot Trigger mode is disabled

bit 5 **ALTSYNC:** CCPx Clock Select bits
1 = An alternate signal is used as the module synchronization output signal
0 = The module synchronization output signal is the Time Base Reset/rollover event

bit 4-0 **SYNC<4:0>:** CCPx Synchronization Source Select bits
See Table 14-6 for the definition of inputs.

Note 1: This control bit has no function in Input Capture modes.
2: This control bit has no function when TRIGEN = 0.
3: Output postscale settings, from 1:5 to 1:16 ('0100' to '1111'), will result in a FIFO buffer overflow for Input Capture modes.

TABLE 14-6: SYNCHRONIZATION SOURCES

SYNC<4:0>	Synchronization Source
00000	None; Timer with Rollover on CCPxPRH/L Match or FFFFh
00001	Module's Own Timer Sync Out
00010	MCCP1 Sync Output
00011	SCCP2 Sync Output
00100	SCCP3 Sync Output
00101	SCCP4 Sync Output
00110	SCCP5 Sync Output
00111	SCCP6 Sync Output
01000	SCCP7 Sync Output
01001	INT0
01010	INT1
01011	INT2
01100 to 01111	Unused
10000	CLC1 Output(1)
10010	CLC2 Output(1)
10011	CLC3 Output(1)
10100	CLC4 Output(1)
10101 to 10111	Unused
11000	Comparator 3 Trigger
11001	Comparator 2 Trigger
11010	Comparator 1 Trigger
11011	A/D(1)
11100	CTMU Trigger
11101 and 11110	Unused
11111	None; Timer with Auto-Rollover (FFFFh → 0000h)

Note 1: These sources are only available when the source module is being used in a Synchronous mode.

REGISTER 17-3: SPIxCON2L: SPIx CONTROL REGISTER 2 LOW

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	WLENGTH<4:0>(1,2)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **WLENGTH<4:0>:** Variable Word Length bits(1,2)

11111 = 32-bit data
11110 = 31-bit data
11101 = 30-bit data
11100 = 29-bit data
11011 = 28-bit data
11010 = 27-bit data
11001 = 26-bit data
11000 = 25-bit data
10111 = 24-bit data
10110 = 23-bit data
10101 = 22-bit data
10100 = 21-bit data
10011 = 20-bit data
10010 = 19-bit data
10001 = 18-bit data
10000 = 17-bit data
01111 = 16-bit data
01110 = 15-bit data
01101 = 14-bit data
01100 = 13-bit data
01011 = 12-bit data
01010 = 11-bit data
01001 = 10-bit data
01000 = 9-bit data
00111 = 8-bit data
00110 = 7-bit data
00101 = 6-bit data
00100 = 5-bit data
00011 = 4-bit data
00010 = 3-bit data
00001 = 2-bit data
00000 = See MODE<32,16> bits in SPIxCON1L<11:10>

Note 1: These bits are effective when AUDEN = 0 only.

2: Varying the length by changing these bits does not affect the depth of the TX/RX FIFO.

20.3 USB Interrupts

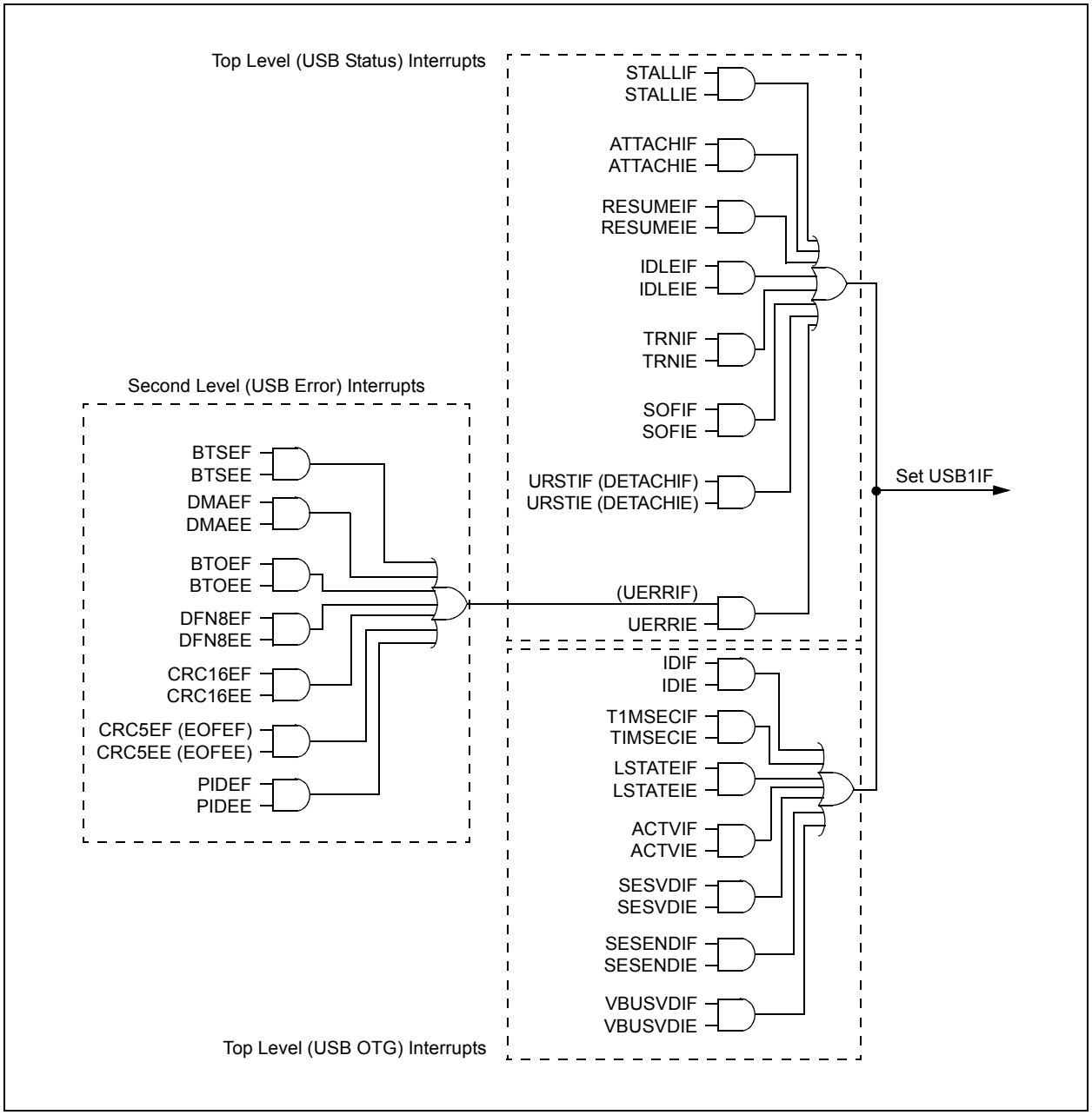
The USB OTG module has many conditions that can be configured to cause an interrupt. All interrupt sources use the same interrupt vector.

Figure 20-8 shows the interrupt logic for the USB module. There are two layers of interrupt registers in the USB module. The top level consists of overall USB status interrupts; these are enabled and flagged in the U1IE and U1IR registers, respectively. The second level consists of USB error conditions, which are enabled and flagged in the U1EIR and U1EIE registers.

An interrupt condition in any of these triggers a USB Error Interrupt Flag (UERRIF) in the top level. Unlike the device-level interrupt flags in the IFSx registers, USB interrupt flags in the U1IR registers can only be cleared by writing a '1' to the bit position.

Interrupts may be used to trap routine events in a USB transaction. Figure 20-9 provides some common events within a USB frame and their corresponding interrupts.

FIGURE 20-8: USB OTG INTERRUPT FUNNEL



REGISTER 20-8: U1CON: USB CONTROL REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-x, HSC	R-x, HSC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
JSTATE	SE0	TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST	SOFEN
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **JSTATE:** Live Differential Receiver J-State Flag bit
- 1 = J-state (differential '0' in low speed, differential '1' in full speed) is detected on the USB
- 0 = No J-state is detected

bit 6 **SE0:** Live Single-Ended Zero Flag bit
- 1 = Single-ended zero is active on the USB bus
- 0 = No single-ended zero is detected

bit 5 **TOKBUSY:** Token Busy Status bit
- 1 = Token is being executed by the USB module in On-The-Go state
- 0 = No token is being executed

bit 4 **USBRST:** USB Module Reset bit
- 1 = USB Reset has been generated for a software Reset; application must set this bit for 50 ms, then clear it
- 0 = USB Reset is terminated

bit 3 **HOSTEN:** Host Mode Enable bit
- 1 = USB host capability is enabled; pull-downs on D+ and D- are activated in hardware
- 0 = USB host capability is disabled

bit 2 **RESUME:** Resume Signaling Enable bit
- 1 = Resume signaling is activated; software must set bit for 10 ms and then clear to enable remote wake-up
- 0 = Resume signaling is disabled

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
- 1 = Resets all Ping-Pong Buffer Pointers to the even BD banks
- 0 = Ping-Pong Buffer Pointers are not reset

bit 0 **SOFEN:** Start-of-Frame Enable bit
- 1 = Start-of-Frame token is sent every one 1 ms
- 0 = Start-of-Frame token is disabled

24.1 RTCC Source Clock

The RTCC clock divider block converts the incoming oscillator source into an accurate 1/2 second clock for the RTCC timer. The clock divider is optimized to work with four different oscillator sources:

- System clock, up to 32 MHz
- 32.768 kHz crystal oscillator
- 31 kHz Low-Power RC Oscillator (LPRC)
- External 50 Hz or 60 Hz power line frequency

An asynchronous prescaler, PS<1:0> (RTCCON2L<5:4>), is provided that allows the RTCC to work with higher speed clock sources, such as the system clock. Divide ratios of 1:16, 1:64 or 1:256 may be selected, allowing sources up to 32 MHz to clock the RTCC.

24.1.1 SELECTING RTCC CLOCK SOURCE

The clock source for the RTCC module can be selected using the CLKSEL<1:0> bits in the RTCCON2L register. When the bits are set to '00', the Secondary Oscillator (SOSC) is used as the reference clock and when the bits are '01', LPRC is used as the reference clock. When CLKSEL<1:0> = 10, the external power line (50 Hz and 60 Hz) is used as the clock source. When CLKSEL<1:0> = 11, the system clock is used as the clock source.

24.1.2 COARSE FREQUENCY DIVISION

The clock divider block has a 16-bit counter used to divide the input clock frequency. The divide ratio is set by the DIV<15:0> register bits (RTCCON2H<15:0>). The DIV<15:0> bits should be programmed with a value to produce a nominal 1/2 second clock divider count period.

24.1.3 FINE FREQUENCY DIVISION

The fine frequency division is set using the FDIV<4:0> (RTCCON2L<15:11>) bits. Increasing the FDIVx value will lengthen the overall clock divider period.

If FDIV<4:0> = 00000, the fine frequency division circuit is effectively disabled. Otherwise, it will optionally remove a clock pulse from the input of the clock divider every 1/2 second. This functionality will allow the user to remove up to 31 pulses over a fixed period of 16 seconds, depending on the value of FDIVx.

The value for DIV<15:0> is calculated as shown in Equation 24-1. The fractional remainder of the DIV<15:0> calculation result can be used to calculate the value for FDIV<4:0>.

EQUATION 24-1: RTCC CLOCK DIVIDER OUTPUT FREQUENCY

$$F_{OUT} = \frac{F_{IN}}{2 \bullet (PS\text{<1:0>}\ Prescaler) \bullet (DIV\text{<15:0>} + 1) + \left(\frac{FDIV\text{<4:0>}}{32}\right)}$$

The DIV<15:0> value is the integer part of this calculation:

$$DIV\text{<15:0>} = \left(\frac{F_{IN}}{2 \bullet (PS\text{<1:0>}\ Prescaler)}\right) - 1$$

The FDIV<4:0> value is the fractional part of the DIV<15:0> calculation, multiplied by 32.

24.1.4 CLOCK SOURCE CALIBRATION

A crystal oscillator that is connected to the RTCC may be calibrated to provide an accurate 1-second clock in two ways. First, coarse frequency adjustment is performed by adjusting the value written to the DIV<15:0> bits. Secondly, a 5-bit value can be written to the FDIV<4:0> control bits to perform a fine clock division.

The DIVx and FDIVx values can be concatenated and considered as a 21-bit prescaler value. If the oscillator source is slightly faster than ideal, the FDIV<4:0> value can be increased to make a small decrease in the RTC frequency. The value of DIV<15:0> should be increased to make larger decreases in the RTC frequency. If the oscillator source is slower than ideal, FDIV<4:0> may be decreased for small calibration changes and DIV<15:0> may need to be decreased to make larger calibration changes.

Before calibration, the user must determine the error of the crystal. This should be done using another timer resource on the device or an external timing reference. It is up to the user to include in the error value the initial error of the crystal, drift due to temperature and drift due to crystal aging.

REGISTER 25-5: CFGPAGE: SECURE ARRAY CONFIGURATION BITS (OTP PAGE 0) REGISTER (CONTINUED)

bit 21-20 **KEY1TYPE<1:0>:** Key Type for OTP Pages 1 and 2 bits
11 = Keys in these pages are for 192-bit/256-bit AES operations only
10 = Keys in these pages are for 128-bit AES operations only
01 = Keys in these pages are for 3DES operations only
00 = Keys in these pages are for DES/2DES operations only

bit 19 **SKEYEN:** Session Key Enable bit
1 = Stored Key #1 may be used only as a Key Encryption Key
0 = Stored Key #1 may be used for any operation

bit 18-11 **LKYSRC<7:0>:** Locked Key Source Configuration bits
If SRCLCK = 1:
1xxxxxxx = Key source is as if KEYSRC<3:0> = 1111
01xxxxxx = Key source is as if KEYSRC<3:0> = 0111
001xxxxx = Key source is as if KEYSRC<3:0> = 0110
0001xxxx = Key source is as if KEYSRC<3:0> = 0101
00001xxx = Key source is as if KEYSRC<3:0> = 0100
000001xx = Key source is as if KEYSRC<3:0> = 0011
0000001x = Key source is as if KEYSRC<3:0> = 0010
00000001 = Key source is as if KEYSRC<3:0> = 0001
00000000 = Key source is as if KEYSRC<3:0> = 0000
If SRCLCK = 0:
These bits are ignored.

bit 10 **SRCLCK:** Key Source Lock bit
1 = The key source is determined by the LKYSRC<7:0> bits (software key selection is disabled)
0 = The key source is determined by the KEYSRC<3:0> (CRYCONH<3:0>) bits (locked key selection is disabled)

bit 9-1 **WRLOCK<8:0>:** Write Lock Page Enable bits
For OTP Pages 0 (CFGPAGE) through 8:
1 = OTP Page is permanently locked and may not be programmed
0 = OTP Page is unlocked and may be programmed

bit 0 **SWKYDIS:** Software Key Disable bit
1 = Software key (CRYKEY register) is disabled; when KEYSRC<3:0> = 0000, the KEYFAIL status bit will be set and no encryption/decryption/session key operations can be started until KEYSRC<3:0> bits are changed to a value other than '0000'
0 = Software key (CRYKEY register) can be used as a key source when KEYSRC<3:0> = 0000

Note 1: This bit's state is mirrored by the PGMTST bit (CRYOTP<7>).

FIGURE 27-2: EXAMPLE OF BUFFER ADDRESS GENERATION IN PIA MODE (4-WORD BUFFERS PER CHANNEL)

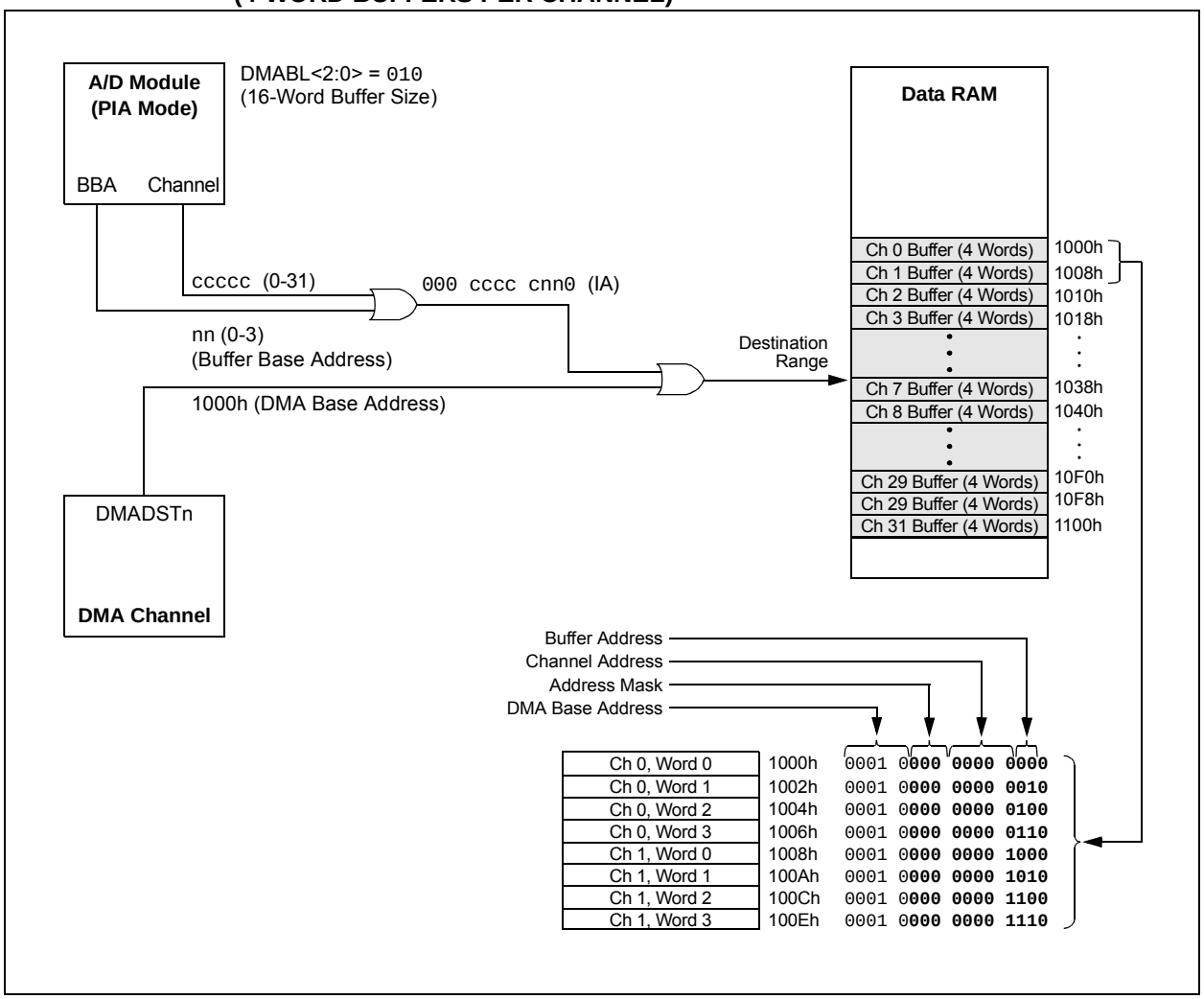


TABLE 27-1: INDIRECT ADDRESS GENERATION IN PIA MODE

DMABL<2:0>	Buffer Size per Channel (words)	Generated Offset Address (lower 11 bits)	Available Input Channels	Allowable DMADSTn Addresses
000	1	000 00cc ccc0	32	xxxx xxxx xx00 0000
001	2	000 0ccc ccn0	32	xxxx xxxx x000 0000
010	4	000 cccc cnn0	32	xxxx xxxx 0000 0000
011	8	00c cccc nnn0	32	xxxx xxx0 0000 0000
100	16	0cc cccn nnn0	32	xxxx xx00 0000 0000
101	32	ccc ccnn nnn0	32	xxxx x000 0000 0000
110	64	ccc cnnn nnn0	16	xxxx x000 0000 0000
111	128	ccc nnnn nnn0	8	xxxx x000 0000 0000

Legend: ccc = Channel number (three to five bits), n = Base buffer address (zero to seven bits), x = User-definable range of DMADSTn for base address, 0 = Masked bits of DMADSTn for IA.

34.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta , flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

34.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

TABLE 36-21: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
OS50	FPLLI	PLL Input Frequency Range(1)	1.97	4	4.04	MHz	ECPLL, XTPLL, HSPLL or FRCPLL modes
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	128	µs	
OS53	DCLK	CLKO Stability (Jitter)	-0.25	—	0.25	%	

Note 1: The PLL accepts a 1.97 MHz to 4.04 MHz input frequency. Higher input frequencies, up to 48 MHz, may be supplied to the PLL if they are prescaled down by the PLLMODE<3:0> Configuration bits into the 1.97 MHz to 4.04 MHz range.

TABLE 36-22: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Characteristic	Min	Typ	Max	Units	Conditions
F20	FRC Accuracy @ 8 MHz(4)	-1	±0.15	1	%	2.0V ≤ VDD ≤ 3.6V, 0°C ≤ TA ≤ +85°C **(Note 1)**
		-1.5	—	1.5	%	2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA < 0°C
		-0.20	±0.05	0.20	%	2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C, self-tune is enabled and locked **(Note 2)**
F21	LPRC @ 31 kHz	-20	—	20	%	
F22	OSCTUN Step-Size	—	0.05	—	%/bit	
F23	FRC Self-Tune Lock Time	—	<5	8	ms	**(Note 3)**

Note 1: To achieve this accuracy, physical stress applied to the microcontroller package (ex., by flexing the PCB) must be kept to a minimum.

2: Accuracy measured with respect to reference source accuracy.

3: Time from when the reference clock is stable and in range until the FRC is tuned within the range specified by F20 (with self-tune).

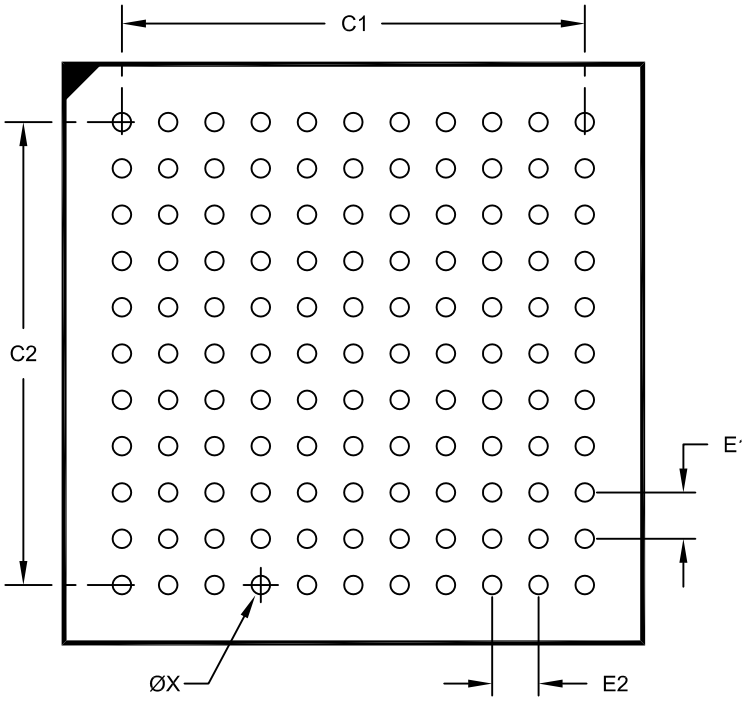
4: Other frequencies that are derived from the FRC (either through digital division by prescalers or multiplication through a PLL) will also have the same accuracy tolerance specifications as provided here.

TABLE 36-23: RC OSCILLATOR START-UP TIME

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
FR0	TFRC	FRC Oscillator Start-up Time	—	15	—	µs	
FR1	TLPRC	Low-Power RC Oscillator Start-up Time	—	50	—	µs	

121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA--Formerly XBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E1		0.80 BSC	
Contact Pitch	E2		0.80 BSC	
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Diameter (X121)	X			0.32

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2148 Rev D