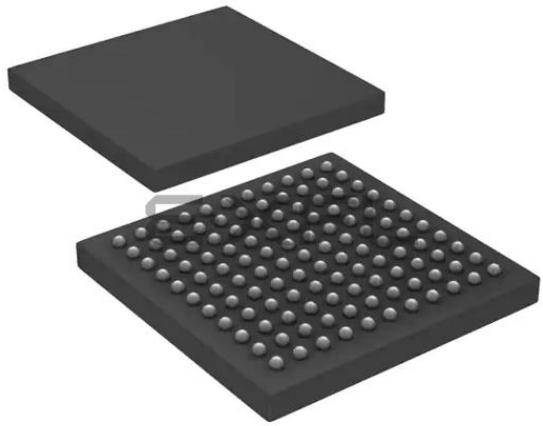
Microchip Technology - PIC24FJ256GB412T-I/BG Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	101
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256gb412t-i-bg

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
RE0	60	93	A4	I/O	DIG/ST	PORTE Digital I/Os
RE1	61	94	B4	I/O	DIG/ST	
RE2	62	98	B3	I/O	DIG/ST	
RE3	63	99	A2	I/O	DIG/ST	
RE4	64	100	A1	I/O	DIG/ST	
RE5	1	3	D3	I/O	DIG/ST	
RE6	2	4	C1	I/O	DIG/ST	
RE7	3	5	D2	I/O	DIG/ST	
RE8	—	18	G1	I/O	DIG/ST	
RE9	—	19	G2	I/O	DIG/ST	
REFI1	24	35	K5	I	ST	Reference Clock Input
RF0	58	87	B6	I/O	DIG/ST	PORTF Digital I/Os
RF1	59	88	A6	I/O	DIG/ST	
RF2	34	52	K11	I/O	DIG/ST	
RF3	33	51	K10	I/O	DIG/ST/TTL	
RF4	31	49	L10	I/O	DIG/ST	
RF5	32	50	L11	I/O	DIG/ST	
RF6	35	55	H9	I/O	DIG/ST	
RF7	—	54	H8	I/O	DIG/ST	
RF8	—	53	J10	I/O	DIG/ST	
RF12	—	40	K6	I/O	DIG/ST	
RF13	—	39	L6	I/O	DIG/ST	
RG0	—	90	A5	I/O	DIG/ST	PORTG Digital I/Os
RG1	—	89	E6	I/O	DIG/ST	
RG2	37	57	H10	I/O	DIG/ST	
RG3	36	56	J11	I/O	DIG/ST	
RG6	4	10	E3	I/O	DIG/ST/TTL	
RG7	5	11	F4	I/O	DIG/ST	
RG8	6	12	F2	I/O	DIG/ST	
RG9	8	14	F3	I/O	DIG/ST	
RG12	—	96	E17	I/O	DIG/ST	
RG13	—	97	E18	I/O	DIG/ST	
RG14	—	95	E16	I/O	DIG/ST	
RG15	—	1	B2	I/O	DIG/ST	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

TABLE 4-10: SFR BLOCK 500h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
DMA (Continued)			CRYTXTB6	564	xxxxxxxxxxxxxxxx	U1EP8(1)	5B2	0000000000000000
DMAINT5	500	0000000000000000	CRYTXTB7	566	xxxxxxxxxxxxxxxx	U1EP9(1)	5B4	0000000000000000
DMASRC5	502	0000000000000000	CRYTXTC0	558	xxxxxxxxxxxxxxxx	U1EP10(1)	5B6	0000000000000000
DMADST5	504	0000000000000000	CRYTXTC1	56A	xxxxxxxxxxxxxxxx	U1EP11(1)	5B8	0000000000000000
DMACNT5	506	0000000000000001	CRYTXTC2	56C	xxxxxxxxxxxxxxxx	U1EP12(1)	5BA	0000000000000000
Cryptographic Engine			CRYTXTC3	56E	xxxxxxxxxxxxxxxx	U1EP13(1)	5BC	0000000000000000
CRYCONL	51C	x0xxxx0xxxxxxxxx	CRYTXTC4	570	xxxxxxxxxxxxxxxx	U1EP14(1)	5BE	0000000000000000
CRYCONH	51E	0xxxxxxxxxx0xxxx	CRYTXTC5	572	xxxxxxxxxxxxxxxx	U1EP15(1)	5C0	0000000000000000
CRYSTAT	520	00000000xxxx0xxx	CRYTXTC6	574	xxxxxxxxxxxxxxxx	**LCD Controller**		
CRYOTP	524	00000000xxxxxxxx	CRYTXTC7	576	xxxxxxxxxxxxxxxx	LCDCON	5C2	0000000000000000(2)
CRYKEY0	528	xxxxxxxxxxxxxxxx	**USB**			LCDREF	5C4	0000000000000000(2)
CRYKEY1	52A	xxxxxxxxxxxxxxxx	U1OTGIR(1)	578	0000000000000000	LCDPS	5C6	0000000000000000(2)
CRYKEY2	52C	xxxxxxxxxxxxxxxx	U1OTGIE(1)	57A	0000000000000000	LCDDATA0	5C8	0000000000000000(2)
CRYKEY3	52E	xxxxxxxxxxxxxxxx	U1OTGSTAT(1)	57C	0000000000000000	LCDDATA1	5CA	0000000000000000(2)
CRYKEY4	530	xxxxxxxxxxxxxxxx	U1OTGCON(1)	57E	0000000000000000	LCDDATA2	5CC	0000000000000000(2)
CRYKEY5	532	xxxxxxxxxxxxxxxx	U1PWRC(1)	580	00000000x0000000	LCDDATA3	5CE	0000000000000000(2)
CRYKEY6	534	xxxxxxxxxxxxxxxx	U1IR(1)	582	0000000000000000	LCDDATA4	5D0	0000000000000000(2)
CRYKEY7	536	xxxxxxxxxxxxxxxx	U1IE(1)	584	0000000000000000	LCDDATA5	5D2	0000000000000000(2)
CRYKEY8	538	xxxxxxxxxxxxxxxx	U1EIR(1)	586	0000000000000000	LCDDATA6	5D4	0000000000000000(2)
CRYKEY9	53A	xxxxxxxxxxxxxxxx	U1EIE(1)	588	0000000000000000	LCDDATA7	5D6	0000000000000000(2)
CRYKEY10	53C	xxxxxxxxxxxxxxxx	U1STAT(1)	58A	0000000000000000	LCDDATA8	5D8	0000000000000000(2)
CRYKEY11	53E	xxxxxxxxxxxxxxxx	U1CON(1)	58C	00000000xx000000	LCDDATA9	5DA	0000000000000000(2)
CRYKEY12	540	xxxxxxxxxxxxxxxx	U1ADDR(1)	58E	000000000xxxxxxx	LCDDATA10	5DC	0000000000000000(2)
CRYKEY13	542	xxxxxxxxxxxxxxxx	U1BDTP1(1)	590	0000000000000000	LCDDATA11	5DE	0000000000000000(2)
CRYKEY14	544	xxxxxxxxxxxxxxxx	U1FRML(1)	592	0000000000000000	LCDDATA12	5E0	0000000000000000(2)
CRYKEY15	546	xxxxxxxxxxxxxxxx	U1FRMH(1)	594	0000000000000000	LCDDATA13	5E2	0000000000000000(2)
CRYTXTA0	548	xxxxxxxxxxxxxxxx	U1TOK(1)	596	0000000000000000	LCDDATA14	5E4	0000000000000000(2)
CRYTXTA1	54A	xxxxxxxxxxxxxxxx	U1SOF(1)	598	0000000000000000	LCDDATA15	5E6	0000000000000000(2)
CRYTXTA2	54C	xxxxxxxxxxxxxxxx	U1BDTP2(1)	59A	0000000000000000	LCDDATA16	5E8	0000000000000000(2)
CRYTXTA3	54E	xxxxxxxxxxxxxxxx	U1BDTP3(1)	59C	0000000000000000	LCDDATA17	5EA	0000000000000000(2)
CRYTXTA4	550	xxxxxxxxxxxxxxxx	U1CNFG1(1)	59E	0000000000000000	LCDDATA18	5EC	0000000000000000(2)
CRYTXTA5	552	xxxxxxxxxxxxxxxx	U1CNFG2(1)	5A0	0000000000000000	LCDDATA19	5EE	0000000000000000(2)
CRYTXTA6	554	xxxxxxxxxxxxxxxx	U1EP0(1)	5A2	0000000000000000	LCDDATA20	5F0	0000000000000000(2)
CRYTXTA7	556	xxxxxxxxxxxxxxxx	U1EP1(1)	5A4	0000000000000000	LCDDATA21	5F2	0000000000000000(2)
CRYTXTB0	558	xxxxxxxxxxxxxxxx	U1EP2(1)	5A6	0000000000000000	LCDDATA22	5F4	0000000000000000(2)
CRYTXTB1	55A	xxxxxxxxxxxxxxxx	U1EP3(1)	5A8	0000000000000000	LCDDATA23	5F6	0000000000000000(2)
CRYTXTB2	55C	xxxxxxxxxxxxxxxx	U1EP4(1)	5AA	0000000000000000	LCDDATA24	5F8	0000000000000000(2)
CRYTXTB3	55E	xxxxxxxxxxxxxxxx	U1EP5(1)	5AC	0000000000000000	LCDDATA25	5FA	0000000000000000(2)
CRYTXTB4	560	xxxxxxxxxxxxxxxx	U1EP6(1)	5AE	0000000000000000	LCDDATA26	5FC	0000000000000000(2)
CRYTXTB5	562	xxxxxxxxxxxxxxxx	U1EP7(1)	5B0	0000000000000000	LCDDATA27	5FE	0000000000000000(2)

Legend: x = unknown or indeterminate value. Reset and address values are in hexadecimal.

Note 1: Implemented in PIC24FJXXXGB4XX devices only.

2: LCD registers are only reset on a device POR.

TABLE 4-11: SFR BLOCK 600h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
LCD Controller (Continued)			IOCPDB	684	0000000000000000	PORTF	6C4	0000000000000000
LCDDATA28	600	0000000000000000(1)	TRISC	686	1001000000011110	LATF	6C6	0000000000000000
LCDDATA29	602	0000000000000000(1)	PORTC	688	0000000000000000	ODCF	6C8	0000000000000000
LCDDATA30	604	0000000000000000(1)	LATC	68A	0000000000000000	ANSF	6CA	0011000100111111
LCDDATA31	606	0000000000000000(1)	ODCC	68C	0000000000000000	IOCPF	6CC	0000000000000000
LCDSE0	608	0000000000000000(1)	ANSC	68E	0000000000011110	IOCNF	6CE	0000000000000000
LCDSE1	60A	0000000000000000(1)	IOCPC	690	0000000000000000	IOCFF	6D0	0000000000000000
LCDSE2	60C	0000000000000000(1)	IOCNC	692	0000000000000000	IOCPUF	6D2	0000000000000000
LCDSE3	60E	0000000000000000(1)	IOCFC	694	0000000000000000	IOCPDF	6D4	0000000000000000
LCDREG	610	0000000000000000(1)	IOCPUC	696	0000000000000000	TRISG	6D6	1111001111001111
I/O(3)			IOCPDC	698	0000000000000000	PORTG	6D8	0000000000000000
PADCON	65A	0000000000000000	TRISD	69A	1111111111111111	LATG	6DA	0000000000000000
IOCSTAT	65C	0000000000000000	PORTD	69C	0000000000000000	ODCG	6DC	0000000000000000
TRISA	65E	1100011011111111	LATD	69E	0000000000000000	ANSG	6DE	1111001111000011
PORTA	660	0000000000000000	ODCD	6A0	0000000000000000	IOCPG	6E0	0000000000000000
LATA	662	0000000000000000	ANSD	6A2	1111111111111111	IOCNG	6E2	0000000000000000
ODCA	664	0000000000000000	IOCPD	6A4	0000000000000000	IOCFG	6E4	0000000000000000
ANSA	666	1100011011101101	IOCND	6A6	0000000000000000	IOCPUG	6E6	0000000000000000
IOCPA	668	0000000000000000	IOCFD	6A8	0000000000000000	IOCPDG	6E8	0000000000000000
IOCNA	66A	0000000000000000	IOCPUD	6AA	0000000000000000	TRISH	6EA	1111111111111110
IOCFA	66C	0000000000000000	IOCPDD	6AC	0000000000000000	PORTH	6EC	0000000000000000
IOCPUA	66E	0000000000000000	TRISE	6AE	0000001111111111	LATH	6EE	0000000000000000
IOCPDA	670	0000000000000000	PORTE	6B0	0000000000000000	ODCH	6F0	0000000000000000
TRISB	672	1111111111111111	LATE	6B2	0000000000000000	ANSH	6F2	0000000000011110
PORTB	674	0000000000000000	ODCE	6B4	0000000000000000	IOCPH	6F4	0000000000000000
LATB	676	0000000000000000	ANSE	6B6	0000001111111111	IOCNH	6F6	0000000000000000
ODCB	678	0000000000000000	IOCPE	6B8	0000000000000000	IOCFH	6F8	0000000000000000
ANSB	67A	1111111111111111	IOCNE	6BA	0000000000000000	IOCPUH	6FA	0000000000000000
IOCPB	67C	0000000000000000	IOCFE	6BC	0000000000000000	IOCPDH	6FC	0000000000000000
IOCNB	67E	0000000000000000	IOCPUE	6BE	0000000000000000	TRISJ	6FE	0000000000000011
IOCFB	680	0000000000000000	IOCPDE	6C0	0000000000000000			
IOCPUB	682	0000000000000000	TRISF(2)	6C2	0011000111111111			

Legend: x = unknown or indeterminate value. Reset and address values are in hexadecimal.

Note 1: LCD registers are only reset on a device POR.

2: TRISF6 is only '1' in PIC24FJXXXGA4XX devices.

3: Reset values shown are for full pin count devices. Please refer to Table 1-4 and Table 1-5 for pin count-specific devices.

REGISTER 8-17: IEC3: INTERRUPT ENABLE CONTROL REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CCP1IE	RTCIE	DMA5IE	SPI3RXIE	SPI2RXIE	SPI1RXIE	SPI4RXIE	KEYSTRIE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
CRYDNIE	INT4IE(1)	INT3IE(1)	—	CCT7IE	MI2C2IE	SI2C2IE	CCT6IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CCP1IE:** MCCP1 Capture/Compare Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 14 **RTCIE:** Real-Time Clock and Calendar Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13 **DMA5IE:** DMA Channel 5 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12 **SPI3RXIE:** SPI3 Receive Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 11 **SPI2RXIE:** SPI2 Receive Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 10 **SPI1RXIE:** SPI1 Receive Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 9 **SPI4RXIE:** SPI4 Receive Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 8 **KEYSTRIE:** Cryptographic Key Store Program Done Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 7 **CRYDNIE:** Cryptographic Operation Done Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 6 **INT4IE:** External Interrupt 4 Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 5 **INT3IE:** External Interrupt 3 Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 4 **Unimplemented:** Read as '0'

Note 1: If an external interrupt is enabled, the interrupt input must also be configured to an available RPn or RPIn pin. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

REGISTER 8-19: IEC5: INTERRUPT ENABLE CONTROL REGISTER 5 (CONTINUED)

bit 3 **U3TXIE:** UART3 Transmitter Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **U3RXIE:** UART3 Receiver Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **U3ERIE:** UART3 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **Unimplemented:** Read as '0'

REGISTER 8-25: IPC3: INTERRUPT PRIORITY CONTROL REGISTER 3

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	NVMIP2	NVMIP1	NVMIP0	—	DMA1IP2	DMA1IP1	DMA1IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	AD1IP2	AD1IP1	AD1IP0	—	U1TXIP2	U1TXIP1	U1TXIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-11 **NVMIP<2:0>:** Flash Memory Write/Program Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 10-8 **DMA1IP<2:0>:** DMA Channel 1 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **AD1IP<2:0>:** 12-Bit Pipeline A/D Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **U1TXIP<2:0>:** UART1 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-50: IPC28: INTERRUPT PRIORITY CONTROL REGISTER 28

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U6TXIP2	U6TXIP1	U6TXIP0	—	U6RXIP2	U6RXIP1	U6RXIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U5ERIP2	U5ERIP1	U5ERIP0	—	U5TXIP2	U5TXIP1	U5TXIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **U6TXIP<2:0>:** UART6 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **U6RXIP<2:0>:** UART6 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **U5ERIP<2:0>:** UART5 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **U5TXIP<2:0>:** UART5 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 11-23: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP1R5	RP1R4	RP1R3	RP1R2	RP1R1	RP1R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP0R5	RP0R4	RP0R3	RP0R2	RP0R1	RP0R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP1R<5:0>:** RP1 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP1 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP0R<5:0>:** RP0 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP0 (see Table 11-12 for peripheral function numbers).

REGISTER 11-24: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP3R5	RP3R4	RP3R3	RP3R2	RP3R1	RP3R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP2R5	RP2R4	RP2R3	RP2R2	RP2R1	RP2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP3R<5:0>:** RP3 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP3 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP2R<5:0>:** RP2 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP2 (see Table 11-12 for peripheral function numbers).

REGISTER 11-25: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP5R5(1)	RP5R4(1)	RP5R3(1)	RP5R2(1)	RP5R1(1)	RP5R0(1)
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP4R5	RP4R4	RP4R3	RP4R2	RP4R1	RP4R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP5R<5:0>:** RP5 Output Pin Mapping bits(1)
Peripheral Output Number n is assigned to pin, RP5 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP4R<5:0>:** RP4 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP4 (see Table 11-12 for peripheral function numbers).

Note 1: RP5 and its associated bits are not available on PIC24FJXXXGA/GB406 devices.

REGISTER 11-26: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP7R5	RP7R4	RP7R3	RP7R2	RP7R1	RP7R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP6R5	RP6R4	RP6R3	RP6R2	RP6R1	RP6R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP7R<5:0>:** RP7 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP7 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP6R<5:0>:** RP6 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP6 (see Table 11-12 for peripheral function numbers).

REGISTER 15-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Synchronization/Trigger Source Selection bits

1111x = Reserved
11101 = Reserved
11100 = CTMU(1)
11011 = A/D(1)
11010 = Comparator 3(1)
11001 = Comparator 2(1)
11000 = Comparator 1(1)
10111 = SCCP5 capture/compare
10110 = SCCP4 capture/compare
10101 = SCCP3 capture/compare
10100 = SCCP2 capture/compare
10011 = MCCP1 capture/compare
10010 = Input Capture 3(2)
10001 = Input Capture 2(2)
10000 = Input Capture 1(2)
01111 = SCCP7 capture/compare
01110 = SCCP6 capture/compare
01101 = Timer3
01100 = Timer2
01011 = Timer1
01010 = SCCP7 sync/trigger
01001 = SCCP6 sync/trigger
01000 = SCCP5 sync/trigger
00111 = SCCP4 sync/trigger
00110 = SCCP3 sync/trigger
00101 = SCCP2 sync/trigger
00100 = MCCP1 sync/trigger
00011 = Output Compare 3
00010 = Output Compare 2
00001 = Output Compare 1
00000 = Not synchronized to any other module

Note 1: Use these inputs as trigger sources only and never as sync sources.
2: Never use an ICx module as its own trigger source by selecting this mode.

19.2 Transmitting in 8-Bit Data Mode

1. Set up the UARTx:
   a) Write appropriate values for data, parity and Stop bits.
   b) Write appropriate baud rate value to the UxBRG register.
   c) Set up transmit and receive interrupt enable and priority bits.
2. Enable the UARTx.
3. Set the UTXEN bit (causes a transmit interrupt, two cycles after being set).
4. Write a data byte to the lower byte of the UxTXREG word. The value will be immediately transferred to the Transmit Shift Register (TSR) and the serial bit stream will start shifting out with the next rising edge of the baud clock.
5. Alternatively, the data byte may be transferred while UTXEN = 0 and then the user may set UTXEN. This will cause the serial bit stream to begin immediately because the baud clock will start from a cleared state.
6. A transmit interrupt will be generated as per interrupt control bits, UTXISEL<1:0>.

19.3 Transmitting in 9-Bit Data Mode

1. Set up the UARTx (as described in **Section 19.2 "Transmitting in 8-Bit Data Mode"**).
2. Enable the UARTx.
3. Set the UTXEN bit (causes a transmit interrupt).
4. Write UxTXREG as a 16-bit value only.
5. A word write to UxTXREG triggers the transfer of the 9-bit data to the TSR. The serial bit stream will start shifting out with the first rising edge of the baud clock.
6. A transmit interrupt will be generated as per the setting of control bits, UTXISELx.

19.4 Break and Sync Transmit Sequence

The following sequence will send a message frame header, made up of a Break, followed by an auto-baud Sync byte.

1. Configure the UARTx for the desired mode.
2. Set UTXEN and UTXBRK to set up the Break character.
3. Load the UxTXREG with a dummy character to initiate transmission (value is ignored).
4. Write 55h to UxTXREG; this loads the Sync character into the transmit FIFO.
5. After the Break has been sent, the UTXBRK bit is reset by hardware. The Sync character now transmits.

19.5 Receiving in 8-Bit or 9-Bit Data Mode

1. Set up the UARTx (as described in **Section 19.2 "Transmitting in 8-Bit Data Mode"**).
2. Enable the UARTx.
3. Set the URXEN bit (UxSTAL<12>).
4. A receive interrupt will be generated when one or more data characters have been received as per interrupt control bits, URXISEL<1:0>.
5. Read the OERR bit to determine if an overrun error has occurred. The OERR bit must be reset in software.
6. Read UxRXREG.

The act of reading the UxRXREG character will move the next character to the top of the receive FIFO, including a new set of PERR and FERR values.

19.6 Operation of $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Control Pins

UARTx Clear-to-Send ($\overline{\text{UxCTS}}$) and Request-to-Send ($\overline{\text{UxRTS}}$) are the two hardware controlled pins that are associated with the UARTx modules. These two pins allow the UARTx to operate in Simplex and Flow Control mode. They are implemented to control the transmission and reception between the Data Terminal Equipment (DTE). The UEN<1:0> bits in the UxMODE register configure these pins.

19.7 Infrared Support

The UARTx module provides two types of infrared UART support: one is the IrDA clock output to support an external IrDA encoder and decoder device (legacy module support), and the other is the full implementation of the IrDA encoder and decoder. Note that because the IrDA modes require a 16x baud clock, they will only work when the BRGH bit (UxMODE<3>) is '0'.

19.7.1 IrDA CLOCK OUTPUT FOR EXTERNAL IrDA SUPPORT

To support external IrDA encoder and decoder devices, the UxBCLK pin (same as the $\overline{\text{UxRTS}}$ pin) can be configured to generate the 16x baud clock. With UEN<1:0> = 11, the UxBCLK pin will output the 16x baud clock if the UARTx module is enabled. It can be used to support the IrDA codec chip.

19.7.2 BUILT-IN IrDA ENCODER AND DECODER

The UARTx has full implementation of the IrDA encoder and decoder as part of the UARTx module. The built-in IrDA encoder and decoder functionality is enabled using the IREN bit (UxMODE<12>). When enabled (IREN = 1), the receive pin (UxRX) acts as the input from the infrared receiver. The transmit pin (UxTX) acts as the output to the infrared transmitter.

REGISTER 21-8: PMSTAT: EPMP STATUS REGISTER (SLAVE MODE ONLY)

R-0, HSC	R/W-0, HS	U-0	U-0	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IBF	IBOV	—	—	IB3F(1)	IB2F(1)	IB1F(1)	IB0F(1)
bit 15							bit 8

R-1, HSC	R/W-0, HS	U-0	U-0	R-1, HSC	R-1, HSC	R-1, HSC	R-1, HSC
OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E
bit 7							bit 0

Legend:	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **IBF:** Input Buffer Full Status bit
1 = All writable Input Buffer registers are full
0 = Some or all of the writable Input Buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
1 = A write attempt to a full Input register occurred (must be cleared in software)
0 = No overflow occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IB3F:IB0F:** Input Buffer x Status Full bits(1)
1 = Input buffer contains unread data (reading the buffer will clear this bit)
0 = Input buffer does not contain unread data

bit 7 **OBE:** Output Buffer Empty Status bit
1 = All readable Output Buffer registers are empty
0 = Some or all of the readable Output Buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
1 = A read occurred from an empty Output Buffer register (must be cleared in software)
0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OB3E:OB0E:** Output Buffer x Status Empty bits
1 = Output buffer is empty (writing data to the buffer will clear this bit)
0 = Output buffer contains untransmitted data

Note 1: Even though an individual bit represents the byte in the buffer, the bits corresponding to the word (Byte 0 and 1, or Byte 2 and 3) get cleared, even on byte reading.

TABLE 22-1: LCDDATA REGISTERS AND BITS FOR SEGMENT AND COM COMBINATIONS

COM Lines	Segments			
	0 to 15	16 to 31	32 to 47	48 to 64
0	LCDDATA0 S00C0:S15C0	LCDDATA1 S16C0:S31C0	LCDDATA2 S32C0:S47C0	LCDDATA3 S48C0:S63C0
1	LCDDATA4 S00C1:S15C1	LCDDATA5 S16C1:S31C1	LCDDATA6 S32C1:S47C1	LCDDATA7 S48C1:S63C1
2	LCDDATA8 S00C2:S15C2	LCDDATA9 S16C2:S31C2	LCDDATA10 S32C2:S47C2	LCDDATA11 S48C2:S63C2
3	LCDDATA12 S00C3:S15C3	LCDDATA13 S16C3:S31C3	LCDDATA14 S32C3:S47C3	LCDDATA15 S48C3:S63C3
4	LCDDATA16 S00C4:S15C4	LCDDATA17 S16C4:S31C4	LCDDATA18 S32C4:S47C4	LCDDATA19 S48C4:S59C4
5	LCDDATA20 S00C5:S15C5	LCDDATA21 S16C5:S31C5	LCDDATA22 S32C5:S47C5	LCDDATA23 S48C5:S69C5
6	LCDDATA24 S00C6:S15C6	LCDDATA25 S16C6:S31C6	LCDDATA26 S32C6:S47C6	LCDDATA27 S48C6:S59C6
7	LCDDATA28 S00C7:S15C7	LCDDATA29 S16C7:S31C7	LCDDATA30 S32C7:S47C7	LCDDATA31 S48C7:S59C7

25.4 Encrypting Data

1. If not already set, set the CRYON bit.
2. Configure the CPHRSEL, CPHRMODx, KEYMODx and KEYSRCx bits as desired to select the proper mode and key length.
3. Set OPMOD<3:0> to '0000'.
4. If a software key is being used, write it to the CRYKEY register. It is only necessary to write the lowest *n* bits of CRYKEY for a key length of *n*, as all unused CRYKEY bits are ignored.
5. Read the KEYFAIL bit. If this bit is '1', an illegal configuration has been selected and the encrypt operation will NOT be performed.
6. Write the data to be encrypted to the appropriate CRYTXT register. For a single DES encrypt operation, it is only necessary to write the lowest 64 bits. However, for data less than the block size (64 bits for DES, 128 bits for AES), it is the responsibility of the software to properly pad the upper bits within the block.
7. Set the CRYGO bit.
8. In ECB and CBC modes, set the FREEIE bit (CRYCONL<10>) to enable the optional CRYTXTA interrupt to indicate when the next plaintext block can be loaded.
9. Poll the CRYGO bit until it is cleared or wait for the CRYDNIF module interrupt (DONEIE must be set). If other Cryptographic Engine interrupts are enabled, it will be necessary to poll the CRYGO bit to verify the interrupt source.
10. Read the encrypted block from the appropriate CRYTXT register.
11. Repeat Steps 5 through 8 to encrypt further blocks in the message with the same key.

25.5 Decrypting Data

1. If not already set, set the CRYON bit.
2. Configure the CPHRSEL, CPHRMODx, KEYMODx and KEYSRCx bits as desired to select the proper mode and key length.
3. Set OPMOD<3:0> to '0001'.
4. If a software key is being used, write the CRYKEY register. It is only necessary to write the lowest *n* bits of CRYKEY for a key length of *n*, as all unused CRYKEY bits are ignored.
5. If an AES-ECB or AES-CBC mode decryption is being performed, you must first perform an AES decryption key expansion operation.
6. Read the KEYFAIL status bit. If this bit is '1', an illegal configuration has been selected and the encrypt operation will not be performed.
7. Write the data to be decrypted into the appropriate Text/Data register. For a DES decrypt operation, it is only necessary to write the lowest 64 bits of CRYTXTB.
8. Set the CRYGO bit.
9. If this is the first decrypt operation after a Reset, or if a key storage program operation was performed after the last decrypt operation, or if the KEYMODx or KEYSRCx fields are changed, the engine will perform a new key expansion operation. This will result in extra clock cycles for the decrypt operation, but will otherwise be transparent to the application (i.e., the CRYGO bit will be cleared only after the key expansion and the decrypt operation have completed).
10. In ECB and CBC modes, set the FREEIE bit (CRYCONL<10>) to enable the optional CRYTXTA interrupt to indicate when the next plaintext block can be loaded.
11. Poll the CRYGO bit until it is cleared or wait for the CRYDNIF module interrupt (DONEIE must be set). If other Cryptographic Engine interrupts are enabled, it will be necessary to poll the CRYGO bit to verify the interrupt source.
12. Read the decrypted block out of the appropriate Text/Data register.
13. Repeat Steps 6 through 10 to encrypt further blocks in the message with the same key.

27.0 12-BIT A/D CONVERTER WITH THRESHOLD DETECT

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the 12-Bit A/D Converter, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"12-Bit A/D Converter with Threshold Detect"** (DS39739). The information in this data sheet supersedes the information in the FRM.

The 12-bit A/D Converter has the following key features:

- Successive Approximation Register (SAR) Conversion
- Conversion Speeds of up to 200 ksps
- Up to 20 Analog Input Channels (internal and external)
- Selectable 10-Bit or 12-Bit (default) Conversion Resolution
- Multiple Internal Reference Input Channels
- External Voltage Reference Input Pins
- Unipolar Differential Sample-and-Hold (S/H) Amplifier
- Automated Threshold Scan and Compare Operation to Pre-Evaluate Conversion Results
- Selectable Conversion Trigger Source
- Fixed Length (one word per channel), Configurable Conversion Result Buffer
- Four Options for Results Alignment
- Configurable Interrupt Generation
- Enhanced DMA Operations with Indirect Address Generation
- Operation During CPU Sleep and Idle modes

The 12-bit A/D Converter module is an enhanced version of the 10-bit module offered in earlier PIC24 devices. It is a Successive Approximation Register (SAR) Converter, enhanced with 12-bit resolution, a wide range of automatic sampling options, tighter integration with other analog modules and a configurable results buffer.

It also includes a unique Threshold Detect feature that allows the module itself to make simple decisions based on the conversion results, and enhanced operation with the DMA Controller through Peripheral Indirect Addressing (PIA).

A simplified block diagram for the module is shown in Figure 27-1.

27.1 Basic Operation

To perform a standard A/D conversion:

1. Configure the module:
   a) Configure port pins as analog inputs by setting the appropriate bits in the ANSx registers (see **Section 11.2 "Configuring Analog Port Pins (ANSx)"** for more information).
   b) Select the voltage reference source to match the expected range on analog inputs (AD1CON2<15:13>).
   c) Select the positive and negative multiplexer inputs for each channel (AD1CHS<15:0>).
   d) Select the analog conversion clock to match the desired data rate with the processor clock (AD1CON3<7:0>).
   e) Select the appropriate sample/conversion sequence (AD1CON1<7:4> and AD1CON3<12:8>).
   f) For Channel A scanning operations, select the positive channels to be included (AD1CSSH and AD1CSSL registers).
   g) Select how conversion results are presented in the buffer (AD1CON1<9:8> and AD1CON5 register).
   h) Select the interrupt rate (AD1CON2<6:2>).
   i) Turn on A/D module (AD1CON1<15>).
2. Configure the A/D interrupt (if required):
   a) Clear the AD1IF bit (IFS0<13>).
   b) Enable the AD1IE interrupt (IEC0<13>).
   c) Select the A/D interrupt priority (IPC3<6:4>).
3. If the module is configured for manual sampling, set the SAMP bit (AD1CON1<1>) to begin sampling.

REGISTER 33-11: FBTSEQ: BOOT SEQUENCE CONFIGURATION WORD(1)

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
IBSEQ11	IBSEQ10	IBSEQ9	IBSEQ8	IBSEQ7	IBSEQ6	IBSEQ5	IBSEQ4
bit 23							bit 16

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
IBSEQ3	IBSEQ2	IBSEQ1	IBSEQ0	BSEQ11	BSEQ10	BSEQ9	BSEQ8
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
BSEQ7	BSEQ6	BSEQ5	BSEQ4	BSEQ3	BSEQ2	BSEQ1	BSEQ0
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-12 **IBSEQ<11:0>:** Inverse Boot Sequence Number bits
The inverse of the boot sequence number (FBTSEQ<11:0>). The user is responsible for correctly calculating and programming this value.

bit 11-0 **BSEQ<11:0>:** Inverse Boot Sequence Number bits
An arbitrary value assigned by the user at device programming. On device initialization, the code segment with the lower value of the boot sequence number becomes the Active (executable) Partition.

Note 1: Implemented only when a Dual Partition mode is selected (FBOOT<1:0> is any value except '11').

34.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

34.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

34.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

34.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

34.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

TABLE 36-6: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Operating Temperature**	**VDD**	**Conditions**
Power-Down Current (IPD)						
DC60	3.24	—	µA	-40°C	2.0V	Sleep(2)
	4.08	22	µA	+25°C		
	7.81	—	µA	+60°C		
	23.25	40	µA	+85°C		
	3.20	—	µA	-40°C	3.3V	
	4.07	25	µA	+25°C		
	7.94	—	µA	+60°C		
	19.85	42	µA	+85°C		
DC61	0.07	—	µA	-40°C	2.0V	Low-Voltage Sleep(3)
	0.07	—	µA	+25°C		
	3.54	—	µA	+60°C		
	15.30	—	µA	+85°C		
	0.10	—	µA	-40°C	3.3V	
	0.06	—	µA	+25°C		
	3.68	—	µA	+60°C		
	15.65	—	µA	+85°C		
DC70	120	—	nA	-40°C	2.0V	Deep Sleep, capacitor on VCAP is fully discharged
	80	800	nA	+25°C		
	620	—	nA	+60°C		
	1.13	5	µA	+85°C		
	110	—	nA	-40°C	3.3V	
	110	1500	nA	+25°C		
	830	—	nA	+60°C		
	3.67	10	µA	+85°C		
DC74	0.6	3	µA	-40°C to +85°C	0V	RTCC with VBAT mode (LPRC/SOSC)(4)

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The low-voltage/retention regulator is disabled; RETEN (RCON<12>) = 0, $\overline{\text{LPCFG}}$ (FPOR<2>) = 1.

3: The low-voltage/retention regulator is enabled; RETEN (RCON<12>) = 1, $\overline{\text{LPCFG}}$ (FPOR<2>) = 0.

4: The VBAT pin is connected to the battery and RTCC is running with VDD = 0.

TABLE 36-7: DC CHARACTERISTICS: Δ CURRENT (BOR, WDT, HLVD, RTCC, DSBOR, DSWDT, LCD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Operating Temperature**	**VDD**	**Conditions**
Incremental Current Brown-out Reset (ΔBOR)(2)						
DC25	4	8	μA	-40°C to +85°C	VBOR	ΔBOR(2)
	4	8	μA	-40°C to +85°C	3.3V	
Incremental Current Watchdog Timer (ΔWDT)(2)						
DC71	0.15	2	μA	-40°C to +85°C	2.0V	ΔWDT (with LPRC selected)(2)
	0.24	2	μA	-40°C to +85°C	3.3V	
Incremental Current HLVD (ΔHLVD)(2)						
DC75	3.8	25	μA	-40°C to +85°C	2.0V	ΔHLVD(2)
	3.8	25	μA	-40°C to +85°C	3.3V	
Incremental Current Real-Time Clock and Calendar (ΔRTCC)(2)						
DC77	0.17	2.5	μA	-40°C to +85°C	2.0V	ΔRTCC (with SOSC)(2)
	0.17	2.5	μA	-40°C to +85°C	3.3V	
DC77A	0.55	2.5	μA	-40°C to +85°C	2.0V	ΔRTCC (with LPRC)(2)
	0.55	2.5	μA	-40°C to +85°C	3.3V	
Incremental Current Deep Sleep BOR (ΔDSBOR)(2)						
DC81	0.1	0.9	μA	-40°C to +85°C	2.0V	ΔDeep Sleep BOR(2)
	0.1	0.9	μA	-40°C to +85°C	3.3V	
Incremental Current Deep Sleep Watchdog Timer (ΔDSWDT)(2)						
DC80	0.1	0.9	μA	-40°C to +85°C	2.0V	ΔDeep Sleep WDT(2)
	0.1	0.9	μA	-40°C to +85°C	3.3V	
VBAT A/D Monitor(5)						
DC91	2	—	μA	-40°C to +85°C	3.3V	VBAT = 2V
	5	—	μA	-40°C to +85°C	3.3V	VBAT = 3.3V
Incremental Current LCD (ΔLCD)						
DC82	5	—	μA	+25°C	2.0V	(ΔLCD)/LCD internal, 1/8 MUX, 1/3 bias(2,4)
	5	—	μA	+25°C	3.3V	
DC90	100	—	μA	+25°C	2.0V	(ΔLCD)/LCD charge pump, 1/8 MUX, 1/3 bias(2,3)
	6	—	μA	+25°C	3.3V	

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Incremental current while the module is enabled and running.

3: LCD is enabled and running, no glass is connected; the resistor ladder current is not included.

4: LCD is enabled and running, no glass is connected; the low-power resistor ladder current is included.

5: The A/D channel is connected to the VBAT pin internally; this is the current during A/D VBAT operation.

FIGURE 36-14: SPIx MODULE MASTER MODE TIMING CHARACTERISTICS (CKE = 1)

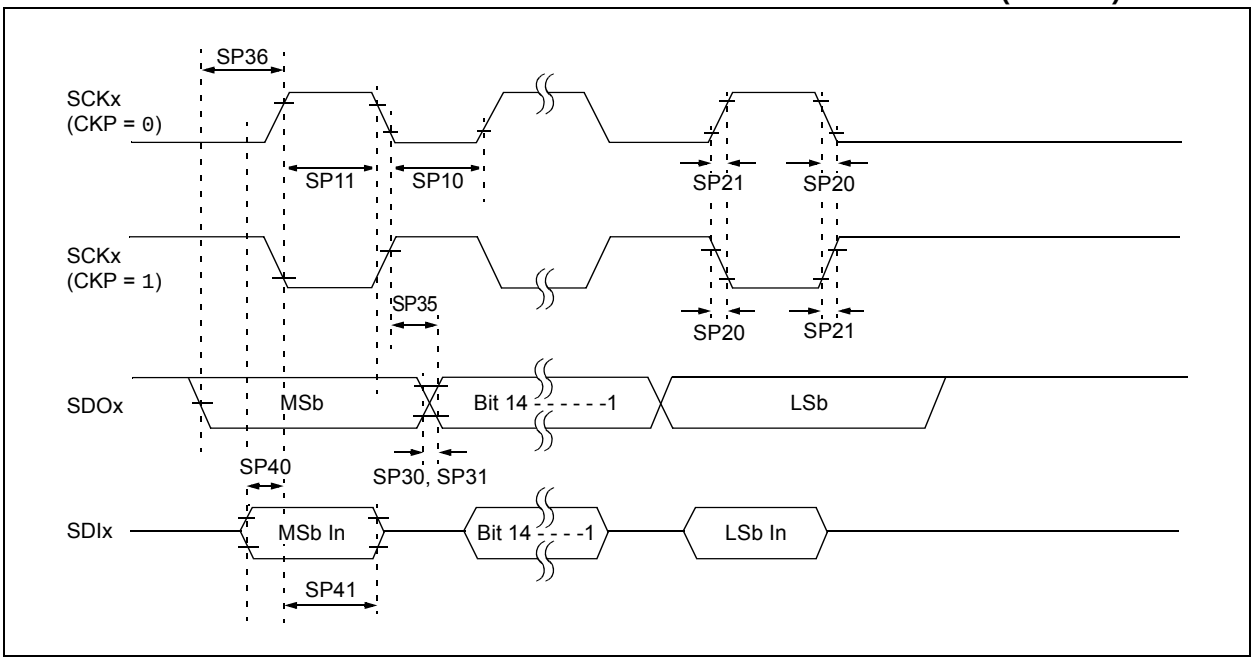

TABLE 36-35: SPIx MODULE MASTER MODE TIMING REQUIREMENTS (CKE = 1)

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
SP10	TscL	SCKx Output Low Time(2)	TCY/2	—	—	ns	
SP11	TscH	SCKx Output High Time(2)	TCY/2	—	—	ns	
SP20	TscF	SCKx Output Fall Time(3)	—	10	25	ns	
SP21	TscR	SCKx Output Rise Time(3)	—	10	25	ns	
SP30	TdoF	SDOx Data Output Fall Time(3)	—	10	25	ns	
SP31	TdoR	SDOx Data Output Rise Time(3)	—	10	25	ns	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	—	30	ns	
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	—	—	ns	

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The minimum clock period for SCKx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

3: Assumes 50 pF load on all SPIx pins.