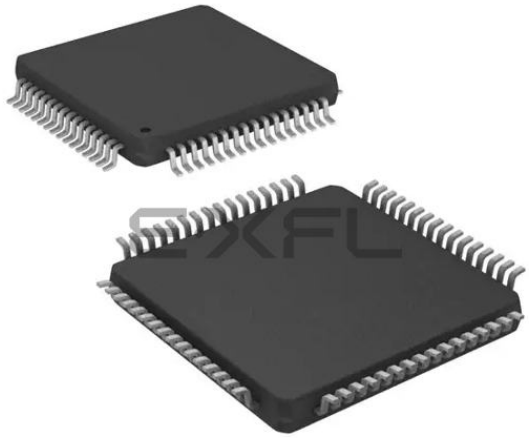

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64ga406-i-pt

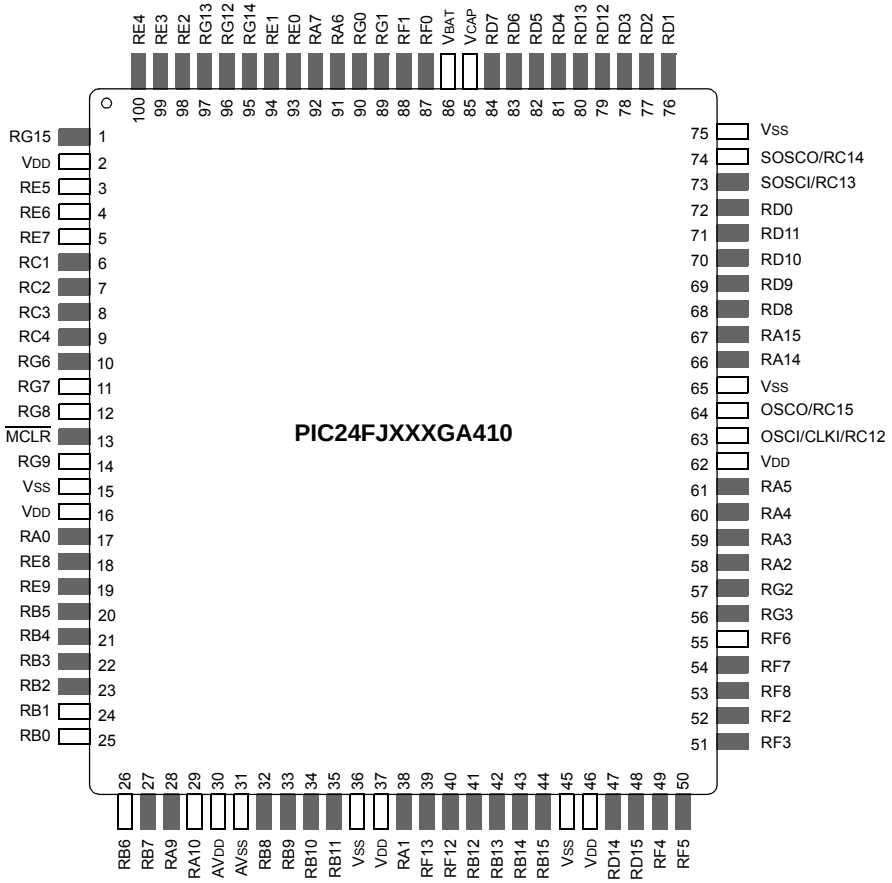
TABLE 1: COMPLETE PIN FUNCTION DESCRIPTIONS FOR PIC24FJXXXGA406 DEVICES

Pin	Function	Pin	Function
1	LCDBIAS2/IC4/CTED4/PMD5/IOCE5/RE5	33	SEG12/**RP16**/IOCF3/RF3
2	LCDBIAS1/SCL3/IC5/PMD6/IOCE6/RE6	34	SEG40/**RP30**/IOCF2/RF2
3	LCDBIAS0/SDA3/IC6/PMD7/IOCE7/RE7	35	IOCF6/RF6
4	SEG0/C1IND/**RP21**/ICM1/OCM1A/PMA5/IOCG6/RG6	36	SDA1/IOCG3/RG3
5	VLCAP1/C1INC/**RP26**/OCM1B/PMA4/IOCG7/RG7	37	SCL1/IOCG2/RG2
6	VLCAP2/C2IND/**RP19**/ICM2/OCM2/PMA3/IOCG8/RG8	38	VDD
7	$\overline{\text{MCLR}}$	39	OSCI/CLKI/IOCC12/RC12
8	SEG1/C1INC/C2INC/C3INC/**RP27**/DAC1/PMA2/PMALU/IOCG9/RG9	40	OSCO/CLKO/IOCC15/RC15
9	VSS	41	VSS
10	VDD	42	SEG13/CLC4OUT/**RP2**/RTCC/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/IOCD8/RD8
11	PGEC3/SEG2/AN5/C1INA/**RP18**/ICM3/OCM3/IOCB5/RB5	43	SEG14/**RP4**/PMACK2/IOCD9/RD9
12	PGED3/SEG3/AN4/C1INB/**RP28**/IOCB4/RB4	44	SEG15/C3IND/**RP3**/PMA15/APMCS2/IOCD10/RD10
13	SEG4/AN3/C2INA/IOCB3/RB3	45	SEG16/C3INC/**RP12**/PMA14/PMCS/APMCS1/IOCD11/RD11
14	SEG5/AN2/CTCMP/C2INB/**RP13**/CTED13/IOCB2/RB2	46	SEG17/CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/IOCD0/RD0
15	PGEC1/SEG6/VREF-/CVREF-/AN1/AN1-/**RP1**/CTED12/IOCB1/RB1	47	SOSCI/IOCC13/RC13
16	PGED1/SEG7/VREF+/CVREF+/DVREF+/AN0/**RP0**/PMA6/IOCB0/RB0	48	SOSCO/SCLKI/**RPI37**/PWRLCLK/IOCC14/RC14
17	PGEC2/LCDBIAS3/AN6/**RP6**/IOCB6/RB6	49	SEG20/**RP24**/U5TX/ICM4/IOCD1/RD1
18	PGED2/SEG63/AN7/**RP7**/U6TX/IOCB7/RB7	50	SEG21/**RP23**/PMACK1/IOCD2/RD2
19	AVDD	51	SEG22/**RP22**/ICM7/PMBE0/IOCD3/RD3
20	AVSS	52	SEG23/**RP25**/PMWR/PMENB/IOCD4/RD4
21	COM7/SEG31/AN8/**RP8**/PWRGT/IOCB8/RB8	53	SEG24/**RP20**/PMRD/$\overline{\text{PMWR}}$/IOCD5/RD5
22	COM6/SEG30/AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/PMA7/IOCB9/RB9	54	SEG25/C3INB/U5RX/OC4/IOCD6/RD6
23	TMS/COM5/SEG29/CVREF/AN10/SDO4/PMA13/IOCB10/RB10	55	SEG26/C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/IOCD7/RD7
24	TDO/AN11/REFI1/$\overline{\text{SS4}}$/FSYNC4/PMA12/IOCB11/RB11	56	VCAP
25	VSS	57	VBAT
26	VDD	58	SEG27/$\overline{\text{U5CTS}}$/OC6/IOCF0/RF0
27	TCK/SEG18/AN12/U6RX/CTED2/PMA11/IOCB12/RB12	59	COM4/SEG47/SCK4/IOCF1/RF1
28	TDI/SEG19/AN13/SDI4/CTED1/PMA10/IOCB13/RB13	60	COM3/PMD0/IOCE0/RE0
29	SEG8/AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/IOCB14/RB14	61	COM2/PMD1/IOCE1/RE1
30	SEG9/AN15/**RP29**/CTED6/PMA0/PMALL/IOCB15/RB15	62	COM1/PMD2/IOCE2/RE2
31	SEG10/**RP10**/SDA2/PMA9/IOCF4/RF4	63	COM0/CTED9/PMD3/IOCE3/RE3
32	SEG11/**RP17**/SCL2/PMA8/IOCF5/RF5	64	SEG62/LVDIN/CTED8/PMD4/IOCE4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

Pin Diagrams (Continued)

100-Pin TQFP



Legend: **Shaded pins** indicate pins tolerant to up to +5.5 VDC. See Table 3 for a complete description of pin functions.

TABLE 4: COMPLETE PIN FUNCTION DESCRIPTIONS FOR PIC24FJXXXGB410 DEVICES

Pin	Function	Pin	Function
1	SEG50/OCM1C/CTED3/IOCG15/RG15	51	SEG12/**RP16**/USBID/IOCF3/RF3
2	VDD	52	SEG40/**RP30**/IOCF2/RF2
3	LCDBIAS2/IC4/CTED4/PMD5/IOCE5/RE5	53	SEG41/**RP15**/IOCF8/RF8
4	LCDBIAS1/SCL3/IC5/PMD6/IOCE6/RE6	54	VBUS/IOCF7/RF7
5	LCDBIAS0/SDA3/IC6/PMD7/IOCE7/RE7	55	VUSB3V3
6	SEG32/**RPI38**/OCM1D/IOCC1/RC1	56	D-/IOCG3/RG3
7	SEG51/**RPI39**/IOCC2/RC2	57	D+/IOCG2/RG2
8	SEG33/**RPI40**/IOCC3/RC3	58	SEG55/SCL2/IOCA2/RA2
9	SEG52/AN16/**RPI41**/PMCS2/IOCC4/RC4	59	SEG56/SDA2/PMA20/IOCA3/RA3
10	SEG0/AN17/C1IND/**RP21**/ICM1/OCM1A/PMA5/IOCG6/RG6	60	TDI/PMA21/IOCA4/RA4
11	VLCAP1/AN18/C1INC/**RP26**/OCM1B/PMA4/IOCG7/RG7	61	TDO/SEG28/IOCA5/RA5
12	VLCAP2/AN19/C2IND/**RP19**/ICM2/OCM2/PMA3/IOCG8/RG8	62	VDD
13	$\overline{\text{MCLR}}$	63	OSCI/CLKI/IOCC12/RC12
14	SEG1/AN20/C1INC/C2INC/C3INC/**RP27**/DAC1/PMA2/PMALU/IOCG9/RG9	64	OSCO/CLKO/IOCC15/RC15
15	VSS	65	VSS
16	VDD	66	SEG42/**RPI36**/SCL1/PMA22/IOCA14/RA14
17	TMS/SEG48/CTED14/IOCA0/RA0	67	SEG43/**RPI35**/SDA1/PMBE1/IOCA15/RA15
18	SEG34/**RPI33**/PMCS1/IOCE8/RE8	68	SEG13/CLC4OUT/**RP2**/RTCC/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/IOCD8/RD8
19	SEG35/AN21/**RPI34**/PMA19/IOCE9/RE9	69	SEG14/**RP4**/PMACK2/IOCD9/RD9
20	PGEC3/SEG2/AN5/C1INA/**RP18**/ICM3/OCM3/IOCB5/RB5	70	SEG15/C3IND/**RP3**/PMA15/APMCS2/IOCD10/RD10
21	PGED3/SEG3/AN4/C1INB/**RP28**/$\overline{\text{USBOEN}}$/IOCB4/RB4	71	SEG16/C3INC/**RP12**/PMA14/PMCS/APMCS1/IOCD11/RD11
22	SEG4/AN3/C2INA/IOCB3/RB3	72	SEG17/CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/IOCD0/RD0
23	SEG5/AN2/CTCMP/C2INB/**RP13**/CTED13/IOCB2/RB2	73	SOSCI/IOCC13/RC13
24	PGEC1/SEG6/VREF-/CVREF-/AN1/AN1-/**RP1**/CTED12/IOCB1/RB1	74	SOSCO/SCLKI/**RPI37**/PWRLCLK/IOCC14/RC14
25	PGED1/SEG7/VREF+/CVREF+/DVREF+/AN0/**RP0**/IOCB0/RB0	75	VSS
26	PGEC2/LCDBIAS3/AN6/**RP6**/IOCB6/RB6	76	SEG20/**RP24**/U5TX/ICM4/IOCD1/RD1
27	PGED2/SEG63/AN7/**RP7**/U6TX/IOCB7/RB7	77	SEG21/**RP23**/PMACK1/IOCD2/RD2
28	SEG36/VREF-/CVREF-/PMA7/IOCA9/RA9	78	SEG22/**RP22**/ICM7/PMBE0/IOCD3/RD3
29	SEG37/VREF+/CVREF+/DVREF+/PMA6/IOCA10/RA10	79	SEG44/**RPI42**/PMD12/IOCD12/RD12
30	AVDD	80	SEG45/PMD13/IOCD13/RD13
31	AVSS	81	SEG23/**RP25**/PMWR/PMENB/IOCD4/RD4
32	COM7/SEG31/AN8/**RP8**/PWRGT/IOCB8/RB8	82	SEG24/**RP20**/PMRD/$\overline{\text{PMWR}}$/IOCD5/RD5
33	COM6/SEG30/AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/IOCB9/RB9	83	SEG25/C3INB/U5RX/OC4/PMD14/IOCD6/RD6
34	COM5/SEG29/CVREF/AN10/SDO4/PMA13/IOCB10/RB10	84	SEG26/C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/PMD15/IOCD7/RD7
35	AN11/REFI1/$\overline{\text{SS4}}$/FSYNC4/PMA12/IOCB11/RB11	85	VCAP
36	VSS	86	VBAT
37	VDD	87	SEG27/$\overline{\text{U5CTS}}$/OC6/PMD11/IOCF0/RF0
38	TCK/IOCA1/RA1	88	COM4/SEG47/SCK4/PMD10/IOCF1/RF1
39	SEG53/**RP31**/IOCF13/RF13	89	SEG46/PMD9/IOCG1/RG1
40	SEG54/**RPI32**/CTED7/PMA18/IOCF12/RF12	90	SEG49/PMD8/IOCG0/RG0
41	SEG18/AN12/U6RX/CTED2/PMA11/IOCB12/RB12	91	SEG57/AN23/OCM1E/IOCA6/RA6
42	SEG19/AN13/SDI4/CTED1/PMA10/IOCB13/RB13	92	SEG58/AN22/OCM1F/PMA17/IOCA7/RA7
43	SEG8/AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/IOCB14/RB14	93	COM3/PMD0/IOCE0/RE0
44	SEG9/AN15/**RP29**/CTED6/PMA0/PMALL/IOCB15/RB15	94	COM2/PMD1/IOCE1/RE1
45	VSS	95	SEG59/CTED11/PMA16/IOCG14/RG14
46	VDD	96	SEG60/IOCG12/RG12
47	SEG38/**RPI43**/IOCD14/RD14	97	SEG61/CTED10/IOCG13/RG13
48	SEG39/**RP5**/IOCD15/RD15	98	COM1/PMD2/IOCE2/RE2
49	SEG10/**RP10**/PMA9/IOCF4/RF4	99	COM0/CTED9/PMD3/IOCE3/RE3
50	SEG11/**RP17**/PMA8/IOCF5/RF5	100	SEG62/LVDIN/CTED8/PMD4/IOCE4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select functions.

1.6 Other Special Features

- **Integrated Interrupt-on-Change:** All digital I/O ports now feature Interrupt-on-Change (IOC) functionality for convenient Change Notification interrupt generation on any I/O pin. IOC can be individually enabled or disabled on each pin, and configured for both edge detection polarity and the use of pull-ups or pull-downs.
- **Peripheral Pin Select (PPS):** The Peripheral Pin Select feature allows most digital peripherals to be mapped over a fixed set of digital I/O pins. Users may independently map the input and/or output of any one of the many digital peripherals to any one of the I/O pins.
- **Communications:** The PIC24FJ256GA412/GB412 family incorporates multiple serial communication peripherals to handle a range of application requirements. All devices have six independent UARTs with built-in IrDA® encoders/decoders. There are also three independent I^2C modules that support both Master and Slave modes of operation, and three SPI modules with I^2S and variable data width support.
- **Analog Features:** All members of the PIC24FJ256GA412/GB412 family include a 12-bit A/D Converter module, a triple comparator module and the CTMU interface. The A/D module incorporates a range of features that allow the converter to assess and make decisions on incoming data, reducing CPU overhead for routine A/D conversions.
  The comparator module includes three analog comparators that are configurable for a wide range of operations. The CTMU provides a convenient method for precision time measurement and pulse generation, and can serve as an interface for capacitive sensors.
- **Enhanced Parallel Master/Parallel Slave Port:** This module allows rapid and transparent access to the microcontroller data bus, and enables the CPU to directly address external data memory. The parallel port can function in Master or Slave mode, accommodating data widths of 4, 8 or 16 bits, and address widths of up to 23 bits in Master modes.
- **Real-Time Clock and Calendar (RTCC):** This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.

1.7 Details on Individual Family Members

Devices in the PIC24FJ256GA412/GB412 family are available in 64-pin, 100-pin and 121-pin packages. General block diagrams for general purpose and USB devices are shown in Figure 1-1 and Figure 1-2, respectively.

The devices are differentiated from each other in five ways:

1. USB On-The-Go functionality (present only in PIC24FJXXXGB4XX devices).
2. Available I/O pins and ports (up to 53 pins on 6 ports for 64-pin devices, up to 85 pins on 7 ports for 100-pin devices and up to 102 pins on 9 ports for 121-pin devices).
3. Available remappable pins (29 pins on 64-pin devices and 44 pins on 100/121-pin devices).
4. Maximum available drivable LCD pixels (up to 248 for 64-pin devices and 512 on 100/121-pin devices.)
5. Analog input channels for the A/D Converter (16 channels for 64-pin devices and 24 channels for 100/121-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1, Table 1-2 and Table 1-3.

A list of pin features available on the PIC24FJ256GA412/GB412 family devices, sorted by function, is shown in Table 1-4 (for general purpose devices) or Table 1-5 (for USB devices). Note that these tables show the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams in the beginning of this data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

TABLE 1-3: DEVICE FEATURES FOR THE PIC24FJ256GA412/GB412 FAMILY: 121-PIN

Features	PIC24FJXXXGA/GB412					
	64GA	128GA	256GA	64GB	128GB	256GB
Operating Frequency	DC – 32 MHz					
Program Memory (bytes)	64K	128K	256K	64K	128K	256K
Program Memory (instructions)	22,016	44,032	88,064	22,016	44,032	88,064
Data Memory (bytes)	8K	16K		8K	16K	
Interrupt Sources (soft vectors/ NMI traps)	113 (107/6)					
I/O Ports	Ports A, B, C, D, E, F, G, H, J					
Total I/O Pins	102			101		
Remappable Pins	44 (32 I/O, 12 input only)					
Timers:						
Total Number (16-bit)	19(1,2)					
32-Bit (from paired 16-bit timers)	9					
Input Capture w/Timer Channels	6(2)					
Output Compare/PWM Channels	6(2)					
Single Output CCP (SCCP)	6					
Multiple Output CCP (MCCP)	1					
Serial Communications:						
UART	6(2)					
SPI (3-wire/4-wire)	4(2)					
I^2C	3					
USB On-The-Go	No			Yes		
Cryptographic Engine	Yes					
Parallel Communications (EPMP/PSP)	Yes					
10/12-Bit Analog-to-Digital Converter (A/D) (input channels)	24					
Digital-to-Analog Converter (DAC)	1					
Analog Comparators	3					
CTMU Interface	Yes					
LCD Controller (available pixels)	512 (64 SEG x 8 COM)					
JTAG Boundary Scan	Yes					
Resets (and delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)					
Instruction Set	77 Base Instructions, Multiple Addressing Mode Variations					
Packages	121-Pin TFBGA					

Note 1: Includes the Timer modes of SCCP and MCCP modules.

2: Some instantiations of these modules are only available through remappable pins.

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
CLKI	39	63	F9	—	—	Main Clock Input Connection
CLKO	40	64	F11	O	DIG	System Clock Output
COM0	63	99	E30	O	ANA	LCD Driver Common Outputs
COM1	62	98	E19	O	ANA	
COM2	61	94	E15	O	ANA	
COM3	60	93	A4	O	ANA	
COM4	59	88	B1	O	ANA	
COM5	23	34	D4	O	ANA	
COM6	22	33	G4	O	ANA	
COM7	21	32	H3	O	ANA	
CTCMP	14	23	J2	O	ANA	CTMU Comparator 2 Input (Pulse mode)
CTED1	28	42	L7	I	ST	CTMU External Edge Inputs
CTED2	27	41	J7	I	ST	
CTED3	—	1	B2	I	ST	
CTED4	1	3	D3	I	ST	
CTED5	29	43	K7	I	ST	
CTED6	30	44	L8	I	ST	
CTED7	—	40	K6	I	ST	
CTED8	64	100	E31	I	ST	
CTED9	63	99	E30	I	ST	
CTED10	—	97	E18	I	ST	
CTED11	—	95	E16	I	ST	
CTED12	15	24	K1	I	ST	
CTED13	14	23	J2	I	ST	
CTED14	—	17	G3	I	ST	
CTPLS	29	43	K7	O	DIG	CTMU Pulse Output
CV_{REF}	23	34	H5	O	ANA	Comparator Voltage Reference Output
CV_{REF+}	16	25,29	K2,K3	I	ANA	Comparator Voltage Reference (high) Input
CV_{REF-}	15	24,28	K1,L2	I	ANA	Comparator Voltage Reference (low) Input
D+	—	—	—	I/O	XCVR	USB D-
D-	—	—	—	I/O	XCVR	
DAC1	8	14	F3	O	ANA	DAC1 Analog Output
DV_{REF+}	16	25,29	K2,K3	I	ANA	DAC External Reference
IC4	1	3	D3	I	ST	Input Capture 4
IC5	2	4	C1	I	ST	Input Capture 5
IC6	3	5	D2	I	ST	Input Capture 6
ICM1	4	10	E3	I	ST	MCCP1 Input Capture
ICM2	6	12	F2	I	ST	SCCP2 Input Capture
ICM3	11	20	H1	I	ST	SCCP3 Input Capture
ICM4	49	76	A11	I	ST	SCCP4 Input Capture
ICM5	42	68	E9	I	ST	SCCP5 Input Capture
ICM6	46	72	D9	I	ST	SCCP6 Input Capture
ICM7	51	78	B9	I	ST	SCCP7 Input Capture

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface-mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

Typical low-cost, 10 μF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R), or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

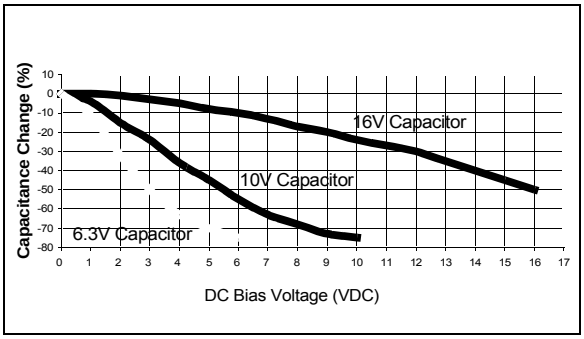
The X5R and X7R capacitors typically exhibit satisfactory temperature stability (i.e., ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 μF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

Typical DC bias voltage vs. capacitance graph for X7R type capacitors is shown in Figure 2-4.

When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 2.5V or 1.8V core voltage. Suggested capacitors are shown in Table 2-1.

FIGURE 2-4: DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming (ICSP) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

For device emulation, ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins), programmed into the device, matches the physical connections for the ICSP to the Microchip debugger/emulator tool.

The $\overline{MCLR}$ connection from the ICSP header should connect directly to the $\overline{MCLR}$ pin on the device. A capacitor to ground (C1 in Figure 2-2) is optional, but if used, may interfere with ICSP operation if the value exceeds 0.01 μF. In most cases, this capacitor is not required.

For more information on available Microchip development tools connection requirements, refer to **Section 34.0 "Development Support"**.

4.1.4 FLASH CONFIGURATION WORDS

In PIC24FJ256GA412/GB412 family devices, the top nine words of on-chip program memory are reserved for configuration information. On device Reset, the configuration information is copied into the actual Configuration registers, located in configuration space.

The address range of the Flash Configuration Words for devices in the PIC24FJ256GA412/GB412 family are shown in Table 4-2. Their location in the memory map is shown with the other memory vectors in Figure 4-1. Additional details on the device Configuration Words are provided in **Section 33.0 "Special Features"**.

4.1.4.1 Dual Partition Configuration Words

In Dual Partition Flash modes, each partition has its own set of Flash Configuration Words. The full set of Configuration registers in the Active Partition is used to determine the device's configuration; the Configuration Words in the Inactive Partition are used to determine the device's configuration when that partition becomes active. However, some of the Configuration registers in the Inactive Partition (FSEC, FBSLIM and FSIGN) may be used to determine how the Active Partition is able or allowed to access the Inactive Partition.

4.1.5 ONE-TIME-PROGRAMMABLE (OTP) MEMORY

PIC24FJ256GA412/GB412 family devices provide 384 bytes of One-Time-Programmable (OTP) memory, located at addresses, 801380h through 8013FEh. This memory can be used for persistent storage of application-specific information that will not be erased by reprogramming the device. This includes many types of information, such as (but not limited to):

- Application checksums
- Code revision information
- Product information
- Serial numbers
- System manufacturing dates
- Manufacturing lot numbers

OTP memory may be programmed in any mode, including user RTSP mode, but it cannot be erased. Data is not cleared by a Chip Erase. Once programmed, it cannot be rewritten.

Do not perform repeated write operations on the OTP.

TABLE 4-2: FLASH CONFIGURATION WORDS FOR PIC24FJ256GA412/GB412 FAMILY DEVICES

Device Family	Program Memory (Words)	Configuration Word Address Range	
		Single Partition	Dual Partition(1)
PIC24FJ64GA4XX/GB4XX	22,016	00AF80h:00AFB0h	005780h:0057FCh
PIC24FJ128GA4XX/GB4XX	44,032	015780h:0157B0h	00AB80h:00ABFCh
PIC24FJ256GA4XX/GB4XX	88,065	02AF80h:02AFB0h	015780h:0157FCh

Note 1: Addresses for the Active Partition are shown. For the Inactive Partitions, add 400000h.

4.3 Data Memory Space

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Data Memory with Extended Data Space (EDS)"** (DS39733). The information in this data sheet supersedes the information in the FRM.

The PIC24F core has a 16-bit wide data memory space, addressable as a single linear range. The Data Space (DS) is accessed using two Address Generation Units (AGUs), one each for read and write operations. The Data Space memory map is shown in Figure 4-5.

The 16-bit wide data addresses in the data memory space point to bytes within the Data Space. This gives a DS address range of 64 Kbytes or 32K words. The lower half (0000h to 7FFFh) is used for implemented (on-chip) memory addresses.

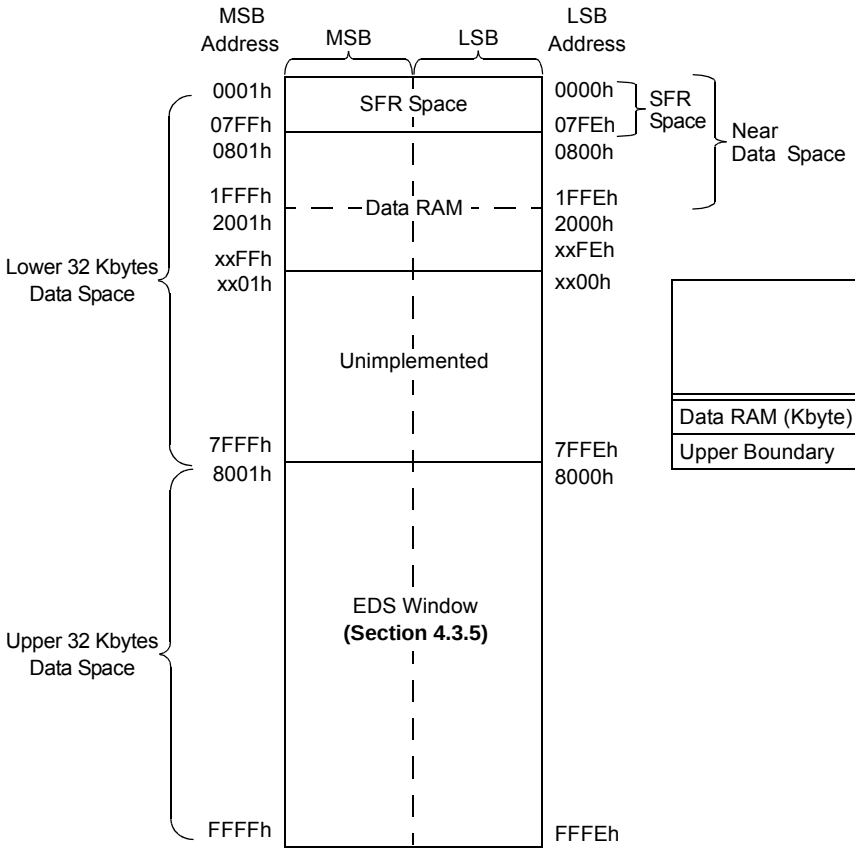
The upper half of data memory address space (8000h to FFFFh) is used as a window into the Extended Data Space (EDS). This allows the microcontroller to directly access a greater range of data beyond the standard 16-bit address range. EDS is discussed in detail in **Section 4.3.5 "Extended Data Space (EDS)"**.

Devices with 64 Kbytes of program memory implement 8 Kbytes of data RAM in the lower half of the DS, from 0800h to 27FFh. All other devices in this family implement 16 Kbytes of data RAM, from 0800h to 47FFh. The lower half of the DS is compatible with previous PIC24F microcontrollers without EDS.

4.3.1 DATA SPACE WIDTH

The data memory space is organized in byte-addressable, 16-bit wide blocks. Data is aligned in data memory and registers as 16-bit words, but all Data Space Effective Addresses (EAs) resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

FIGURE 4-5: DATA SPACE MEMORY MAP FOR PIC24FJ256GA412/GB412 FAMILY DEVICES



	Program Memory	
	64-Kbyte	128-Kbyte 256-Kbyte
Data RAM (Kbyte)	8	16
Upper Boundary	27FFh	47FFh

Note: Memory areas are not shown to scale.

TABLE 4-10: SFR BLOCK 500h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
DMA (Continued)			CRYTXTB6	564	xxxxxxxxxxxxxxxx	U1EP8(1)	5B2	0000000000000000
DMAINT5	500	0000000000000000	CRYTXTB7	566	xxxxxxxxxxxxxxxx	U1EP9(1)	5B4	0000000000000000
DMASRC5	502	0000000000000000	CRYTXTC0	558	xxxxxxxxxxxxxxxx	U1EP10(1)	5B6	0000000000000000
DMADST5	504	0000000000000000	CRYTXTC1	56A	xxxxxxxxxxxxxxxx	U1EP11(1)	5B8	0000000000000000
DMACNT5	506	0000000000000001	CRYTXTC2	56C	xxxxxxxxxxxxxxxx	U1EP12(1)	5BA	0000000000000000
Cryptographic Engine			CRYTXTC3	56E	xxxxxxxxxxxxxxxx	U1EP13(1)	5BC	0000000000000000
CRYCONL	51C	x0xxxx0xxxxxxxxx	CRYTXTC4	570	xxxxxxxxxxxxxxxx	U1EP14(1)	5BE	0000000000000000
CRYCONH	51E	0xxxxxxxxxx0xxxx	CRYTXTC5	572	xxxxxxxxxxxxxxxx	U1EP15(1)	5C0	0000000000000000
CRYSTAT	520	00000000xxxx0xxx	CRYTXTC6	574	xxxxxxxxxxxxxxxx	**LCD Controller**		
CRYOTP	524	00000000xxxxxxxx	CRYTXTC7	576	xxxxxxxxxxxxxxxx	LCDCON	5C2	0000000000000000(2)
CRYKEY0	528	xxxxxxxxxxxxxxxx	**USB**			LCDREF	5C4	0000000000000000(2)
CRYKEY1	52A	xxxxxxxxxxxxxxxx	U1OTGIR(1)	578	0000000000000000	LCDPS	5C6	0000000000000000(2)
CRYKEY2	52C	xxxxxxxxxxxxxxxx	U1OTGIE(1)	57A	0000000000000000	LCDDATA0	5C8	0000000000000000(2)
CRYKEY3	52E	xxxxxxxxxxxxxxxx	U1OTGSTAT(1)	57C	0000000000000000	LCDDATA1	5CA	0000000000000000(2)
CRYKEY4	530	xxxxxxxxxxxxxxxx	U1OTGCON(1)	57E	0000000000000000	LCDDATA2	5CC	0000000000000000(2)
CRYKEY5	532	xxxxxxxxxxxxxxxx	U1PWRC(1)	580	00000000x0000000	LCDDATA3	5CE	0000000000000000(2)
CRYKEY6	534	xxxxxxxxxxxxxxxx	U1IR(1)	582	0000000000000000	LCDDATA4	5D0	0000000000000000(2)
CRYKEY7	536	xxxxxxxxxxxxxxxx	U1IE(1)	584	0000000000000000	LCDDATA5	5D2	0000000000000000(2)
CRYKEY8	538	xxxxxxxxxxxxxxxx	U1EIR(1)	586	0000000000000000	LCDDATA6	5D4	0000000000000000(2)
CRYKEY9	53A	xxxxxxxxxxxxxxxx	U1EIE(1)	588	0000000000000000	LCDDATA7	5D6	0000000000000000(2)
CRYKEY10	53C	xxxxxxxxxxxxxxxx	U1STAT(1)	58A	0000000000000000	LCDDATA8	5D8	0000000000000000(2)
CRYKEY11	53E	xxxxxxxxxxxxxxxx	U1CON(1)	58C	00000000xx000000	LCDDATA9	5DA	0000000000000000(2)
CRYKEY12	540	xxxxxxxxxxxxxxxx	U1ADDR(1)	58E	000000000xxxxxxx	LCDDATA10	5DC	0000000000000000(2)
CRYKEY13	542	xxxxxxxxxxxxxxxx	U1BDTP1(1)	590	0000000000000000	LCDDATA11	5DE	0000000000000000(2)
CRYKEY14	544	xxxxxxxxxxxxxxxx	U1FRML(1)	592	0000000000000000	LCDDATA12	5E0	0000000000000000(2)
CRYKEY15	546	xxxxxxxxxxxxxxxx	U1FRMH(1)	594	0000000000000000	LCDDATA13	5E2	0000000000000000(2)
CRYTXTA0	548	xxxxxxxxxxxxxxxx	U1TOK(1)	596	0000000000000000	LCDDATA14	5E4	0000000000000000(2)
CRYTXTA1	54A	xxxxxxxxxxxxxxxx	U1SOF(1)	598	0000000000000000	LCDDATA15	5E6	0000000000000000(2)
CRYTXTA2	54C	xxxxxxxxxxxxxxxx	U1BDTP2(1)	59A	0000000000000000	LCDDATA16	5E8	0000000000000000(2)
CRYTXTA3	54E	xxxxxxxxxxxxxxxx	U1BDTP3(1)	59C	0000000000000000	LCDDATA17	5EA	0000000000000000(2)
CRYTXTA4	550	xxxxxxxxxxxxxxxx	U1CNFG1(1)	59E	0000000000000000	LCDDATA18	5EC	0000000000000000(2)
CRYTXTA5	552	xxxxxxxxxxxxxxxx	U1CNFG2(1)	5A0	0000000000000000	LCDDATA19	5EE	0000000000000000(2)
CRYTXTA6	554	xxxxxxxxxxxxxxxx	U1EP0(1)	5A2	0000000000000000	LCDDATA20	5F0	0000000000000000(2)
CRYTXTA7	556	xxxxxxxxxxxxxxxx	U1EP1(1)	5A4	0000000000000000	LCDDATA21	5F2	0000000000000000(2)
CRYTXTB0	558	xxxxxxxxxxxxxxxx	U1EP2(1)	5A6	0000000000000000	LCDDATA22	5F4	0000000000000000(2)
CRYTXTB1	55A	xxxxxxxxxxxxxxxx	U1EP3(1)	5A8	0000000000000000	LCDDATA23	5F6	0000000000000000(2)
CRYTXTB2	55C	xxxxxxxxxxxxxxxx	U1EP4(1)	5AA	0000000000000000	LCDDATA24	5F8	0000000000000000(2)
CRYTXTB3	55E	xxxxxxxxxxxxxxxx	U1EP5(1)	5AC	0000000000000000	LCDDATA25	5FA	0000000000000000(2)
CRYTXTB4	560	xxxxxxxxxxxxxxxx	U1EP6(1)	5AE	0000000000000000	LCDDATA26	5FC	0000000000000000(2)
CRYTXTB5	562	xxxxxxxxxxxxxxxx	U1EP7(1)	5B0	0000000000000000	LCDDATA27	5FE	0000000000000000(2)

Legend: x = unknown or indeterminate value. Reset and address values are in hexadecimal.

Note 1: Implemented in PIC24FJXXXGB4XX devices only.

2: LCD registers are only reset on a device POR.

REGISTER 8-5: INTCON4: INTERRUPT CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HSC
—	—	—	—	—	—	—	SGHT
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-1 **Unimplemented:** Read as ‘0’

bit 0 **SGHT:** Software Generated Hard Trap Status bit
1 = A software generated hard trap has occurred
0 = No software generated hard trap has occurred

REGISTER 8-33: IPC11: INTERRUPT PRIORITY CONTROL REGISTER 11

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CCT5IP2	CCT5IP1	CCT5IP0	—	DMA4IP2	DMA4IP1	DMA4IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	PMIP2	PMIP1	PMIP0	—	CCT4IP2	CCT4IP1	CCT4IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **CCT5IP<2:0>:** SCCP5 Timer Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 10-8 **DMA4IP<2:0>:** DMA Channel 4 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **PMIP<2:0>:** Parallel Master Port Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **CCT4IP<2:0>:** SCCP4 Timer Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 11-23: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP1R5	RP1R4	RP1R3	RP1R2	RP1R1	RP1R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP0R5	RP0R4	RP0R3	RP0R2	RP0R1	RP0R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP1R<5:0>:** RP1 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP1 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP0R<5:0>:** RP0 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP0 (see Table 11-12 for peripheral function numbers).

REGISTER 11-24: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP3R5	RP3R4	RP3R3	RP3R2	RP3R1	RP3R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP2R5	RP2R4	RP2R3	RP2R2	RP2R1	RP2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP3R<5:0>:** RP3 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP3 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP2R<5:0>:** RP2 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP2 (see Table 11-12 for peripheral function numbers).

REGISTER 20-11: U1SOF: USB OTG START-OF-TOKEN THRESHOLD REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **CNT<7:0>:** Start-of-Frame Size bits

Value represents 10 + (packet size of n bytes). For example:
0100 1010 = 64-byte packet
0010 1010 = 32-byte packet
0001 0010 = 8-byte packet

REGISTER 21-7: PMCSxMD: EPMP CHIP SELECT x MODE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
ACKM1	ACKM0	AMWAIT2	AMWAIT1	AMWAIT0	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DWAITB1	DWAITB0	DWAITM3	DWAITM2	DWAITM1	DWAITM0	DWAITE1	DWAITE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **ACKM<1:0>:** Chip Select x Acknowledge Mode bits
11 = Reserved
10 = PMACKx is used to determine when a read/write operation is complete
01 = PMACKx is used to determine when a read/write operation is complete with time-out
(If DWAITM<3:0> = 0000, the maximum time-out is 255 TCY or else it is DWAITM<3:0> cycles.)
00 = PMACKx is not used

bit 13-11 **AMWAIT<2:0>:** Chip Select x Alternate Master Wait States bits
111 = Wait of 10 alternate master cycles
...
001 = Wait of 4 alternate master cycles
000 = Wait of 3 alternate master cycles

bit 10-8 **Unimplemented:** Read as '0'

bit 7-6 **DWAITB<1:0>:** Chip Select x Data Setup Before Read/Write Strobe Wait States bits
11 = Wait of 3¼ TCY
10 = Wait of 2¼ TCY
01 = Wait of 1¼ TCY
00 = Wait of ¼ TCY

bit 5-2 **DWAITM<3:0>:** Chip Select x Data Read/Write Strobe Wait States bits
For Write Operations:
1111 = Wait of 15½ TCY
...
0001 = Wait of 1½ TCY
0000 = Wait of ½ TCY
For Read Operations:
1111 = Wait of 15¾ TCY
...
0001 = Wait of 1¾ TCY
0000 = Wait of ¾ TCY

bit 1-0 **DWAITE<1:0>:** Chip Select x Data Hold After Read/Write Strobe Wait States bits
For Write Operations:
11 = Wait of 3¼ TCY
10 = Wait of 2¼ TCY
01 = Wait of 1¼ TCY
00 = Wait of ¼ TCY
For Read Operations:
11 = Wait of 3 TCY
10 = Wait of 2 TCY
01 = Wait of 1 TCY
00 = Wait of 0 TCY

REGISTER 24-4: RTCCON2H: RTCC CONTROL REGISTER 2 (HIGH)(1)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
DIV<15:8>							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
DIV<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **DIV<15:0>:** Clock Divide bits
Sets the period of the clock divider counter; value should cause a nominal 1/2 second underflow.

Note 1: A write to this register is only allowed when WRLOCK = 1.

REGISTER 24-5: RTCCON3L: RTCC CONTROL REGISTER 3 (LOW)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWCSAMP7	PWCSAMP6	PWCSAMP5	PWCSAMP4	PWCSAMP3	PWCSAMP2	PWCSAMP1	PWCSAMP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWCSTAB7	PWCSTAB6	PWCSTAB5	PWCSTAB4	PWCSTAB3	PWCSTAB2	PWCSTAB1	PWCSTAB0
bit 7							bit 0

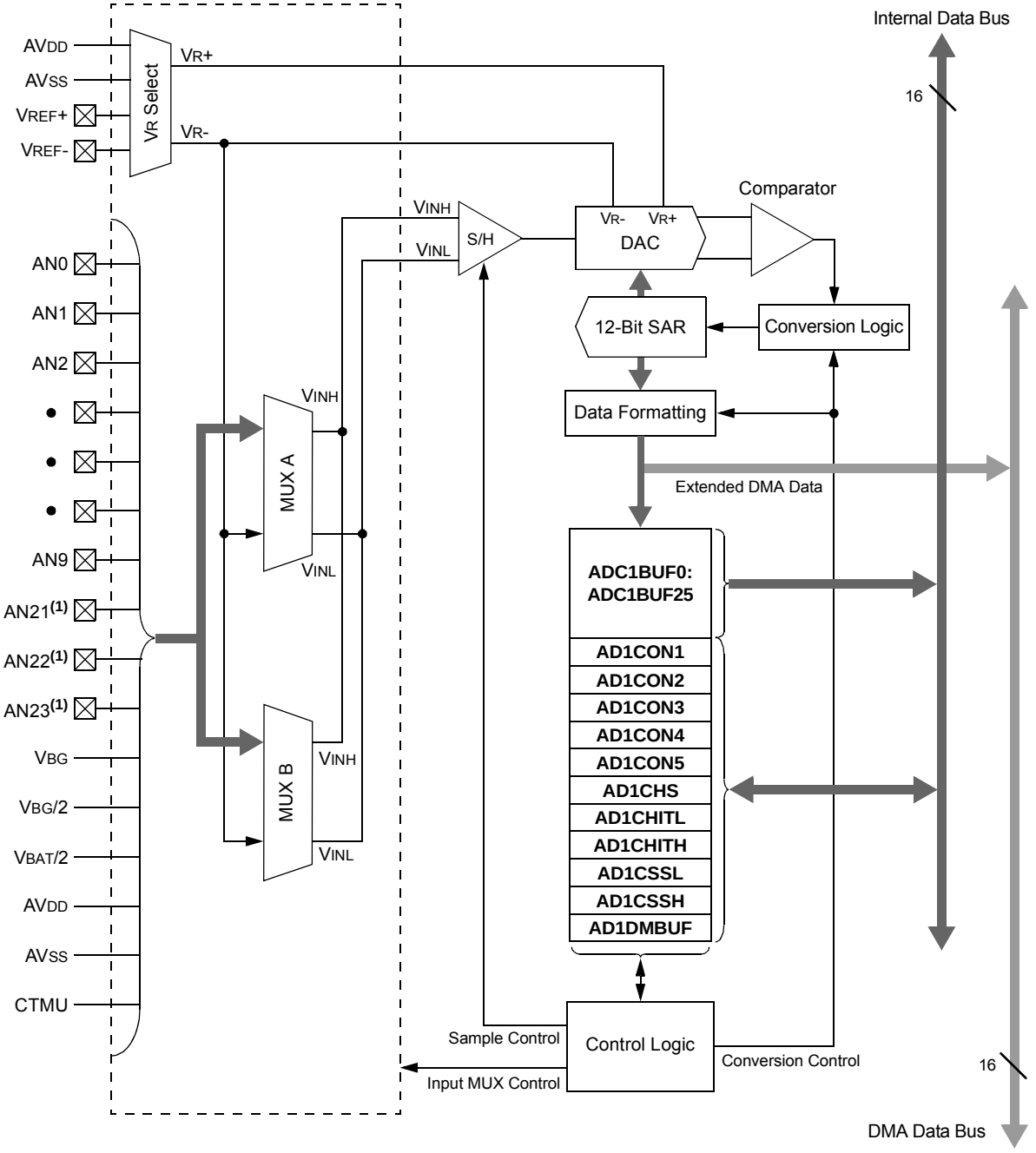
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **PWCSAMP<7:0>:** Power Control Sample Time Window bits
11111111 = Sample input is always allowed (not gated)
11111110 = Sample Time Window is 254 TPWC
• • •
00000010 = Sample Time Window is 2 TPWC
00000001 = Sample Time Window is 1 TPWC
00000000 = Sample input is always gated

bit 7-0 **PWCSTAB<7:0>:** Power Control Stability Time bits
11111111 = Stability Time Window is 255 TPWC
11111110 = Stability Time Window is 254 TPWC
• • •
00000010 = Stability Time Window is 2 TPWC
00000001 = Stability Time Window is 1 TPWC
00000000 = No Stability Time Window

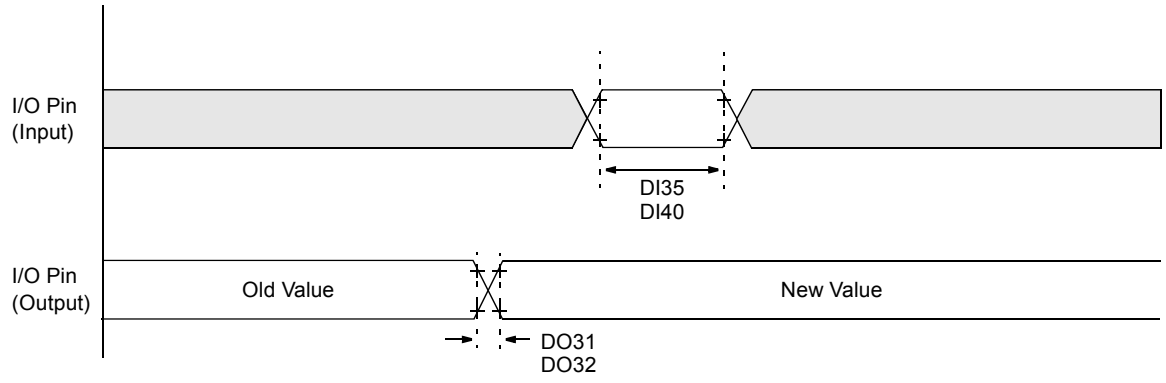
Note 1: The Sample Window always starts when the Stability Window timer expires, except when its initial value is 00h.

FIGURE 27-1: 12-BIT A/D CONVERTER BLOCK DIAGRAM (PIC24FJ256GA412/GB412 FAMILY)



Note 1: AN16 through AN23 are not implemented on 64-pin devices.

FIGURE 36-4: CLKO AND I/O TIMING CHARACTERISTICS



Note: Refer to Figure 36-2 for load conditions.

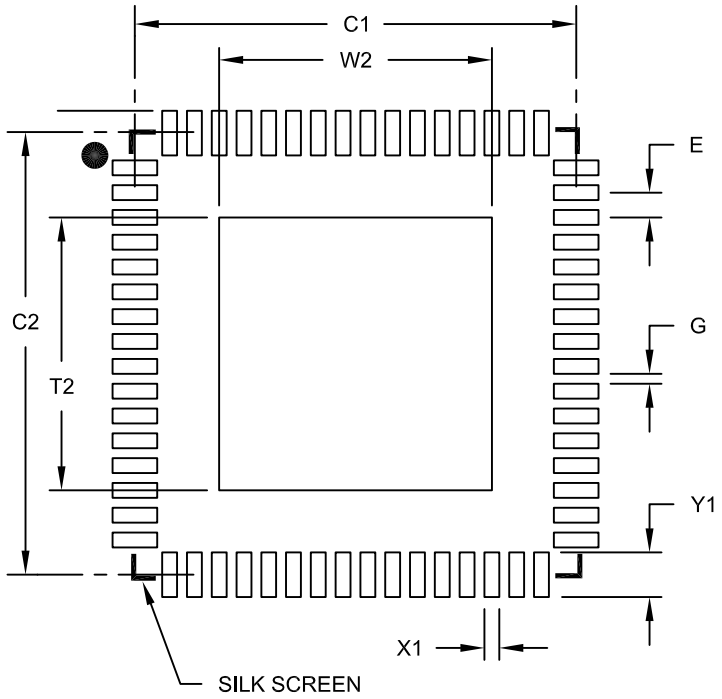
TABLE 36-24: CLKO AND I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
DO31	TIOR	Port Output Rise Time	—	5	25	ns	
DO32	TIOF	Port Output Fall Time	—	5	25	ns	
DI35	TINP	INTx Pin High or Low Time (input)	20	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	TCY	

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length and 5.40x5.40mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			5.50
Optional Center Pad Length	T2			5.50
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

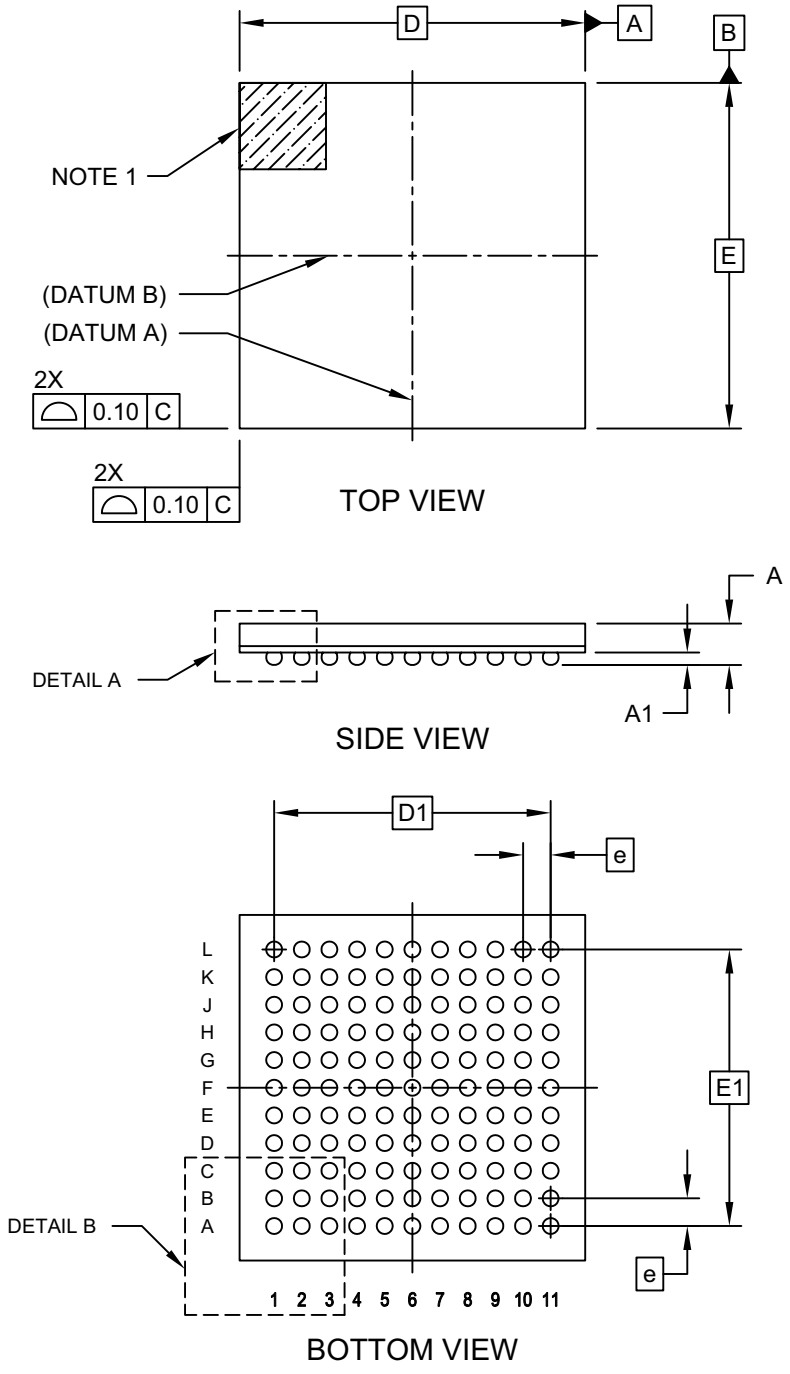
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2154A

121-Ball Plastic Thin Profile Fine Pitch Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-148 Rev F Sheet 1 of 2