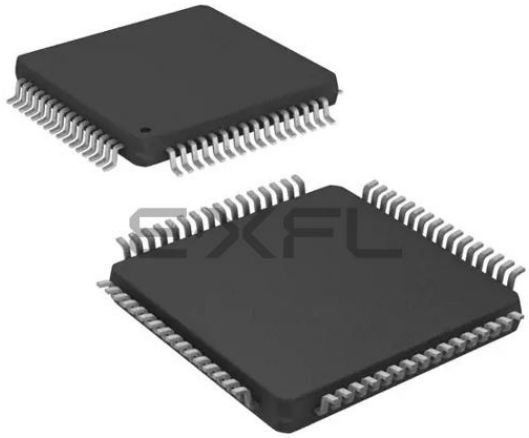


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64ga406t-i-pt

REGISTER 3-2: CORCON: CPU CORE CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/C-0	r-1	U-0	U-0
—	—	—	—	IPL3(1)	—	—	—
bit 7							bit 0

Legend:	C = Clearable bit	r = Reserved bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit(1)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

bit 2 **Reserved:** Read as '1'

bit 1-0 **Unimplemented:** Read as '0'

Note 1: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level; see Register 3-1 for bit description.

REGISTER 7-1: RCON: RESET CONTROL REGISTER

R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
TRAPR(1)	IOPUWR(1)	—	RETEN(2)	—	DPSLP(1)	CM(1)	PMSLP(3)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR(1)	SWR(1)	SWDTEN(4)	WDTO(1)	SLEEP(1)	IDLE(1)	BOR(1)	POR(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit(1)
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit(1)
1 = An illegal opcode detection, an illegal address mode or Uninitialized W register is used as an Address Pointer and caused a Reset
0 = An illegal opcode or Uninitialized W Register Reset has not occurred

bit 13 **Unimplemented:** Read as '0'

bit 12 **RETEN:** Retention Mode Enable bit(2)
1 = Retention mode is enabled while device is in Sleep modes (1.2V regulator supplies to the core)
0 = Retention mode is disabled; normal voltage levels are present

bit 11 **Unimplemented:** Read as '0'

bit 10 **DPSLP:** Deep Sleep Flag bit(1)
1 = Device has been in Deep Sleep mode
0 = Device has not been in Deep Sleep mode

bit 9 **CM:** Configuration Word Mismatch Reset Flag bit(1)
1 = A Configuration Word Mismatch Reset has occurred
0 = A Configuration Word Mismatch Reset has not occurred

bit 8 **PMSLP:** Program Memory Power During Sleep bit(3)
1 = Program memory bias voltage remains powered during Sleep
0 = Program memory bias voltage is powered down during Sleep

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin bit(1)
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset (Instruction) Flag bit(1)
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

Note 1: All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the $\overline{LPCFG}$ Configuration bit is '1' (unprogrammed), the retention regulator is disabled and the RETEN bit has no effect.

3: Re-enabling the regulator after it enters Standby mode will add a delay, TVREG, when waking up from Sleep. Applications that do not use the voltage regulator should set this bit to prevent this delay from occurring.

4: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled**,** regardless of the SWDTEN bit setting.

TABLE 8-2: IMPLEMENTED INTERRUPT VECTORS (CONTINUED)

Interrupt Source	Vector Number	IRQ #	IVT Address	Interrupt Bit Locations		
				Flag	Enable	Priority
UART3 Error	89	81	0000B6h	IFS5<1>	IEC5<1>	IPC20<6:4>
UART3 Receiver	90	82	0000B8h	IFS5<2>	IEC5<2>	IPC20<10:8>
UART3 Transmitter	91	83	0000BAh	IFS5<3>	IEC5<3>	IPC20<14:12>
UART4 Error	95	87	0000C2h	IFS5<7>	IEC5<7>	IPC21<14:12>
UART4 Receiver	96	88	0000C4h	IFS5<8>	IEC5<8>	IPC22<2:0>
UART4 Transmitter	97	89	0000C6h	IFS5<9>	IEC5<9>	IPC22<6:4>
UART5 Error	121	113	0000F6h	IFS7<1>	IEC7<1>	IPC28<6:4>
UART5 Receive	119	111	0000F2h	IFS6<15>	IEC6<15>	IPC27<14:12>
UART5 Transmit	120	112	0000F4h	IFS7<0>	IEC7<0>	IPC28<2:0>
UART6 Error	124	116	0000FCh	IFS7<4>	IEC7<4>	IPC29<2:0>
UART6 Receive	122	114	0000F8h	IFS7<2>	IEC7<2>	IPC28<10:8>
UART6 Transmit	123	113	0000FAh	IFS7<3>	IEC7<3>	IPC28<14:12>
USB	94	86	0000C0h	IFS5<6>	IEC5<6>	IPC21<10:8>

REGISTER 8-23: IPC1: INTERRUPT PRIORITY CONTROL REGISTER 1

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	T2IP2	T2IP1	T2IP0	—	OC2IP2	OC2IP1	OC2IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	IC2IP2	IC2IP1	IC2IP0	—	DMA0IP2	DMA0IP1	DMA0IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **T2IP<2:0>:** Timer2 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **OC2IP<2:0>:** Output Compare Channel 2 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **IC2IP<2:0>:** Input Capture Channel 2 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **DMA0IP<2:0>:** DMA Channel 0 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-42: IPC20: INTERRUPT PRIORITY CONTROL REGISTER 20

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U3TXIP2	U3TXIP1	U3TXIP0	—	U3RXIP2	U3RXIP1	U3RXIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	U3ERIP2	U3ERIP1	U3ERIP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **U3TXIP<2:0>:** UART3 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **U3RXIP<2:0>:** UART3 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **U3ERIP<2:0>:** UART3 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

REGISTER 8-44: IPC22: INTERRUPT PRIORITY CONTROL REGISTER 22

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPI3TXIP2	SPI3TXIP1	SPI3TXIP0	—	SPI3IP2	SPI3IP1	SPI3IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U4TXIP2	U4TXIP1	U4TXIP0	—	U4RXIP2	U4RXIP1	U4RXIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **SPI3TXIP<2:0>:** SPI3 Transmit Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **SPI3IP<2:0>:** SPI3 General Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **U4TXIP<2:0>:** UART4 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **U4RXIP<2:0>:** UART4 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 9-2: CLKDIV: CLOCK DIVIDER REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1
ROI	DOZE2	DOZE1	DOZE0	DOZEN(1)	RCDIV2	RCDIV1	RCDIV0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
CPDIV1	CPDIV0	PLLEN	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROI:** Recover on Interrupt bit
1 = Interrupts clear the DOZEN bit and reset the CPU peripheral clock ratio to 1:1
0 = Interrupts have no effect on the DOZEN bit

bit 14-12 **DOZE<2:0>:** CPU Peripheral Clock Ratio Select bits
111 = 1:128
110 = 1:64
101 = 1:32
100 = 1:16
011 = 1:8 (default)
010 = 1:4
001 = 1:2
000 = 1:1

bit 11 **DOZEN:** Doze Enable bit(1)
1 = DOZE<2:0> bits specify the CPU peripheral clock ratio
0 = CPU peripheral clock ratio is set to 1:1

bit 10-8 **RCDIV<2:0>:** FRC Postscaler Select bits
111 = 31.25 kHz (divide-by-256)
110 = 125 kHz (divide-by-64)
101 = 250 kHz (divide-by-32)
100 = 500 kHz (divide-by-16)
011 = 1 MHz (divide-by-8)
010 = 2 MHz (divide-by-4)
001 = 4 MHz (divide-by-2) (default)
000 = 8 MHz (divide-by-1)

bit 7-6 **CPDIV<1:0>:** System Clock Select bits (postscaler select from fast PLL branch)
11 = 4 MHz (divide-by-8)(2)
10 = 8 MHz (divide-by-4)(2)
01 = 16 MHz (divide-by-2)
00 = 32 MHz (divide-by-1)

bit 5 **PLLEN:** USB PLL Enable bit
1 = PLL is always active
0 = PLL is only active when a PLL Oscillator mode is selected (OSCCON<14:12> = 011 or 001)

bit 4-0 **Unimplemented:** Read as '0'

Note 1: This bit is automatically cleared when the ROI bit is set and an interrupt occurs.
2: This setting is not allowed while the USB module is enabled.

For 32-bit cascaded operation, these steps are also necessary:

1. Set the OC32 bits for both registers (OCyCON2<8>) and (OCxCON2<8>). Enable the even numbered module first to ensure the modules will start functioning in unison.
2. Clear the OCTRIG bit of the even module (OCyCON2<7>), so the module will run in Synchronous mode.
3. Configure the desired output and Fault settings for OCy.
4. Force the output pin for OCx to the output state by clearing the OCTRIS bit.
5. If Trigger mode operation is required, configure the trigger options in OCx by using the OCTRIG (OCxCON2<7>), TRIGMODE (OCxCON1<3>) and SYNCSELx (OCxCON2<4:0>) bits.
6. Configure the desired Compare or PWM mode of operation (OCM<2:0>) for OCy first, then for OCx.

Depending on the output mode selected, the module holds the OCx pin in its default state and forces a transition to the opposite state when OCxR matches the timer. In Double Compare modes, OCx is forced back to its default state when a match with OCxRS occurs. The OCxIF interrupt flag is set after an OCxR match in Single Compare modes and after each OCxRS match in Double Compare modes.

Single-shot pulse events only occur once, but may be repeated by simply rewriting the value of the OCxCON1 register. Continuous pulse events continue indefinitely until terminated.

16.3 Pulse-Width Modulation (PWM) Mode

In PWM mode, the output compare module can be configured for edge-aligned or center-aligned pulse waveform generation. All PWM operations are double-buffered (buffer registers are internal to the module and are not mapped into SFR space).

To configure the output compare module for PWM operation:

1. Configure the OCx output for one of the available Peripheral Pin Select pins.
2. Calculate the desired duty cycles and load them into the OCxR register.
3. Calculate the desired period and load it into the OCxRS register.
4. Select the current OCx as the synchronization source by writing '0x1F' to the SYNCSEL<4:0> bits (OCxCON2<4:0>) and '0' to the OCTRIG bit (OCxCON2<7>).
5. Select a clock source by writing to the OCTSEL<2:0> bits (OCxCON1<12:10>).
6. Enable interrupts, if required, for the timer and output compare modules. The output compare interrupt is required for PWM Fault pin utilization.
7. Select the desired PWM mode in the OCM<2:0> bits (OCxCON1<2:0>).
8. Appropriate Fault inputs may be enabled by using the ENFLT<2:0> bits as described in Register 16-1.
9. If a timer is selected as a clock source, set the selected timer prescale value. The selected timer's prescaler output is used as the clock input for the OCx timer and not the selected timer output.

Note: This peripheral contains input and output functions that may need to be configured by the Peripheral Pin Select. For more information, see **Section 11.5 "Peripheral Pin Select (PPS)"**.

Note: Make sure the I/O ports are in Digital mode and the TRISx bits are configured for Output mode for the peripheral pin selected.

REGISTER 17-3: SPIxCON2L: SPIx CONTROL REGISTER 2 LOW

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	WLENGTH<4:0>(1,2)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **WLENGTH<4:0>:** Variable Word Length bits(1,2)

11111 = 32-bit data
11110 = 31-bit data
11101 = 30-bit data
11100 = 29-bit data
11011 = 28-bit data
11010 = 27-bit data
11001 = 26-bit data
11000 = 25-bit data
10111 = 24-bit data
10110 = 23-bit data
10101 = 22-bit data
10100 = 21-bit data
10011 = 20-bit data
10010 = 19-bit data
10001 = 18-bit data
10000 = 17-bit data
01111 = 16-bit data
01110 = 15-bit data
01101 = 14-bit data
01100 = 13-bit data
01011 = 12-bit data
01010 = 11-bit data
01001 = 10-bit data
01000 = 9-bit data
00111 = 8-bit data
00110 = 7-bit data
00101 = 6-bit data
00100 = 5-bit data
00011 = 4-bit data
00010 = 3-bit data
00001 = 2-bit data
00000 = See MODE<32,16> bits in SPIxCON1L<11:10>

Note 1: These bits are effective when AUDEN = 0 only.

2: Varying the length by changing these bits does not affect the depth of the TX/RX FIFO.

REGISTER 18-1: I2CxCONL: I2Cx CONTROL REGISTER LOW (CONTINUED)

bit 7 **GCEN:** General Call Enable bit (I^2C Slave mode only)
1 = Enables interrupt when a general call address is received in I2CxRSR; module is enabled for reception
0 = General call address is disabled.

bit 6 **STREN:** SCLx Clock Stretch Enable bit
In I^2C Slave mode only; used in conjunction with the SCKREL bit.
1 = Enables clock stretching
0 = Disables clock stretching

bit 5 **ACKDT:** Acknowledge Data bit
In I^2C Master mode during Master Receive mode. The value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
In I^2C Slave mode when AHEN = 1 or DHEN = 1. The value that the slave will transmit when it initiates an Acknowledge sequence at the end of an address or data reception.
1 = NACK is sent
0 = ACK is sent

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
In I^2C Master mode only; applicable during Master Receive mode.
1 = Initiates Acknowledge sequence on SDAx and SCLx pins, and transmits ACKDT data bit
0 = Acknowledge sequence is Idle

bit 3 **RCEN:** Receive Enable bit (I^2C Master mode only)
1 = Enables Receive mode for I^2C; automatically cleared by hardware at end of 8-bit receive data byte
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (I^2C Master mode only)
1 = Initiates Stop condition on SDAx and SCLx pins
0 = Stop condition is Idle

bit 1 **RSEN:** Restart Condition Enable bit (I^2C Master mode only)
1 = Initiates Restart condition on SDAx and SCLx pins
0 = Restart condition is Idle

bit 0 **SEN:** Start Condition Enable bit (I^2C Master mode only)
1 = Initiates Start condition on SDAx and SCLx pins
0 = Start condition is Idle

Note 1: Automatically cleared to '0' at the beginning of slave transmission; automatically cleared to '0' at the end of slave reception.

2: Automatically cleared to '0' at the beginning of slave transmission.

21.0 ENHANCED PARALLEL MASTER PORT (EPMP)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Enhanced Parallel Master Port (EPMP)"** (DS39730). The information in this data sheet supersedes the information in the FRM.

The Enhanced Parallel Master Port (EPMP) module provides a parallel, 4-bit (Master mode only), 8-bit (Master and Slave modes) or 16-bit (Master mode only) data bus interface to communicate with off-chip modules, such as memories, FIFOs, LCD controllers and other microcontrollers. This module can serve as either the master or the slave on the communication bus.

For EPMP Master modes, all external addresses are mapped into the internal Extended Data Space (EDS). This is done by allocating a region of the EDS for each Chip Select (CS), and then assigning each Chip Select to a particular external resource, such as a memory or external controller. This region should not be assigned to another device resource, such as RAM or SFRs. To perform a write or read on an external resource, the CPU simply performs a write or read within the address range assigned for the EPMP.

Key features of the EPMP module are:

- Extended Data Space (EDS) Interface allows Direct Access from the CPU
- Up to 23 Programmable Address Lines
- Up to 2 Chip Select Lines
- Up to 2 Acknowledgment Lines (one per Chip Select)
- 4-Bit, 8-Bit or 16-Bit Wide Data Bus
- Programmable Strobe Options (per Chip Select):
  - Individual Read and Write Strobes or;
  - Read/$\overline{\text{Write}}$ Strobe with Enable Strobe
- Programmable Address/Data Multiplexing
- Programmable Address Wait States
- Programmable Data Wait States (per Chip Select)
- Programmable Polarity on Control Signals (per Chip Select)
- Legacy Parallel Slave Port Support
- Enhanced Parallel Slave Support:
  - Address Support
  - 4-Byte Deep Auto-Incrementing Buffer

21.1 Specific Package Variations

While all PIC24FJ256GA412/GB412 family devices implement the EPMP, I/O pin constraints place some limits on 16-Bit Master mode operations in some package types. This is reflected in the number of dedicated Chip Select pins implemented and the number of dedicated address lines that are available. The differences are summarized in Table 21-1. All available EPMP pin functions are summarized in Table 21-2.

For 64-pin devices, the dedicated Chip Select pins (PMCS1 and PMS2) are not implemented. In addition, only 16 address lines (PMA<15:0>) are available. If required, PMA14 and PMA15 can be remapped to function as APMCS1 and APMCS2 (Alternate Chip Select 1/2), respectively.

The memory space addressable by the device depends on the number of address lines available, as well as the number of Chip Select signals required for the application. Devices with lower pin counts are more affected by Chip Select requirements, as these take away address lines. Table 21-1 shows the maximum addressable range for each pin count.

TABLE 21-1: EPMP FEATURE DIFFERENCES BY DEVICE PIN COUNT

Device	Dedicated Chip Select		Address Lines	Address Range (bytes)		
	CS1	CS2		No CS	1 CS	2 CS
PIC24FJXXXGX406 (64-pin)(1)	—	—	16	64K	32K	16K
PIC24FJXXXGX410 (100-pin)	X	X	23	16M		
PIC24FJXXXGX412 (121-pin)	X	X	23	16M		

Note 1: The 64-pin devices can use the Alternate Chip Select pins, APMCS1 and APMCS2.

REGISTER 22-4: LCDSEx: LCD SEGMENT x ENABLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SE(n+15)(1,2)	SE(n+14)	SE(n+13)	SE(n+12)	SE(n+11)	SE(n+10)	SE(n+9)	SE(n+8)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SE(n+7)	SE(n+6)	SE(n+5)	SE(n+4)	SE(n+3)	SE(n+2)	SE(n+1)	SE(n)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **SE(n+15):SE(n)**: Segment Enable bits
For LCDSE0: n = 0
For LCDSE1: n = 16
For LCDSE2: n = 32
For LCDSE3: n = 48(1,2)
1 = Segment function of the pin is enabled, digital I/O is disabled
0 = Segment function of the pin is disabled, digital I/O is enabled

Note 1: SE63 (LCDSE3<15>) is not implemented.
2: For the SEG49 to work correctly, the JTAG needs to be disabled.

REGISTER 22-5: LCDDATAx: LCD DATA x REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
S(n+15)Cy	S(n+14)Cy	S(n+13)Cy	S(n+12)Cy	S(n+11)Cy	S(n+10)Cy	S(n+9)Cy	S(n+8)Cy
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
S(n+7)Cy	S(n+6)Cy	S(n+5)Cy	S(n+4)Cy	S(n+3)Cy	S(n+2)Cy	S(n+1)Cy	S(n)Cy
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **S(n+15)Cy:S(n)Cy**: Pixel On bits
For Registers, LCDDATA0 through LCDDATA3: n = (16x), y = 0
For Registers, LCDDATA4 through LCDDATA7: n = (16(x – 4)), y = 1
For Registers, LCDDATA8 through LCDDATA11: n = (16(x – 8)), y = 2
For Registers, LCDDATA12 through LCDDATA15: n = (16(x – 12)), y = 3
For Registers, LCDDATA16 through LCDDATA19: n = (16(x – 16)), y = 4
For Registers, LCDDATA20 through LCDDATA23: n = (16(x – 20)), y = 5
For Registers, LCDDATA24 through LCDDATA27: n = (16(x – 24)), y = 6
For Registers, LCDDATA28 through LCDDATA31: n = (16(x – 28)), y = 7
1 = Pixel is on
0 = Pixel is off

REGISTER 25-3: CRYSTAT: CRYPTOGRAPHIC STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-x, HSC(1)	R-0, HSC(1)	R/C-0, HS(2)	R/C-0, HS(2)	U-0	R-0, HSC(1)	R-x, HSC(1)	R-x, HSC(1)
CRYBSY(4)	TXTABSY	CRYABRT(5)	ROLLOVR	—	MODFAIL(3)	KEYFAIL(3,4)	PGMFAIL(3,4)
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	HS = Hardware Settable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CRYBSY:** Cryptographic Engine Busy Status bit(1,4)
1 = A cryptographic operation is in progress
0 = No cryptographic operation is in progress

bit 6 **TXTABSY:** CRYTXTA Busy Status bit(1)
1 = The CRYTXTA register is busy and may not be written to
0 = The CRYTXTA is free and may be written to

bit 5 **CRYABRT:** Cryptographic Operation Aborted Status bit(2,5)
1 = Last operation was aborted by clearing the CRYGO bit in software
0 = Last operation completed normally (CRYGO cleared in hardware)

bit 4 **ROLLOVR:** Counter Rollover Status bit(2)
1 = The CRYTXTB counter rolled over on the last CTR mode operation; once set, this bit must be cleared by software before the CRYGO bit can be set again
0 = No rollover event has occurred

bit 3 **Unimplemented:** Read as '0'

bit 2 **MODFAIL:** Mode Configuration Fail Flag bit(1,3)
1 = Currently selected operating and Cipher mode configuration is invalid; the CRYWR bit cannot be set until a valid mode is selected (automatically cleared by hardware with any valid configuration)
0 = Currently selected operating and Cipher mode configurations are valid

bit 1 **KEYFAIL:** Key Configuration Fail Status bit(1,3,4)
See Table 25-1 and Table 25-2 for invalid key configurations.
1 = Currently selected key and mode configurations are invalid; the CRYWR bit cannot be set until a valid mode is selected (automatically cleared by hardware with any valid configuration)
0 = Currently selected configurations are valid

bit 0 **PGMFAIL:** Key Storage/Configuration Program Fail Flag bit(1,3,4)
1 = The page indicated by KEYPG<3:0> is reserved or locked; the CRYWR bit cannot be set and no programming operation can be started
0 = The page indicated by KEYPG<3:0> is available for programming

Note 1: These bits are reset on system Resets or whenever the CRYMD bit (PMD8<0>) is set.
2: These bits are reset on system Resets when the CRYMD bit is set or when CRYGO is cleared.
3: These bits are functional even when the module is disabled (CRYON = 0); this allows mode configurations to be validated for compatibility before enabling the module.
4: These bits are automatically set during all OTP read operations, including the initial read at POR. Once the read is completed, the bit assumes the proper state that reflects the current configuration.
5: If this bit is set, a cryptographic operation cannot be performed.

REGISTER 25-5: CFGPAGE: SECURE ARRAY CONFIGURATION BITS (OTP PAGE 0) REGISTER (CONTINUED)

bit 21-20 **KEY1TYPE<1:0>:** Key Type for OTP Pages 1 and 2 bits
11 = Keys in these pages are for 192-bit/256-bit AES operations only
10 = Keys in these pages are for 128-bit AES operations only
01 = Keys in these pages are for 3DES operations only
00 = Keys in these pages are for DES/2DES operations only

bit 19 **SKEYEN:** Session Key Enable bit
1 = Stored Key #1 may be used only as a Key Encryption Key
0 = Stored Key #1 may be used for any operation

bit 18-11 **LKYSRC<7:0>:** Locked Key Source Configuration bits
If SRCLCK = 1:
1xxxxxxx = Key source is as if KEYSRC<3:0> = 1111
01xxxxxx = Key source is as if KEYSRC<3:0> = 0111
001xxxxx = Key source is as if KEYSRC<3:0> = 0110
0001xxxx = Key source is as if KEYSRC<3:0> = 0101
00001xxx = Key source is as if KEYSRC<3:0> = 0100
000001xx = Key source is as if KEYSRC<3:0> = 0011
0000001x = Key source is as if KEYSRC<3:0> = 0010
00000001 = Key source is as if KEYSRC<3:0> = 0001
00000000 = Key source is as if KEYSRC<3:0> = 0000
If SRCLCK = 0:
These bits are ignored.

bit 10 **SRCLCK:** Key Source Lock bit
1 = The key source is determined by the LKYSRC<7:0> bits (software key selection is disabled)
0 = The key source is determined by the KEYSRC<3:0> (CRYCONH<3:0>) bits (locked key selection is disabled)

bit 9-1 **WRLOCK<8:0>:** Write Lock Page Enable bits
For OTP Pages 0 (CFGPAGE) through 8:
1 = OTP Page is permanently locked and may not be programmed
0 = OTP Page is unlocked and may be programmed

bit 0 **SWKYDIS:** Software Key Disable bit
1 = Software key (CRYKEY register) is disabled; when KEYSRC<3:0> = 0000, the KEYFAIL status bit will be set and no encryption/decryption/session key operations can be started until KEYSRC<3:0> bits are changed to a value other than '0000'
0 = Software key (CRYKEY register) can be used as a key source when KEYSRC<3:0> = 0000

Note 1: This bit's state is mirrored by the PGMTST bit (CRYOTP<7>).

REGISTER 27-5: AD1CON5: A/D CONTROL REGISTER 5

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
ASEN	LPEN	CTMREQ	BGREQ	—	—	ASINT1	ASINT0
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	WM1	WM0	CM1	CM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ASEN:** Auto-Scan Enable bit
1 = Auto-scan is enabled
0 = Auto-scan is disabled

bit 14 **LPEN:** Low-Power Enable bit
1 = Low power is enabled after scan
0 = Full power is enabled after scan

bit 13 **CTMREQ:** CTMU Request bit
1 = CTMU is enabled when the A/D is enabled and active
0 = CTMU is not enabled by the A/D

bit 12 **BGREQ:** Band Gap Request bit
1 = Band gap is enabled when the A/D is enabled and active
0 = Band gap is not enabled by the A/D

bit 11-10 **Unimplemented:** Read as '0'

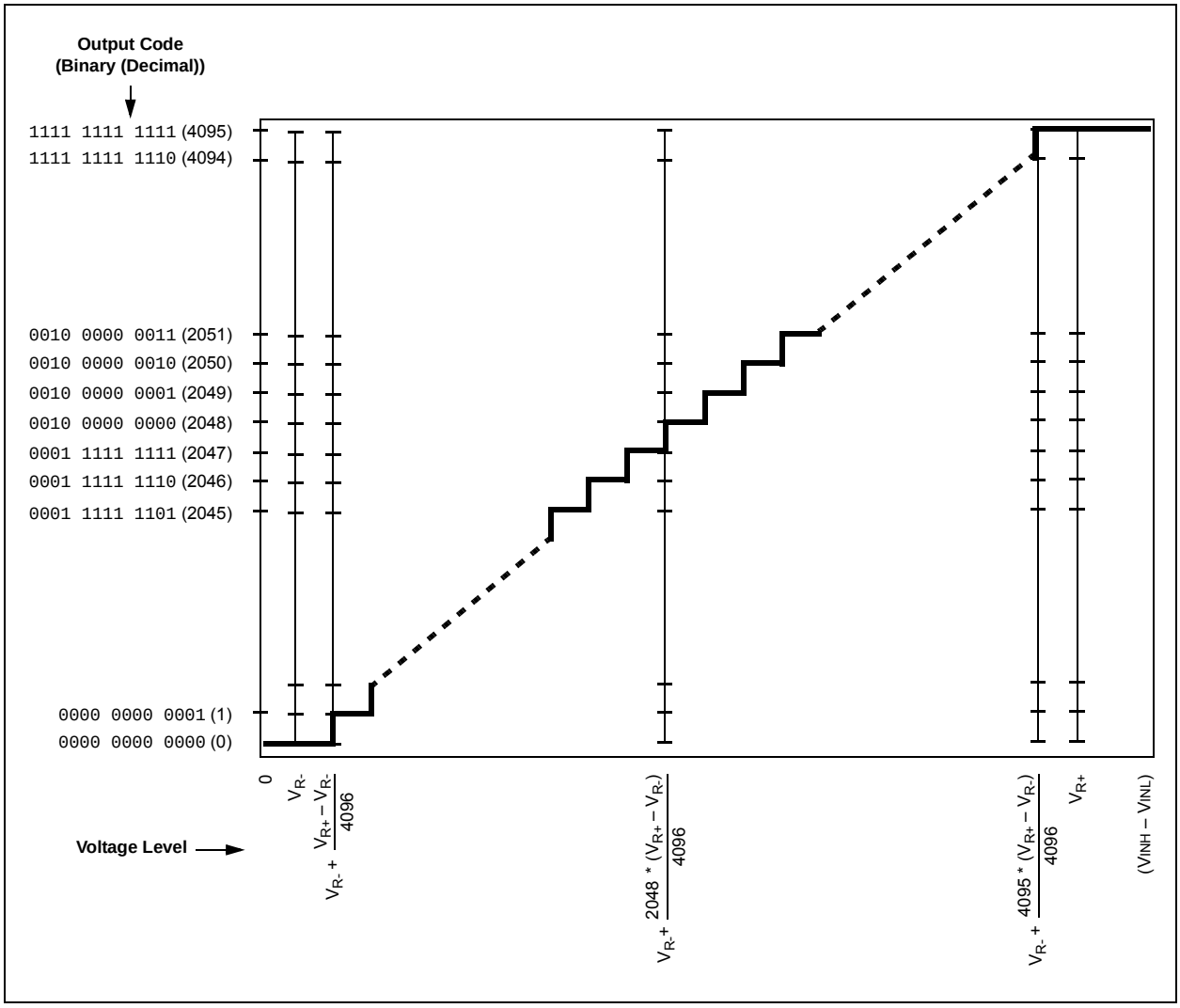
bit 9-8 **ASINT<1:0>:** Auto-Scan (Threshold Detect) Interrupt Mode bits
11 = Interrupt after Threshold Detect sequence has completed and valid compare has occurred
10 = Interrupt after valid compare has occurred
01 = Interrupt after Threshold Detect sequence has completed
00 = No interrupt

bit 7-4 **Unimplemented:** Read as '0'

bit 3-2 **WM<1:0>:** Write Mode bits
11 = Reserved
10 = Auto-compare only (conversion results are not saved, but interrupts are generated when a valid match occurs, as defined by the CMx and ASINTx bits)
01 = Convert and save (conversion results are saved to locations as determined by the register bits when a match occurs, as defined by the CMx bits)
00 = Legacy operation (conversion data is saved to a location determined by the buffer register bits)

bit 1-0 **CM<1:0>:** Compare Mode bits
11 = Outside Window mode (valid match occurs if the conversion result is outside of the window defined by the corresponding buffer pair)
10 = Inside Window mode (valid match occurs if the conversion result is inside the window defined by the corresponding buffer pair)
01 = Greater Than mode (valid match occurs if the result is greater than the value in the corresponding buffer register)
00 = Less Than mode (valid match occurs if the result is less than the value in the corresponding buffer register)

FIGURE 27-4: 12-BIT A/D TRANSFER FUNCTION



28.0 10-BIT DIGITAL-TO-ANALOG CONVERTER (DAC)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"10-Bit Digital-to-Analog Converter (DAC)"** (DS39615). The information in this data sheet supersedes the information in the FRM.

PIC24FJ256GA412/GB412 family devices include 10-bit Digital-to-Analog Converters (DACs) for generating analog outputs from digital data. A simplified block diagram for a the DAC is shown in Figure 28-1.

The DAC generates an analog output voltage based on the digital input code, according to the formula:

$$V_{DAC} = \frac{V_{DACREF} \times DACxDAT}{1024}$$

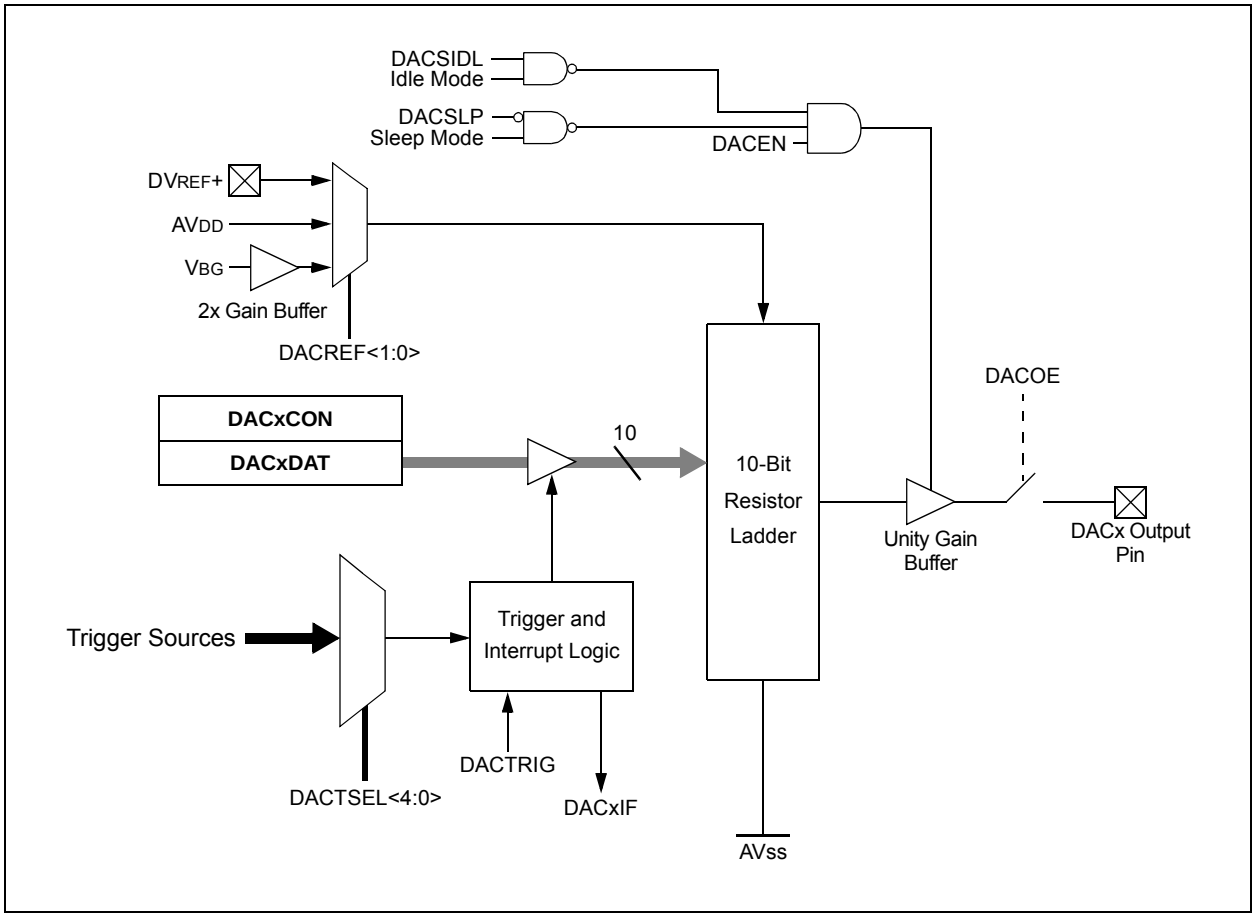
where V_{DAC} is the analog output voltage and V_{DACREF} is the reference voltage selected by DACREF<1:0>.

The DAC includes these features:

- Precision 10-Bit Resistor Ladder for High Accuracy
- Fast Settling Time, Supporting 1 Msps Effective Sampling Rates
- Buffered Output Voltage
- Three User-Selectable Voltage Reference Options
- Multiple Conversion Trigger Options, Plus a Manual Convert-on-Write Option
- Left and Right Justified Input Data Options
- User-Selectable Sleep and Idle mode Operation

When using the DAC, it is required to set the ANSx and TRISx bits for the DACx output pin to configure it as an analog output. See **Section 11.2 "Configuring Analog Port Pins (ANSx)"** for more information.

FIGURE 28-1: DAC SIMPLIFIED BLOCK DIAGRAM



REGISTER 33-5: FOSC: OSCILLATOR CONFIGURATION WORD

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
FCKSM1	FCKSM0	IOL1WAY	PLLSS(1)	SOSCSEL	OSCIOFCN	POSCMOD1	POSCMOD0
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-8 **Unimplemented:** Read as ‘1’

bit 7-6 **FCKSM<1:0>:** Clock Switching and Fail-Safe Clock Monitor Configuration bits
1x = Clock switching and Fail-Safe Clock Monitor are disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 5 **IOL1WAY:** IOLOCK One-Way Set Enable bit
1 = The IOLOCK bit (OSCCON<6>) can be set once, provided the unlock sequence has been completed; once set, the Peripheral Pin Select registers cannot be written to a second time
0 = The IOLOCK bit can be set and cleared as needed, provided the unlock sequence has been completed

bit 4 **PLLSS:** PLL Block Secondary Selection Configuration bit(1)
1 = PLL is driven by the Primary Oscillator
0 = PLL is driven by the FRC Oscillator

bit 3 **SOSCSEL:** SOSC Selection bit
1 = SOSC circuit is selected
0 = Digital (SCLKI) mode(2)

bit 2 **OSCIOFCN:** OSCO Pin Configuration bit
If POSCMOD<1:0> = 11 or 00:
1 = OSCO/CLKO/RC15 functions as CLKO (FOSC/2)
0 = OSCO/CLKO/RC15 functions as port I/O (RC15)
If POSCMOD<1:0> = 10 or 01:
OSCIOFCN has no effect on OSCO/CLKO/RC15.

bit 1-0 **POSCMOD<1:0>:** Primary Oscillator Configuration bits
11 = Primary Oscillator mode is disabled
10 = HS Oscillator mode is selected (HS mode is used if crystal ≥ 10 MHz)
01 = XT Oscillator mode is selected (XT mode is used if crystal < 10 MHz)
00 = EC Oscillator mode is selected

Note 1: Used only when the PLL block is not being used as the system clock source.
2: Ensure that the SCLKI pin is made a digital input while using this configuration (see Table 11-1).

36.2 AC Characteristics and Timing Parameters

The information contained in this section defines the PIC24FJ256GA412/GB412 family AC characteristics and timing parameters.

TABLE 36-18: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial Operating voltage VDD range as described in **Section 36.1 "DC Characteristics"**.

FIGURE 36-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

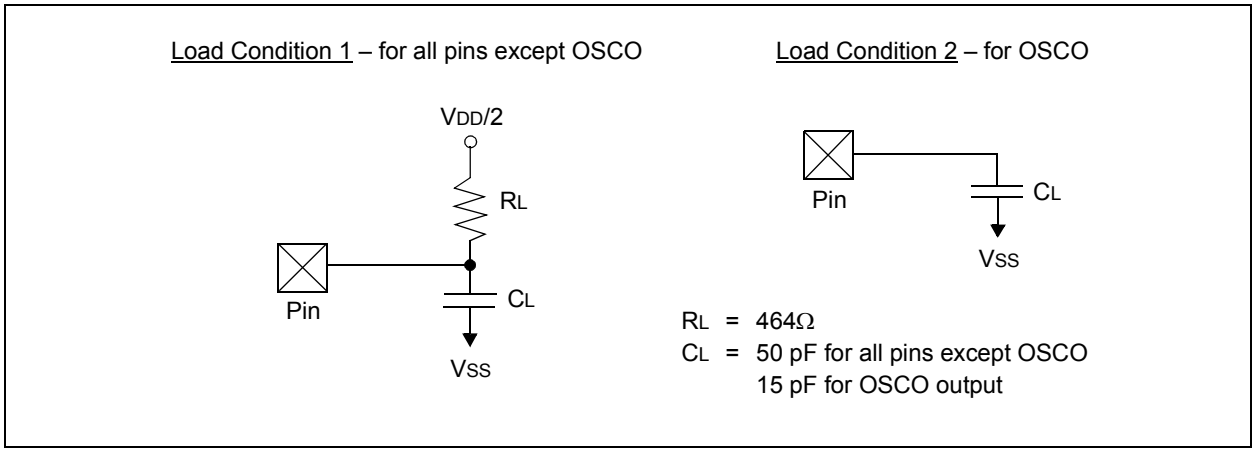


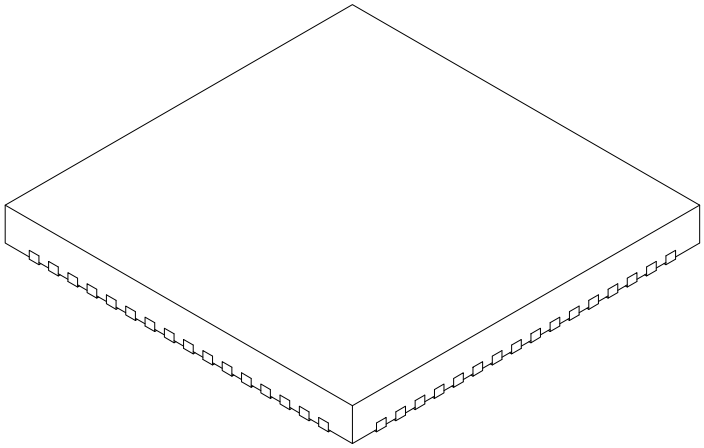
TABLE 36-19: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
DO50	COSCO	OSCO/CLKO Pin	—	—	15	pF	In XT and HS modes when external clock is used to drive OSCI
DO56	CIO	All I/O Pins and OSCO	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^2C mode

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	5.30	5.40	5.50
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	5.30	5.40	5.50
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2