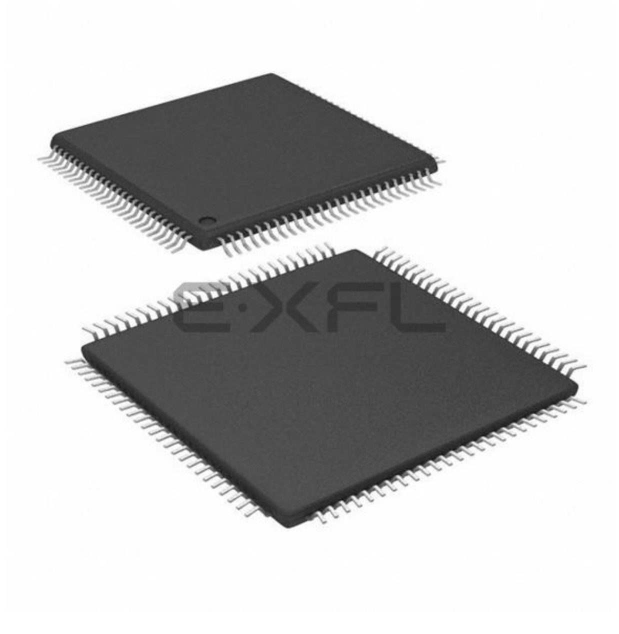


What is "Embedded - Microcontrollers"?

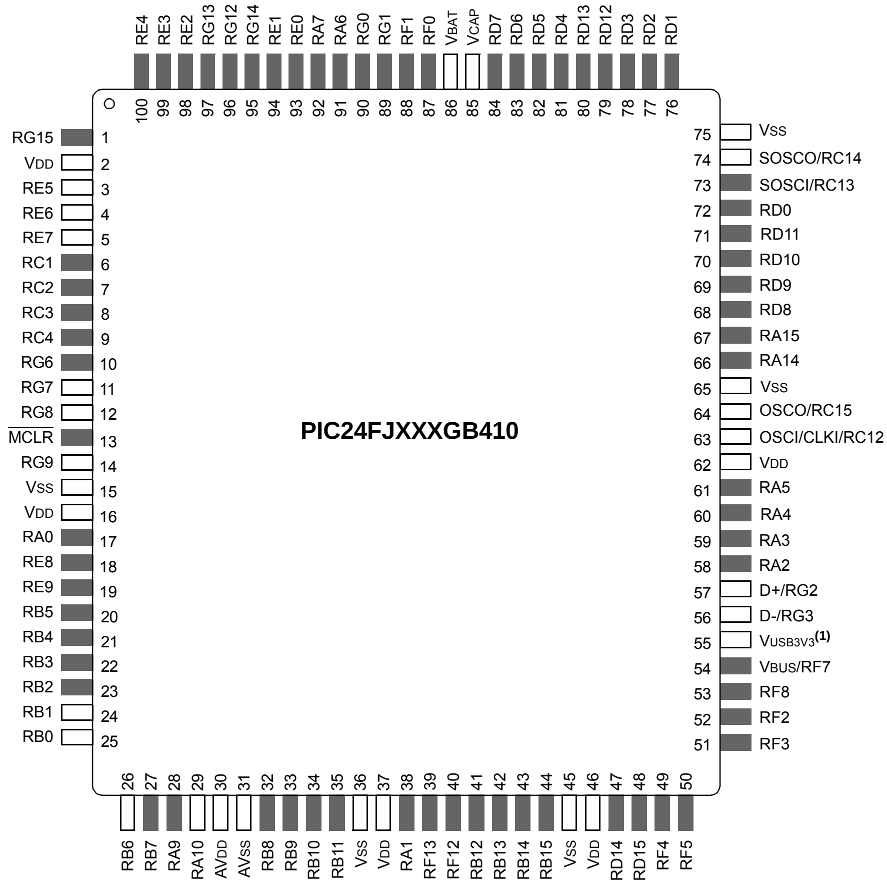
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64ga410t-i-pt

Pin Diagrams (Continued)

100-Pin TQFP



Legend: **Shaded pins** indicate pins tolerant to up to +5.5 VDC. See Table 4 for a complete description of pin functions.

Note 1: PIC24FJ256GB410 devices use VUSB3V3 instead of RF6.

TABLE 1-5: PIC24FJ256GB412 FAMILY PINOUT DESCRIPTION

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
AN0	16	25	K2	I	ANA	A/D Analog Inputs
AN1	15	24	K1	I	ANA	
AN1-	15	24	K1	I	ANA	
AN2	14	23	J2	I	ANA	
AN3	13	22	J1	I	ANA	
AN4	12	21	H2	I	ANA	
AN5	11	20	H1	I	ANA	
AN6	17	26	L1	I	ANA	
AN7	18	27	J3	I	ANA	
AN8	21	32	K4	I	ANA	
AN9	22	33	L4	I	ANA	
AN10	23	34	H5	I	ANA	
AN11	24	35	K5	I	ANA	
AN12	27	41	J7	I	ANA	
AN13	28	42	L7	I	ANA	
AN14	29	43	K7	I	ANA	
AN15	30	44	L8	I	ANA	
AN16	—	9	E1	I	ANA	
AN17	—	10	E3	I	ANA	
AN18	—	11	F4	I	ANA	
AN19	—	12	F2	I	ANA	
AN20	—	14	F3	I	ANA	
AN21	—	19	G2	I	ANA	
AN22	—	92	B5	I	ANA	
AN23	—	91	C5	I	ANA	
AVDD	19	30	J4	P	—	Positive Supply for Analog modules
AVSS	20	31	L3	P	—	Ground Reference for Analog modules
C1INA	11	20	H1	I	ANA	Comparator 1 Input A
C1INB	12	21	H2	I	ANA	Comparator 1 Input B
C1INC	5,8	11,14	F4,F3	I	ANA	Comparator 1 Input C
C1IND	4	10	E3	I	ANA	Comparator 1 Input D
C2INA	13	22	J1	I	ANA	Comparator 2 Input A
C2INB	14	23	J2	I	ANA	Comparator 2 Input B
C2INC	8	14	F3	I	ANA	Comparator 2 Input C
C2IND	6	12	F2	I	ANA	Comparator 2 Input D
C3INA	55	84	C7	I	ANA	Comparator 3 Input A
C3INB	54	83	D7	I	ANA	Comparator 3 Input B
C3INC	8,45	14,71	F3,C11	I	ANA	Comparator 3 Input C
C3IND	44	70	D11	I	ANA	Comparator 3 Input D
CLC3OUT	46	72	D9	O	DIG	CLC3 Output
CLC4OUT	42	68	E9	O	DIG	CLC4 Output

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

6.2 RTSP Operation

The PIC24F Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user to erase blocks of eight rows (512 instructions) at a time and to program one row at a time. It is also possible to program two words.

The 8-row erase blocks and single row write blocks are edge-aligned, from the beginning of program memory on boundaries of 1536 bytes and 192 bytes, respectively.

When data is written to program memory using `TBLWT` instructions, the data is not written directly to memory. Instead, data written using Table Writes is stored in holding latches until the programming sequence is executed.

Any number of `TBLWT` instructions can be executed and a write will be successfully performed. However, 64 `TBLWT` instructions are required to write the full row of memory.

To ensure that no data is corrupted during a write, any unused address should be programmed with FFFFFFh. This is because the holding latches reset to an unknown state, so if the addresses are left in the Reset state, they may overwrite the locations on rows which were not rewritten.

The basic sequence for RTSP programming is:

- Set up a Table Pointer to point to the programming latches
- Perform a series of `TBLWT` instructions to load the buffers
- Set the NVM Address registers to point to the destination

Programming is performed by setting the control bits in the NVMCON register.

Data can be loaded in any order and the holding registers can be written to multiple times before performing a write operation. Subsequent writes, however, will wipe out any previous writes.

Note:	Writing to a location multiple times without erasing is *not* recommended.

All of the Table Write operations are single-word writes (2 instruction cycles), because only the buffers are written. A programming cycle is required for programming each row.

6.3 JTAG Operation

The PIC24F family supports JTAG boundary scan. Boundary scan can improve the manufacturing process by verifying pin to PCB connectivity.

6.4 Enhanced In-Circuit Serial Programming

Enhanced In-Circuit Serial Programming uses an on-board bootloader, known as the Program Executive (PE), to manage the programming process. Using an SPI data frame format, the Program Executive can erase, program and verify program memory. For more information on Enhanced ICSP, see the device programming specification.

6.5 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. During a programming or erase operation, the processor stalls (waits) until the operation is finished. Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished. In Dual Partition modes, programming or erasing the Inactive Partition does not stall the processor; the code in the Active Partition continues to execute during the programming operation.

For more information on programming the device, please refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Dual Partition Flash Program Memory"** (DS70005156).

6.6 Control Registers

There are four SFRs used to read and write the program Flash memory:

- NVMCON
- NVMKEY
- NVMADRL
- NVMADRH

The NVMCON register (Register 6-1) controls which blocks are to be erased, which memory type is to be programmed and when the programming cycle starts.

NVMKEY is a write-only register that is used for write protection. To start a programming or erase sequence, the user must consecutively write 55h and AAh to the NVMKEY register. For more information, refer to **Section 6.5 "Programming Operations"**.

The NVMADRL and NVMADRH registers contain the lower word and upper byte of the destination address of the NVM write or erase operation. Some operations (e.g., chip erase, Inactive Partition erase) operate on fixed locations and do not require an address value.

9.8 Reference Clock

In addition to the CLKO output (FOSC/2), available in certain oscillator modes, the device clock in the PIC24FJ256GA412/GB412 family devices can also be configured to provide a reference clock output signal to a port pin. This feature is available in all oscillator configurations and allows the user to select a greater range of clock submultiples to drive external devices in the application.

This reference clock output is controlled by the REFOCONL register (Register 9-4). Setting the ROEN bit (REFOCON<15>) makes the clock signal available on the REFO pin. The ROSEL<3:0> bits (REFOCONL<3:0>) determine which clock source is used for the reference clock output.

The REFOCONH and REFOTRIML registers (Register 9-5 and Register 9-6) select the divider from the selected clock input source from a wide range of options. The RODIV<14:0> bits (REFOCONH<14:0>) enable the selection of integer clock divider options, from 1:1 to 1:65,534. The ROTRIM<8:0> bits (REFOTRIML<15:7>) allow the user to add a fractional submultiple of the clock input to the RODIVx value.

The ROSWEN bit (REFOCONL<9>) indicates that the clock divider is currently being switched. In order to change the values of the RODIVx or ROTRIMx bits:

1. Verify that ROSWEN is clear
2. Write the updated values to the ROTRIMx and RODIVx bits.
3. Set the ROSWEN bit, then wait until it is clear before assuming that the REFO clock is valid.

The ROSLP bit (REFOCONL<11>) determines if the reference source is available on REFO when the device is in Sleep mode.To use the reference clock output in Sleep mode, the ROSLP bit must be set and the clock selected by the ROSELx bits must be enabled for operation during Sleep mode, if possible. Clearing the ROSELx bits allows the reference output frequency to change as the system clock changes during any clock switches. The ROOUT bit enables/disables the reference clock output on the REFO pin.

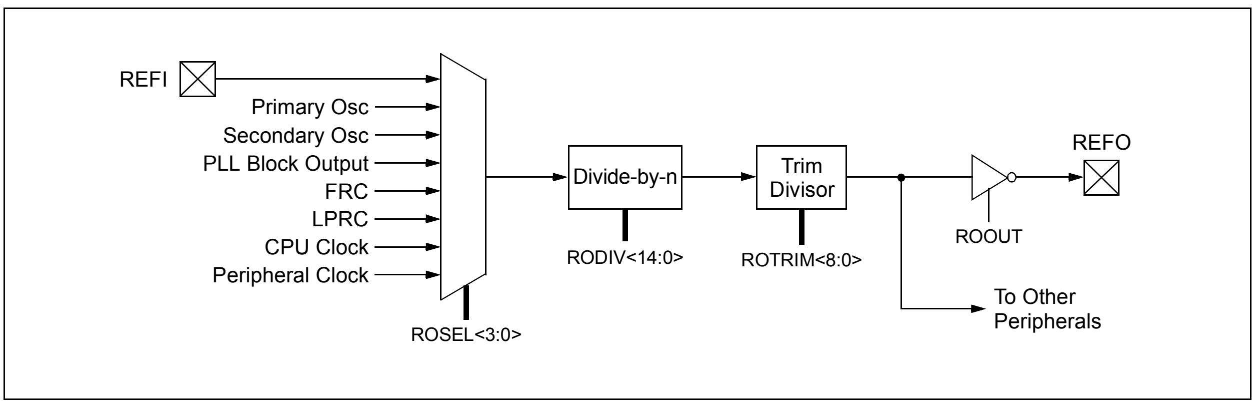
The ROACTIV bit (REFOCONL<8>) indicates that the module is active; it can be cleared by disabling the module (ROEN = `0`). The user must not change the reference clock source, or adjust the trim or divider when the ROACTIV bit indicates that the module is active. To avoid glitches, the user should not disable the module until the ROACTIV bit is '`1`'.

9.8.1 REMAPPABLE OUTPUT

For PIC24FJ256GA412/GB412 family devices, the reference clock output is not available as a dedicated pin function. Instead, it is made available as an optional remappable digital output. If the reference clock output is required for an external consumer, it must be mapped to an available output pin. See **Section 11.5.3.2 "Output Mapping"** for more information.

When REFO is mapped to RP29 (RB15 pin), a reference clock frequency of up to 32 MHz may be used. The drive strength on this pin is also compatible with the fixed REFO pin on previous PIC24F devices. If REFO is mapped to any other output pin, the maximum reference clock frequency is limited to 16 MHz, with a lower drive strength.

FIGURE 9-3: SIMPLIFIED REFERENCE CLOCK BLOCK DIAGRAM



REGISTER 10-6: PMD3: PERIPHERAL MODULE DISABLE REGISTER 3

U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0
—	—	—	—	—	CMPMD	—	PMMD
bit 15							bit 8

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0
CRCMD	DACMD	—	—	U3MD	I2C3MD	I2C2MD	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10 **CMPMD:** Triple Comparator Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 9 **Unimplemented:** Read as ‘0’

bit 8 **PMMD:** Enhanced Parallel Master Port Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 7 **CRCMD:** CRC Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 6 **DACMD:** DAC Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 5-4 **Unimplemented:** Read as ‘0’

bit 3 **U3MD:** UART3 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 2 **I2C3MD:** I2C3 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 1 **I2C2MD:** I2C2 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 0 **Unimplemented:** Read as ‘0’

TABLE 11-4: PORTC REGISTER MAP(1)

Register Name	Bit Range	Bits 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANSC	15:0	—	—	—	—	—	—	—	—	—	—	—	ANSC<4:1>				—
TRISC	15:0	TRISC15	—	—	TRISC12	—	—	—	—	—	—	—	TRISC<4:1>				—
PORTC	15:0	PORTC<15:12>				—	—	—	—	—	—	—	PORTC<4:1>				—
LATC	15:0	LATC15	—	—	LATC12	—	—	—	—	—	—	—	LATC<4:1>				—
ODCC	15:0	ODCC15	—	—	ODCC12	—	—	—	—	—	—	—	ODCC<4:1>				—
IOCPC	15:0	IOCPC<15:12>				—	—	—	—	—	—	—	IOCPC<4:1>				—
IOCNC	15:0	IOCNC<15:12>				—	—	—	—	—	—	—	IOCNC<4:1>				—
IOCFC	15:0	IOCFC<15:12>				—	—	—	—	—	—	—	IOCFC<4:1>				—
IOCPUC	15:0	IOCPUC<15:12>				—	—	—	—	—	—	—	IOCPUC<4:1>				—
IOCPDC	15:0	IOCPDC<15:12>				—	—	—	—	—	—	—	IOCPDC<4:1>				—

Legend: — = unimplemented, read as '0'.

Note 1: PORT register maps show full pin count devices. Please refer to Table 1-4 and Table 1-5 for pin count-specific PORT I/O implementation.

TABLE 11-5: PORTD REGISTER MAP(1)

Register Name	Bit Range	Bits 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANSD	15:0	ANSD<15:0>															
TRISD	15:0	TRISD<15:0>															
PORTD	15:0	PORTD<15:0>															
LATD	15:0	LATD<15:0>															
ODCD	15:0	ODCD<15:0>															
IOCPD	15:0	IOCPD<15:0>															
IOCND	15:0	IOCND<15:0>															
IOCFD	15:0	IOCFD<15:0>															
IOCPUD	15:0	IOCPUD<15:0>															
IOCPDD	15:0	IOCPDD<15:0>															

Legend: — = unimplemented, read as '0'.

Note 1: PORT register maps show full pin count devices. Please refer to Table 1-4 and Table 1-5 for pin count-specific PORT I/O implementation.

14.4 Input Capture Mode

Input Capture mode is used to capture a timer value from an independent timer base upon an event on an input pin or other internal trigger source. The input capture features are useful in applications requiring frequency (time period) and pulse measurement. Figure 14-6 depicts a simplified block diagram of Input Capture mode.

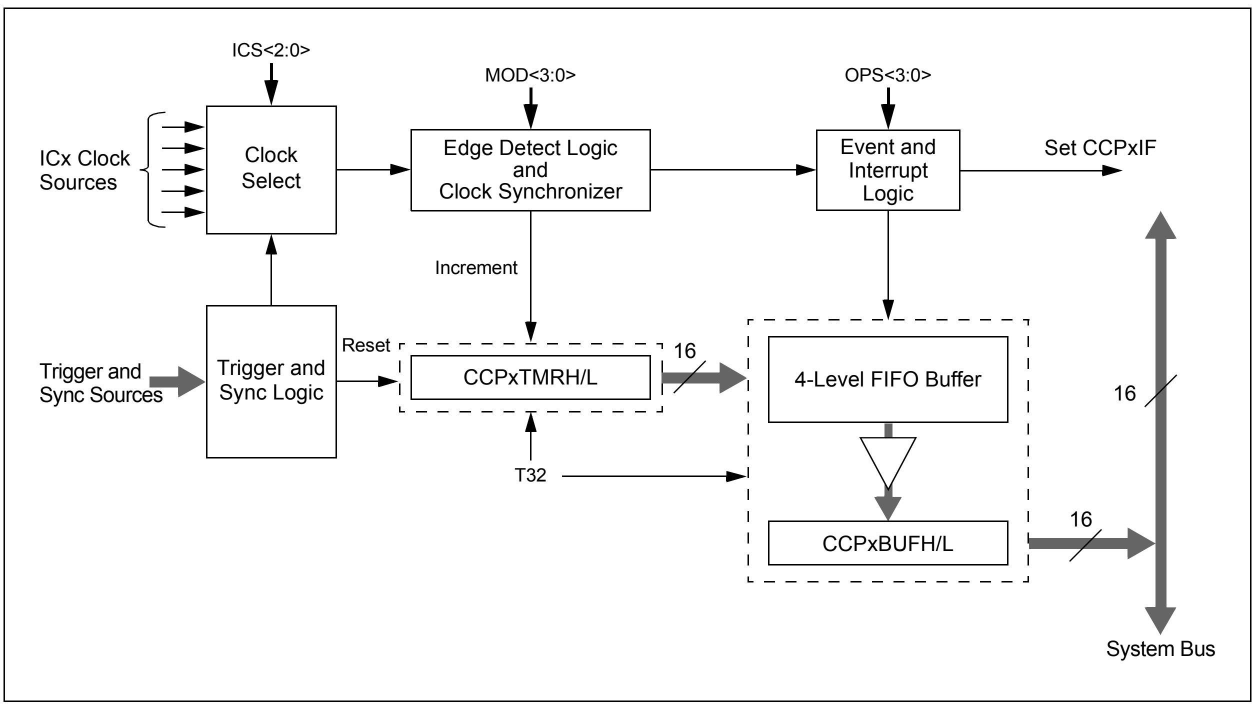
Input Capture mode uses a dedicated 16/32-bit, synchronous, up counting timer for the capture function. The timer value is written to the FIFO when a capture event occurs. The internal value may be read (with a synchronization delay) using the CCPxTMRH/L register.

To use Input Capture mode, the CCSEL bit (CCPxCON1L<4>) must be set. The T32 and the MOD<3:0> bits are used to select the proper Capture mode, as shown in Table 14-3.

TABLE 14-3: INPUT CAPTURE MODES

MOD<3:0> (CCPxCON1L<3:0>)	T32 (CCPxCON1L<5>)	Operating Mode
0000	0	Edge Detect (16-bit capture)
0000	1	Edge Detect (32-bit capture)
0001	0	Every Rising (16-bit capture)
0001	1	Every Rising (32-bit capture)
0010	0	Every Falling (16-bit capture)
0010	1	Every Falling (32-bit capture)
0011	0	Every Rise/Fall (16-bit capture)
0011	1	Every Rise/Fall (32-bit capture)
0100	0	Every 4th Rising (16-bit capture)
0100	1	Every 4th Rising (32-bit capture)
0101	0	Every 16th Rising (16-bit capture)
0101	1	Every 16th Rising (32-bit capture)

FIGURE 14-6: INPUT CAPTURE x BLOCK DIAGRAM



NOTES:

REGISTER 16-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Trigger/Synchronization Source Selection bits

11111 = This OC module[(1)]
11110 = OCTRIG1 external input
11101 = OCTRIG2 external input
11100 = CTMU[(2)]
11011 = A/D[(2)]
11010 = Comparator 3[(2)]
11001 = Comparator 2[(2)]
11000 = Comparator 1[(2)]
10111 = SCCP5 capture/compare
10110 = SCCP4 capture/compare
10101 = SCCP3 capture/compare
10100 = SCCP2 capture/compare
10011 = MCCP1 capture/compare
10010 = Input Capture 3[(2)]
10001 = Input Capture 2[(2)]
10000 = Input Capture 1[(2)]
01111 = SCCP7 capture/compare
01110 = SCCP6 capture/compare
01101 = Timer3
01100 = Timer2
01011 = Timer1
01010 = SCCP7 sync/trigger
01001 = SCCP6 sync/trigger
01000 = SCCP5 sync/trigger
00111 = SCCP4 sync/trigger
00110 = SCCP3 sync/trigger
00101 = SCCP2 sync/trigger
00100 = MCCP1 sync/trigger
00011 = Output Compare 5[(1)]
00010 = Output Compare 3[(1)]
00001 = Output Compare 1[(1)]
00000 = Not synchronized to any other module

Note 1: Never use an OCx module as its own trigger source, either by selecting this mode or another equivalent SYNCSELx setting.

2: Use these inputs as trigger sources only and never as sync sources.

3: The DCB<1:0> bits are double-buffered in PWM modes only (OCM<2:0> (OCxCON1<2:0>) = 111, 110).

REGISTER 17-2: SPIxCON1H: SPIx CONTROL REGISTER 1 HIGH (CONTINUED)

bit 6 **FRMSYNC:** Frame Sync Pulse Direction Control bit
1 = Frame Sync pulse input (slave)
0 = Frame Sync pulse output (master)

bit 5 **FRMPOL:** Frame Sync/Slave Select Polarity bit
1 = Frame Sync pulse/slave select is active-high
0 = Frame Sync pulse/slave select is active-low

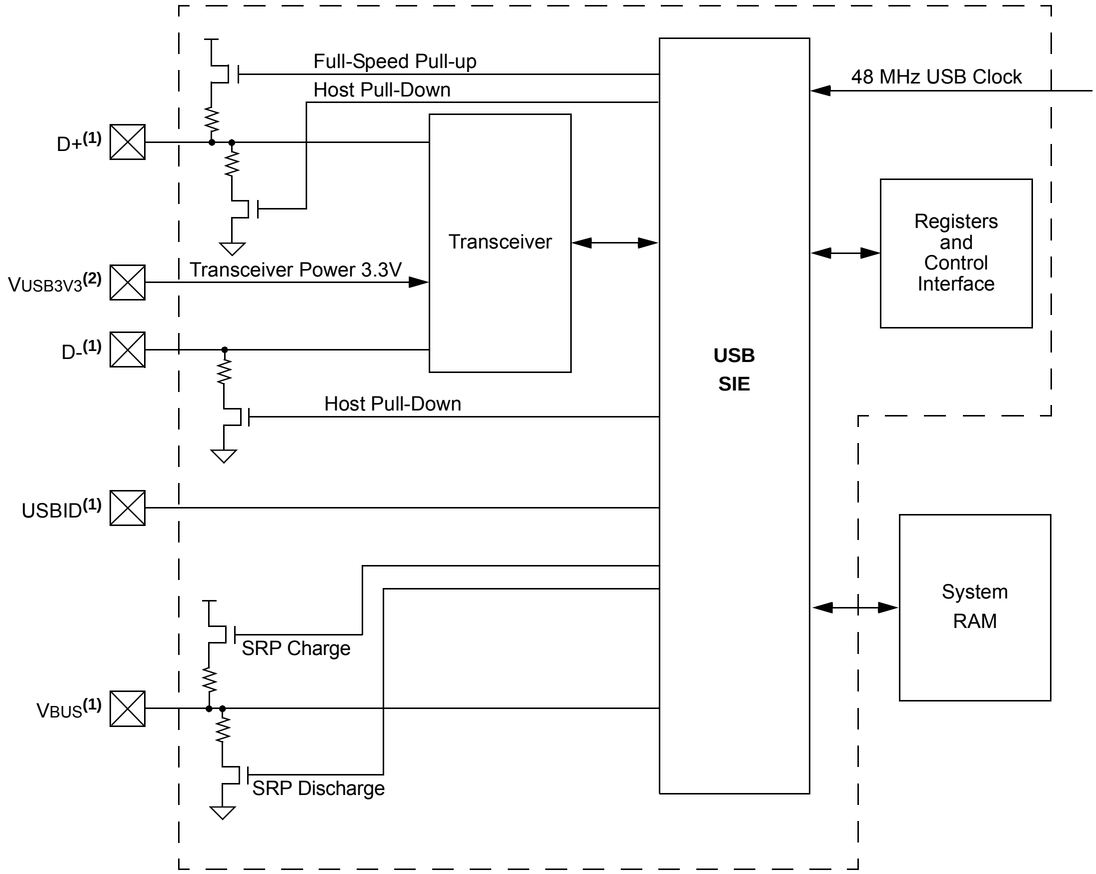
bit 4 **MSSEN:** Master Mode Slave Select Enable bit
1 = SPIx slave select support is enabled with polarity determined by FRMPOL ($\overline{\text{SSx}}$ pin is automatically driven during transmission in Master mode)
0 = Slave select SPIx support is disabled ($\overline{\text{SSx}}$ pin will be controlled by port IO)

bit 3 **FRMSYPW:** Frame Sync Pulse-Width bit
1 = Frame Sync pulse is one serial word length wide (as defined by MODE<32,16>/WLENGTH<4:0>)
0 = Frame Sync pulse is one clock (SCK) wide

bit 2-0 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits
Controls the number of serial words transmitted per Sync pulse.
111 = Reserved
110 = Reserved
101 = Generates a Frame Sync pulse on every 32 serial words
100 = Generates a Frame Sync pulse on every 16 serial words
011 = Generates a Frame Sync pulse on every 8 serial words
010 = Generates a Frame Sync pulse on every 4 serial words
001 = Generates a Frame Sync pulse on every 2 serial words (value used by audio protocols)
000 = Generates a Frame Sync pulse on each serial word

Note 1: AUDEN can only be written when the SPIEN bit = 0.
2: AUDMONO can only be written when the SPIEN bit = 0 and is only valid for AUDEN = 1.
3: URDTEN is only valid when IGNTUR = 1.
4: AUDMOD<1:0> can only be written when the SPIEN bit = 0 and is only valid when AUDEN = 1. When NOT in PCM/DSP mode, this module functions as if FRMSYPW = 1, regardless of its actual value.

FIGURE 20-1: USB OTG MODULE BLOCK DIAGRAM



Note 1: Pins are multiplexed with digital I/O and other device features.

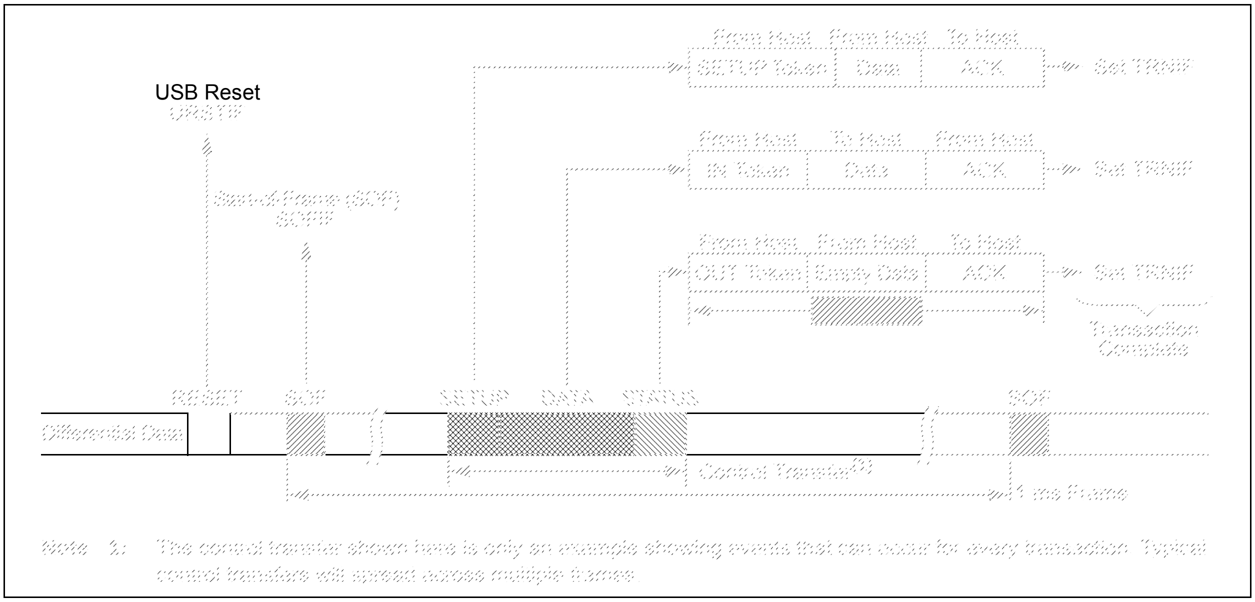
2: Connecting VBUS3V3 to VDD is highly recommended, as floating this input can cause increased IPD currents. The pin should be tied to VDD when the USB functions are not used.

20.3.1 CLEARING USB OTG INTERRUPTS

Unlike device-level interrupts, the USB OTG interrupt status flags are not freely writable in software. All USB OTG flag bits are implemented as hardware settable only bits. Additionally, these bits can only be cleared in software by writing a '1' to their locations (i.e., performing a MOV type instruction). Writing a '0' to a flag bit (i.e., a BCLR instruction) has no effect.

Note:	Throughout this data sheet, a bit that can only be cleared by writing a '1' to its location is referred to as "Write 1 to Clear". In register descriptions, this function is indicated by the descriptor, "K".

FIGURE 20-9: EXAMPLE OF A USB TRANSACTION AND INTERRUPT EVENTS



20.4 Device Mode Operation

The following section describes how to perform a common Device mode task. In Device mode, USB transfers are performed at the transfer level. The USB module automatically performs the status phase of the transfer.

20.4.1 ENABLING DEVICE MODE

1. Reset the Ping-Pong Buffer Pointers by setting, then clearing, the Ping-Pong Buffer Reset bit, PPBRST (U1CON<1>).
2. Disable all interrupts (U1IE and U1EIE = 00h).
3. Clear any existing interrupt flags by writing FFh to U1IR and U1EIR.
4. Verify that VBUS is present (non-OTG devices only).
5. Enable the USB module by setting the USBEN bit (U1CON<0>).
6. Set the OTGEN bit (U1OTGCON<2>) to enable OTG operation.
7. Enable the endpoint zero buffer to receive the first setup packet by setting the EPRXEN and EPHSHK bits for Endpoint 0 (U1EP0<3,0> = 1).
8. Power up the USB module by setting the USBPWR bit (U1PWRC<0>).
9. Enable the D+ pull-up resistor to signal an attach by setting the DPPULUP bit (U1OTGCON<7>).

TABLE 25-1: DES/3DES KEY SOURCE SELECTION

Mode of Operation	KEYMOD<1:0>	KEYSRC<3:0>	Session Key Source (SESSKEY) 0	Session Key Source (SESSKEY) 1	OTP OR RAM Array Address
64-Bit DES	00	0000[1]	CRYKEY<63:0>		—
		0001	DES Key #1	Key Config Error[2]	<63:0>
		0010	DES Key #2		<127:64>
		0011	DES Key #3		<191:128>
		0100	DES Key #4		<255:192>
		0101	DES Key #5		<319:256>
		0110	DES Key #6		<383:320>
		0111	DES Key #7		<447:384>
		1001	DES Key #1 (RAM)		<63:0>
		1010	DES Key #2 (RAM)		<127:64>
		1011	DES Key #3 (RAM)		<191:128>
		1100	DES Key #4 (RAM)		<255:192>
		1101	DES Key #5 (RAM)		<319:256>
		1110	DES Key #6 (RAM)		<383:320>
		1111	DES Key #7 (RAM)		<447:384>
		All Others	Key Config Error[2]		—
64-Bit, 2-Key 3DES (Standard 2-Key E-D-E/D-E-D)	01	0000[1]	CRYKEY<63:0> (1st/3rd) CRYKEY<127:64> (2nd)		—
		0001	DES Key #1 (1st/3rd) DES Key #2 (2nd)	Key Config Error[2]	<63:0> <127:64>
		0010	DES Key #3 (1st/3rd) DES Key #4 (2nd)		<191:128> <255:192>
		0011	DES Key #5 (1st/3rd) DES Key #6 (2nd)		<319:256> <383:320>
		0100	DES Key #7 (1st/3rd) DES Key #8 (2nd)		<447:384> <511:448>
		1001	DES Key #9 (1st/3rd) (RAM) DES Key #10 (2nd) (RAM)		<63:0> <127:64>
		1010	DES Key #11 (1st/3rd) (RAM) DES Key #12 (2nd) (RAM)		<191:128> <255:192>
		1011	DES Key #13 (1st/3rd) (RAM) DES Key #14 (2nd) (RAM)		<319:256> <383:320>
		1100	DES Key #15 (1st/3rd) (RAM) DES Key #16 (2nd) (RAM)		<447:384> <511:448>
		1111	Reserved[2]		—
		All Others	Key Config Error[2]		—
(Reserved)	10	xxxx	Key Config Error[2]		—

Note 1: This configuration is considered a key configuration error (KEYFAIL bit is set) if SWKYDIS is also set.

2: The KEYFAIL bit (CRYSTAT<1>) is set when these configurations are selected and remains set until a valid configuration is selected.

29.0 TRIPLE COMPARATOR MODULE

> **Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Scalable Comparator Module"** (DS39734). The information in this data sheet supersedes the information in the FRM.

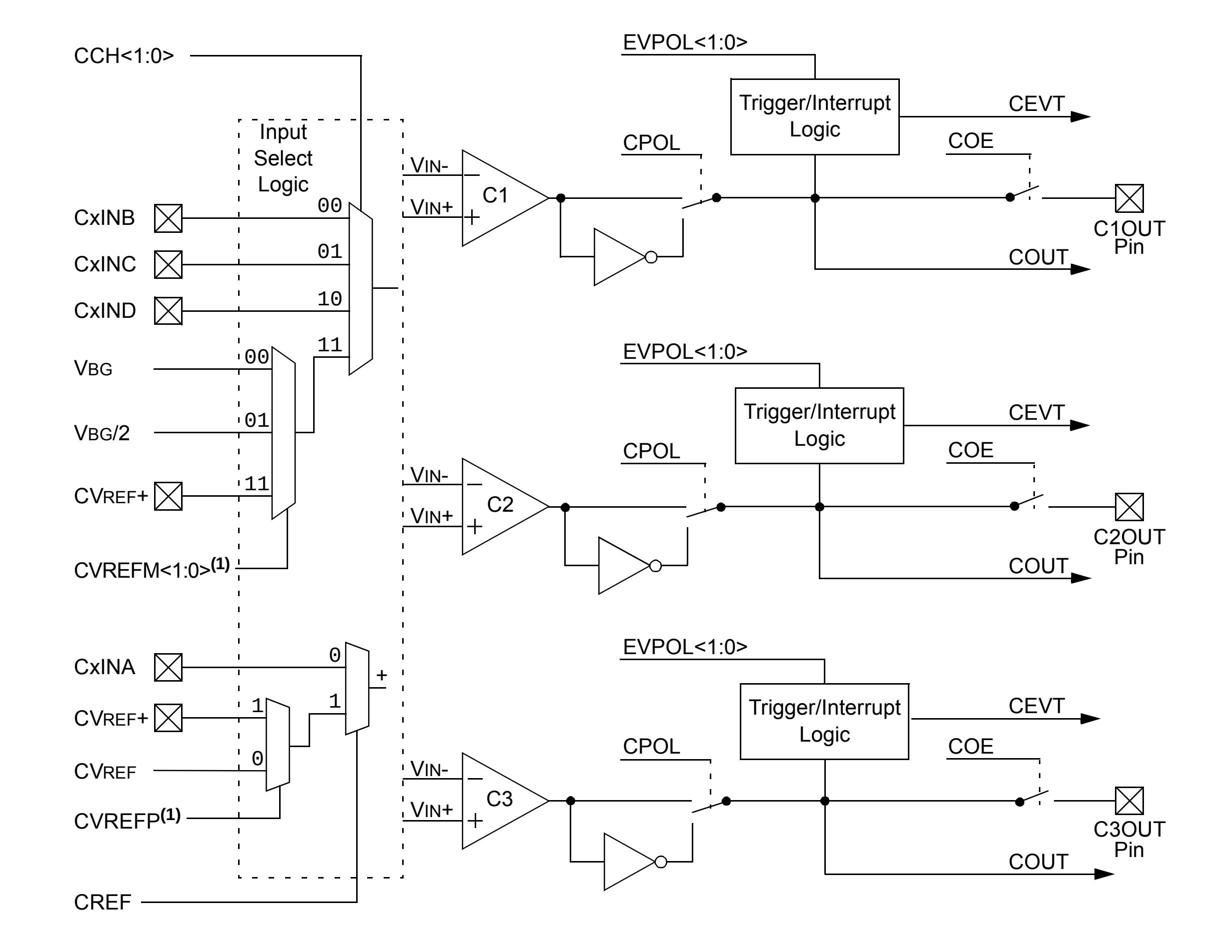
The triple comparator module provides three dual input comparators. The inputs to the comparator can be configured to use any one of five external analog inputs (CxINA, CxINB, CxINC, CxIND and VREF+) and a voltage reference input from one of the internal band gap references or the comparator voltage reference generator (VBG, VBG/2 and CVREF).

The comparator outputs may be directly connected to the CxOUT pins. When the respective COE bit equals '1', the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module in shown in Figure 29-1. Diagrams of the possible individual comparator configurations are shown in Figure 29-2.

Each comparator has its own control register, CMxCON (Register 29-1), for enabling and configuring its operation. The output and event status of all three comparators is provided in the CMSTAT register (Register 29-2).

FIGURE 29-1: TRIPLE COMPARATOR MODULE BLOCK DIAGRAM



Note 1: Refer to the CVRCON register (Register 30-1) for bit details.

REGISTER 33-6: FWDT: WATCHDOG TIMER CONFIGURATION WORD (CONTINUED)

bit 3-0 **WDTPS<3:0>:** Watchdog Timer Postscaler Select bits

1111 = 1:32,768
1110 = 1:16,384
1101 = 1:8,192
1100 = 1:4,096
1011 = 1:2,048
1010 = 1:1,024
1001 = 1:512
1000 = 1:256
0111 = 1:128
0110 = 1:64
0101 = 1:32
0100 = 1:16
0011 = 1:8
0010 = 1:4
0001 = 1:2
0000 = 1:1

REGISTER 33-8: FICD: ICD CONFIGURATION WORD

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R/PO-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
BTSWP	—	—	—	—	—	—	—
bit 15							bit 8

R/PO-1	U-1	R/PO-1	U-1	U-1	U-1	R/PO-1	R/PO-1
$\overline{\text{DEBUG}}$	—	JTAGEN	—	—	—	ICS1	ICS0
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-16 **Unimplemented:** Read as ‘1’

bit 15 **BTSWP:** BOOTSWP Instruction Disable bit
1 = BOOTSWP instruction is disabled
0 = BOOTSWP instruction is allowed

bit 14-8 **Unimplemented:** Read as ‘1’

bit 7 **$\overline{\text{DEBUG}}$:** Background Debugger Enable bit
1 = Device resets into Operational mode
0 = Device resets into Debug mode

bit 6 **Unimplemented:** Read as ‘1’

bit 5 **JTAGEN:** JTAG Port Enable bit
1 = JTAG port is enabled
0 = JTAG port is disabled

bit 4-2 **Unimplemented:** Read as ‘1’

bit 1-0 **ICS<1:0>:** Emulator Pin Placement Select bits
11 = Emulator functions are shared with PGEC1/PGED1
10 = Emulator functions are shared with PGEC2/PGED2
01 = Emulator functions are shared with PGEC3/PGED3
00 = Reserved; do not use

TABLE 36-39: A/D MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of: VDD – 0.3 or 2.2	—	Lesser of: VDD + 0.3 or 3.6	V	
AD02	AVSS	Module VSS Supply	VSS – 0.3	—	VSS + 0.3	V	
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 1.7	—	AVDD	V	
AD06	VREFL	Reference Voltage Low	AVSS	—	AVDD – 1.7	V	
AD07	VREF	Absolute Reference Voltage	AVSS – 0.3	—	AVDD + 0.3	V	
Analog Input							
AD10	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	**(Note 2)**
AD11	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	
AD12	VINL	Absolute VINL Input Voltage	AVSS – 0.3	—	AVDD/3	V	
AD13		Leakage Current	—	±1.0	±610	nA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V, Source Impedance = 2.5 kΩ
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	2.5K	Ω	10-bit
Accuracy							
AD20B	Nr	Resolution	—	12	—	bits	
AD21B	INL	Integral Nonlinearity	—	±1	<±2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V
AD22B	DNL	Differential Nonlinearity	—	—	<±1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V
AD23B	GERR	Gain Error	—	±1	±3	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V
AD24B	EOFF	Offset Error	—	±1	±2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V
AD25B		Monotonicity(1)	—	—	—	—	Guaranteed

Note 1: The conversion result never decreases with an increase in the input voltage and has no missing codes.

2: Measurements are taken with the external VREF+ and VREF- used as the voltage reference.

TABLE 36-40: A/D CONVERSION TIMING REQUIREMENTS[(1)]

AC CHARACTERISTICS			Standard Operating Conditions: 2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	A/D Clock Period	278	—	—	ns	
AD51	tRC	A/D Internal RC Oscillator Period	—	250	—	ns	
Conversion Rate							
AD55	tCONV	Conversion Time	—	14	—	TAD	
AD56	FCNV	Throughput Rate	—	—	200	ksps	AVDD > 2.7V
AD57	tSAMP	Sample Time	—	1	—	TAD	
Clock Parameters							
AD61	tPSS	Sample Start Delay from Setting Sample bit (SAMP)	2	—	3	TAD	

Note 1: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

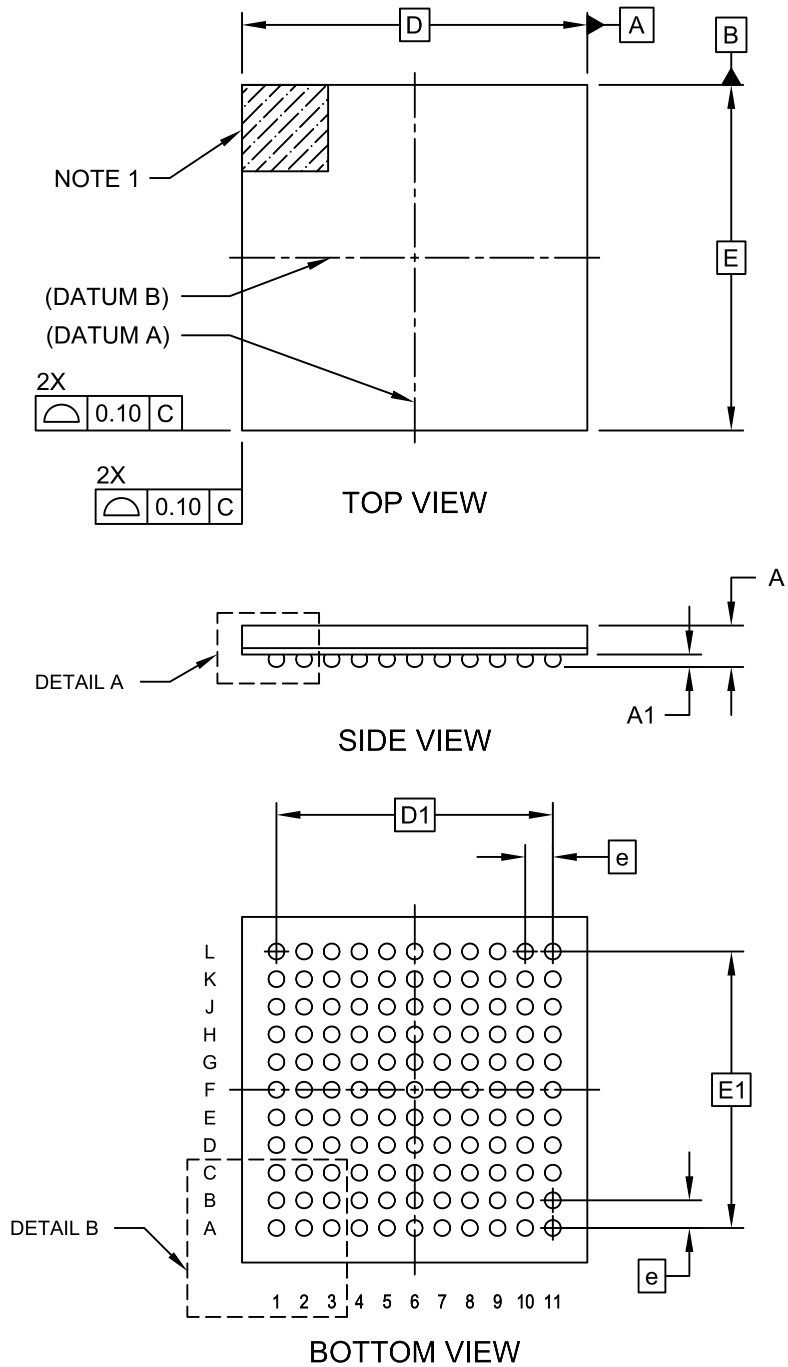
TABLE 36-41: 10-BIT DAC SPECIFICATIONS

AC CHARACTERISTICS			**Operating Conditions:** -40°C < TA < +85°C, 2.0V < (A)VDD < 3.6V[(1)]				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
DAC01		Resolution	10	—	—	bits	
DAC02		DVREF+ Input Voltage Range	—	—	AVDD	V	
DAC03	DNL	Differential Linearity Error	-1	—	+1	LSb	
DAC04	INL	Integral Linearity Error	-3.0	—	+3.0	LSb	
DAC05		Offset Error	-20	—	+20	mV	Code 000h
DAC06		Gain Error	-3.0	—	+3.0	LSb	Code 3FFh, not including offset error

Note 1: Unless otherwise stated, test conditions are with VDD = AVDD = DVREF+ = 3.3V, 3 kΩ load to VSS.

121-Ball Plastic Thin Profile Fine Pitch Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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