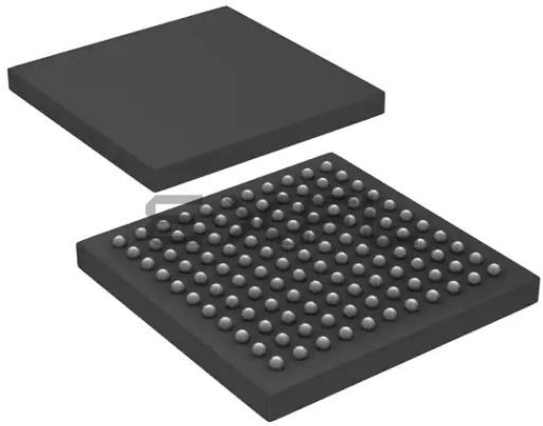
Microchip Technology - PIC24FJ64GA412-I/BG Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	102
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64ga412-i-bg

FIGURE 3-1: PIC24F CPU CORE BLOCK DIAGRAM

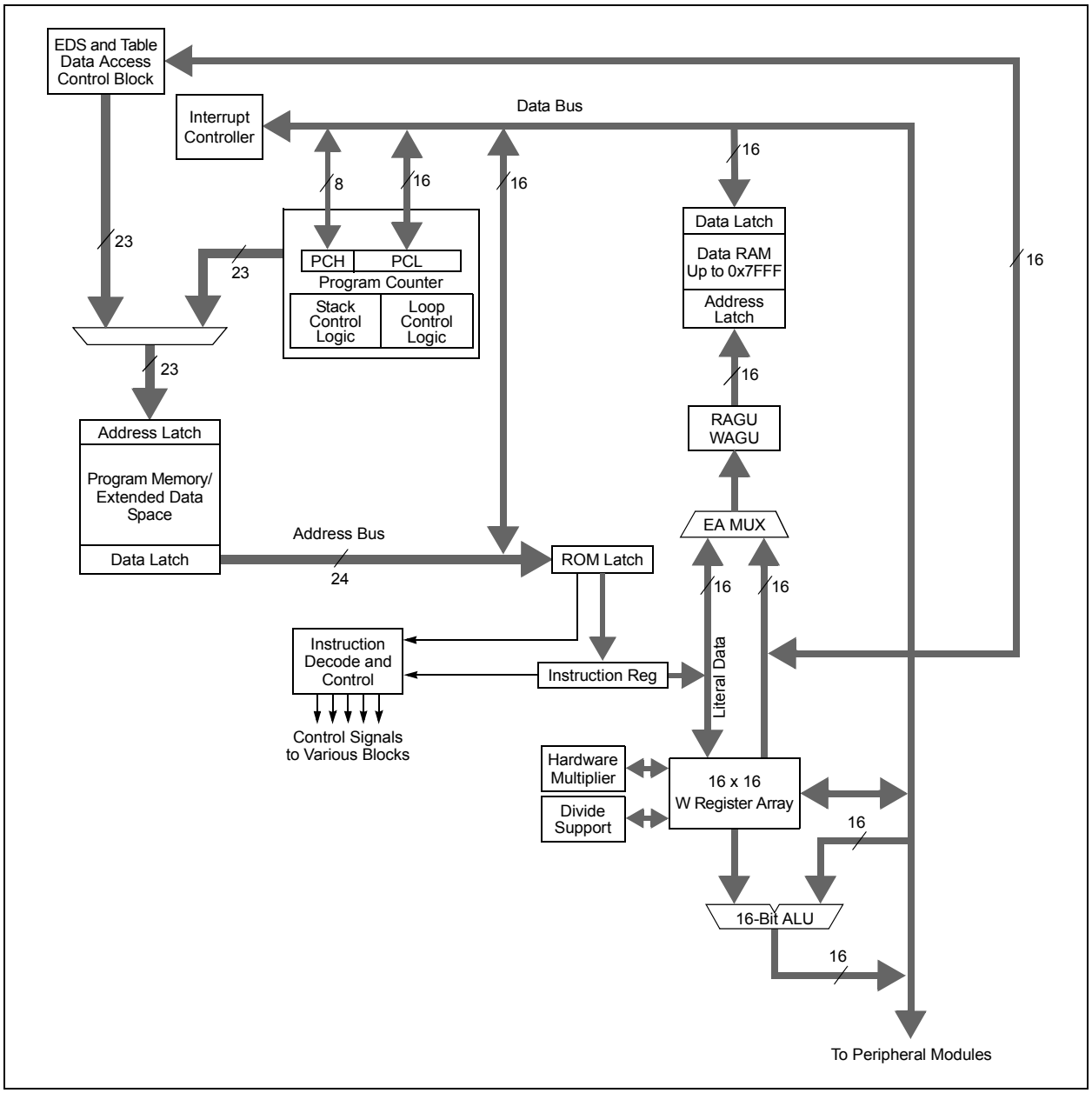


TABLE 3-1: CPU CORE REGISTERS

Register(s) Name	Description
W0 through W15	Working Register Array
PC	23-Bit Program Counter
SR	ALU STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
RCOUNT	REPEAT Loop Counter Register
CORCON	CPU Control Register
DISICNT	Disable Interrupt Count Register
DSRPAG	Data Space Read Page Register
DSWPAG	Data Space Write Page Register

4.4.2 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the program space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two, 16-bit word-wide address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space which contains the least significant data word, and TBLRDH and TBLWTH access the space which contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

1. TBLRDL (Table Read Low): In Word mode, it maps the lower word of the program space location (P<15:0>) to a data address (D<15:0>).

   In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when byte select is '1'; the lower byte is selected when it is '0'.

2. TBLRDH (Table Read High): In Word mode, it maps the entire upper word of a program address (P<23:16>) to a data address. Note that D<15:8>, the 'phantom' byte, will always be '0'.

   In Byte mode, it maps the upper or lower byte of the program word to D<7:0> of the data address, as above. Note that the data will always be '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address. The details of their operation are described in **Section 6.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Memory Page Address (TBLPAG) register. TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.

Note:	Only Table Read operations will execute in the configuration memory space where Device IDs are located. Table Write operations are not allowed.

FIGURE 4-11: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS

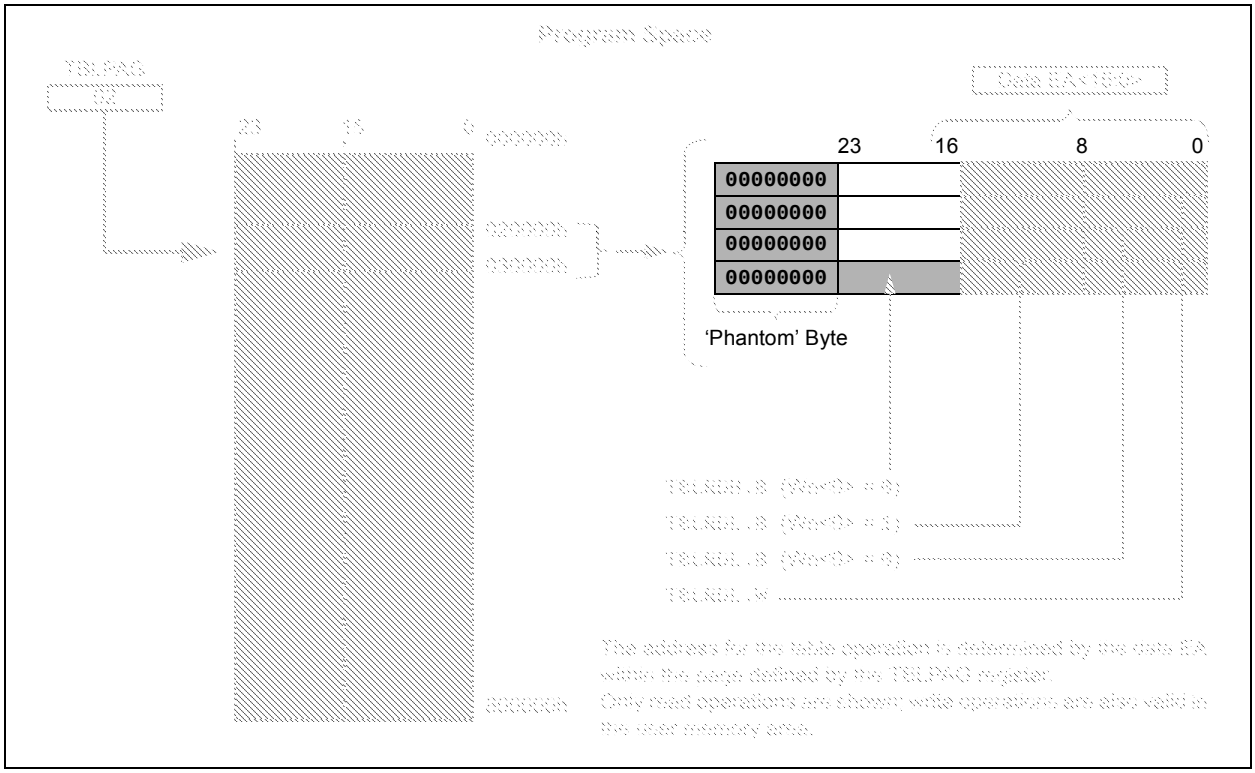


TABLE 8-2: IMPLEMENTED INTERRUPT VECTORS (CONTINUED)

Interrupt Source	Vector Number	IRQ #	IVT Address	Interrupt Bit Locations		
				Flag	Enable	Priority
UART3 Error	89	81	0000B6h	IFS5<1>	IEC5<1>	IPC20<6:4>
UART3 Receiver	90	82	0000B8h	IFS5<2>	IEC5<2>	IPC20<10:8>
UART3 Transmitter	91	83	0000BAh	IFS5<3>	IEC5<3>	IPC20<14:12>
UART4 Error	95	87	0000C2h	IFS5<7>	IEC5<7>	IPC21<14:12>
UART4 Receiver	96	88	0000C4h	IFS5<8>	IEC5<8>	IPC22<2:0>
UART4 Transmitter	97	89	0000C6h	IFS5<9>	IEC5<9>	IPC22<6:4>
UART5 Error	121	113	0000F6h	IFS7<1>	IEC7<1>	IPC28<6:4>
UART5 Receive	119	111	0000F2h	IFS6<15>	IEC6<15>	IPC27<14:12>
UART5 Transmit	120	112	0000F4h	IFS7<0>	IEC7<0>	IPC28<2:0>
UART6 Error	124	116	0000FCh	IFS7<4>	IEC7<4>	IPC29<2:0>
UART6 Receive	122	114	0000F8h	IFS7<2>	IEC7<2>	IPC28<10:8>
UART6 Transmit	123	113	0000FAh	IFS7<3>	IEC7<3>	IPC28<14:12>
USB	94	86	0000C0h	IFS5<6>	IEC5<6>	IPC21<10:8>

REGISTER 8-9: IFS3: INTERRUPT FLAG STATUS REGISTER 3 (CONTINUED)

bit 2 **MI2C2IF:** Master I2C2 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **SI2C2IF:** Slave I2C2 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **CCT6IF:** SCCP6 Timer Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 8-26: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CNIP2	CNIP1	CNIP0	—	CMIP2	CMIP1	CMIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **CNIP<2:0>:** Input Change Notification Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **CMIP<2:0>:** Comparator Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **MI2C1IP<2:0>:** Master I2C1 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **SI2C1IP<2:0>:** Slave I2C1 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-45: IPC23: INTERRUPT PRIORITY CONTROL REGISTER 23

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CCP4IP2	CCP4IP1	CCP4IP0	—	CCP3IP2	CCP3IP1	CCP3IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPI4TXIP2	SPI4TXIP1	SPI4TXIP0	—	SPI4IP2	SPI4IP1	SPI4IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **CCP4IP<2:0>:** SCCP4 Capture/Compare Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **CCP3IP<2:0>:** SCCP3 Capture/Compare Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **SPI4TXIP<2:0>:** SPI4 Transmit Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **SPI4IP<2:0>:** SPI4 General Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-52: INTTREG: INTERRUPT CONTROLLER TEST REGISTER

R-0	r-0	R/W-0	U-0	R-0	R-0	R-0	R-0
CPUIRQ	—	VHOLD	—	ILR3	ILR2	ILR1	ILR0
bit 15							bit 8

U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CPUIRQ:** Interrupt Request from Interrupt Controller CPU bit
1 = An interrupt request has occurred but has not yet been Acknowledged by the CPU; this happens when the CPU priority is higher than the interrupt priority
0 = No interrupt request is unacknowledged

bit 14 **Reserved:** Maintain as '0'

bit 13 **VHOLD:** Vector Number Capture Configuration bit
1 = VECNUM<6:0> bits contain the value of the highest priority pending interrupt
0 = VECNUM<6:0> bits contain the value of the last Acknowledged interrupt (i.e., the last interrupt that has occurred with higher priority than the CPU, even if other interrupts are pending)

bit 12 **Unimplemented:** Read as '0'

bit 11-8 **ILR<3:0>:** New CPU Interrupt Priority Level bits
1111 = CPU Interrupt Priority Level is 15
•
•
•
0001 = CPU Interrupt Priority Level is 1
0000 = CPU Interrupt Priority Level is 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **VECNUM<6:0>:** Vector Number of Pending Interrupt or Last Acknowledged Interrupt bits
When VHOLD = 1:
Indicates the vector number (from 0 to 118) of the last interrupt to occur.
When VHOLD = 0:
Indicates the vector number (from 0 to 118) of the interrupt request currently being handled.

REGISTER 10-1: DSCON: DEEP SLEEP CONTROL REGISTER(1)

R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
DSEN	—	—	RTCCMD	KEYRAMEN	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/C-0, HS
—	—	—	—	—	WAKEDIS	DSBOR(2)	RELEASE
bit 7							bit 0

Legend:	C = Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **DSEN:** Deep Sleep Enable bit
1 = Enters Deep Sleep on execution of PWRSAV #0
0 = Enters normal Sleep on execution of PWRSAV #0

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **RTCCMD:** RTCC Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 11 **KEYRAMEN:** Cryptographic Engine Key RAM Deep Sleep Enable bit
1 = Power is maintained to Key RAM during Deep Sleep and VBAT modes
0 = Power is disabled during Deep Sleep and VBAT modes

bit 10-3 **Unimplemented:** Read as '0'

bit 2 **WAKEDIS:** External Wake-up Source Disable bit
1 = External wake-up source is disabled and ignored during Deep Sleep modes
0 = External wake-up source is enabled and can be used to wake device from Deep Sleep

bit 1 **DSBOR:** Deep Sleep BOR Event bit(2)
1 = The DSBOR was active and a BOR event was detected during Deep Sleep
0 = The DSBOR was not active, or was active, but did not detect a BOR event during Deep Sleep

bit 0 **RELEASE:** I/O Pin State Release bit
1 = Upon waking from Deep Sleep, I/O pins maintain their states previous to Deep Sleep entry
0 = Releases I/O pins from their state previous to Deep Sleep entry, and allows their respective TRISx and LATx bits to control their states

Note 1: All register bits are reset only in the case of a POR event outside of Deep Sleep mode.
2: Unlike all other events, a Deep Sleep BOR event will NOT cause a wake-up from Deep Sleep; this re-arms the POR.

11.4 Interrupt-on-Change (IOC)

The interrupt-on-change function of the I/O ports allows the PIC24FJ256GA412/GB412 family of devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on any of the input port pins. This feature is capable of detecting input Change-of-States, even in Sleep mode when the clocks are disabled.

Interrupt-on-change functionality is globally enabled by setting the IOCON bit in the PADCON register (Register 11-1). Functionality is then enabled for a particular pin by setting the IOCPx and/or IOCNx register bit for that pin. Setting a value of '1' in the IOCPx register enables interrupts for low-to-high transitions, while setting a value of '1' in the IOCNx register enables interrupts for high-to-low transitions. Setting a value of '1' in both register bits will enable interrupts for either case (e.g., a pulse on the pin will generate two interrupts).

When an interrupt request is generated for a pin, the corresponding status flag bit in the IOCFx register will be set, indicating that a Change-of-State occurred on that pin. The IOCFx register bit will remain set until cleared by writing a zero to it. When any IOCFx flag bit in a given port is set, the corresponding IOCPxF bit in the IOCSTAT register (Register 11-2) will also be set. This flag indicates that a change was detected on one of the bits on the given port. The IOCPxF flag will be cleared when all IOCFx<15:0> bits are cleared.

Multiple individual status flags can be cleared by writing a zero to one or more bits using a Read-Modify-Write operation. If another edge is detected on a pin whose status bit is being cleared during the Read-Modify-Write sequence, the associated change flag will still be set at the end of the Read-Modify-Write sequence.

The user should use the instruction sequence (or equivalent) shown in Example 11-1 to clear the Interrupt-on-Change Status registers.

At the end of this sequence, the W0 register will contain a zero for each bit for which the port pin had a change detected. In this way, any indication of a pin changing will not be lost.

Due to the asynchronous and real-time nature of the interrupt-on-change, the value read on the port pins may not indicate the state of the port when the change was detected, as a second change can occur during the interval between clearing the flag and reading the port. It is up to the user code to handle this case if it is a possibility in their application. To keep this interval to a minimum, it is recommended that any code modifying the IOCFx registers be run either in the interrupt handler or with interrupts disabled.

11.4.1 PULL-UPS AND PULL-DOWNS

Each IOC pin has both a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source connected to the pin, while the pull-downs act as a current sink connected to the pin. These eliminate the need for external resistors when push button or keypad devices are connected.

The pull-ups and pull-downs are separately enabled using the IOCPUx registers (for pull-ups) and the IOCPDx registers (for pull-downs). Each IOC pin has individual control bits for its pull-up and pull-down. Setting a control bit enables the weak pull-up or pull-down for the corresponding pin.

Note:	Pull-ups and pull-downs on pins should always be disabled whenever the pin is configured as a digital output.

EXAMPLE 11-1: IOC STATUS READ/CLEAR IN ASSEMBLY

```
MOV   0xFFFF, W0   ; Initial mask value 0xFFFF -> W0
XOR   IOCFx, W0    ; W0 has '1' for each bit set in IOCFx
AND   IOCFx        ; IOCFx & W0 ->IOCFx
```

EXAMPLE 11-2: PORT READ/WRITE IN ASSEMBLY

```
MOV   0xFF00, W0   ; Configure PORTB<15:8> as inputs
MOV   W0, TRISB    ; and PORTB<7:0> as outputs
NOP                ; Delay 1 cycle
BTSS  PORTB, #13   ; Next Instruction
```

EXAMPLE 11-3: PORT READ/WRITE IN 'C'

```
TRISB = 0xFF00;              // Configure PORTB<15:8> as inputs and PORTB<7:0> as outputs
Nop();                       // Delay 1 cycle
If (PORTBbits.RB13){ };      // Next Instruction
```

REGISTER 15-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Synchronization/Trigger Source Selection bits

1111x = Reserved
11101 = Reserved
11100 = CTMU(1)
11011 = A/D(1)
11010 = Comparator 3(1)
11001 = Comparator 2(1)
11000 = Comparator 1(1)
10111 = SCCP5 capture/compare
10110 = SCCP4 capture/compare
10101 = SCCP3 capture/compare
10100 = SCCP2 capture/compare
10011 = MCCP1 capture/compare
10010 = Input Capture 3(2)
10001 = Input Capture 2(2)
10000 = Input Capture 1(2)
01111 = SCCP7 capture/compare
01110 = SCCP6 capture/compare
01101 = Timer3
01100 = Timer2
01011 = Timer1
01010 = SCCP7 sync/trigger
01001 = SCCP6 sync/trigger
01000 = SCCP5 sync/trigger
00111 = SCCP4 sync/trigger
00110 = SCCP3 sync/trigger
00101 = SCCP2 sync/trigger
00100 = MCCP1 sync/trigger
00011 = Output Compare 3
00010 = Output Compare 2
00001 = Output Compare 1
00000 = Not synchronized to any other module

Note 1: Use these inputs as trigger sources only and never as sync sources.
2: Never use an ICx module as its own trigger source by selecting this mode.

REGISTER 17-1: SPIxCON1L: SPIx CONTROL REGISTER 1 LOW (CONTINUED)

bit 9 **SMP:** SPIx Data Input Sample Phase bit
Master Mode:
1 = Input data is sampled at the end of data output time
0 = Input data is sampled at the middle of data output time
Slave Mode:
Input data is always sampled at the middle of data output time, regardless of the SMP setting.

bit 8 **CKE:** SPIx Clock Edge Select bit(1)
1 = Transmit happens on transition from active clock state to Idle clock state
0 = Transmit happens on transition from Idle clock state to active clock state

bit 7 **SSEN:** Slave Select Enable bit (Slave mode)(2)
1 = $\overline{SSx}$ pin is used by the macro in Slave mode; $\overline{SSx}$ pin is used as the slave select input
0 = $\overline{SSx}$ pin is not used by the macro ($\overline{SSx}$ pin will be controlled by the port I/O)

bit 6 **CKP:** Clock Polarity Select bit
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

bit 4 **DISSDI:** Disable SDIx Input Port bit
1 = SDIx pin is not used by the module; pin is controlled by port function
0 = SDIx pin is controlled by the module

bit 3 **DISSCK:** Disable SCKx Output Port bit
1 = SCKx pin is not used by the module; pin is controlled by port function
0 = SCKx pin is controlled by the module

bit 2 **MCLKEN:** Master Clock Enable bit(3)
1 = REFO is used by the BRG
0 = FOSC/2 is used by the BRG

bit 1 **SPIFE:** Frame Sync Pulse Edge Select bit
1 = Frame Sync pulse (Idle-to-active edge) coincides with the first bit clock
0 = Frame Sync pulse (Idle-to-active edge) precedes the first bit clock

bit 0 **ENHBUF:** Enhanced Buffer Enable bit
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

Note 1: When AUDEN (SPIxCON1H<15>) = 1, this module functions as if CKE = 0, regardless of its actual value.
2: When FRMEN = 1, SSEN is not used.
3: MCLKEN can only be written when the SPIEN bit = 0.
4: This channel is not meaningful for DSP/PCM mode as LRC follows FRMSYPW.

REGISTER 27-2: AD1CON2: A/D CONTROL REGISTER 2 (CONTINUED)

bit 1 **BUFM:** Buffer Fill Mode Select bit(1)
1 = Starts buffer filling at ADC1BUF0 on first interrupt and ADC1BUF13 on next interrupt
0 = Always starts filling buffer at ADC1BUF0

bit 0 **ALTS:** Alternate Input Sample Mode Select bit
1 = Uses channel input selects for Sample A on first sample and Sample B on next sample
0 = Always uses channel input selects for Sample A

Note 1: These bits are only applicable when the buffer is used in FIFO mode (BUFREGEN = 0). In addition, BUFS is only used when BUFM = 1.

REGISTER 27-3: AD1CON3: A/D CONTROL REGISTER 3

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	EXTSAM	PUMPEN	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADRC:** A/D Conversion Clock Source bit
1 = RC clock
0 = Clock derived from system clock

bit 14 **EXTSAM:** Extended Sampling Time bit
1 = A/D is still sampling after SAMP = 0
0 = A/D is finished sampling

bit 13 **PUMPEN:** Charge Pump Enable bit
1 = Charge pump for switches is enabled
0 = Charge pump for switches is disabled

bit 12-8 **SAMC<4:0>:** Auto-Sample Time Select bits
11111 = 31 TAD
• • •
00001 = 1 TAD
00000 = 0 TAD

bit 7-0 **ADCS<7:0>:** A/D Conversion Clock Select bits
11111111 = 256 • TCY = TAD
• • •
00000001 = 2 • TCY = TAD
00000000 = TCY = TAD

REGISTER 27-6: AD1CHS: A/D SAMPLE SELECT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB2	CH0NB1	CH0NB0	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA2	CH0NA1	CH0NA0	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **CH0NB<2:0>:** Sample B Channel 0 Negative Input Select bits
1xx = Unimplemented
011 = Unimplemented
010 = AN1
001 = Unimplemented
000 = VREF-/AVSS

bit 12-8 **CH0SB<4:0>:** Sample B Channel 0 Positive Input Select bits
See Table 27-2 for available options.

bit 7-5 **CH0NA<2:0>:** Sample A Channel 0 Negative Input Select bits
Same definitions as for CHONB<2:0>.

bit 4-0 **CH0SA<4:0>:** Sample A Channel 0 Positive Input Select bits
Same definitions as for CHOSB<4:0>.

TABLE 27-2: POSITIVE CHANNEL SELECT OPTIONS (CHOSA<4:0> OR CHOSB<4:0>)

CH0SA<4:0> or CH0SB<4:0>	Analog Channel	CH0SA<4:0> or CH0SB<4:0>	Analog Channel
11111	VBAT/2(1)	01111	AN15
11110	AVDD(1)	01110	AN14
11101	AVSS(1)	01101	AN13
11100	VBG(1)	01100	AN12
11011	Reserved	01011	AN11
11010	Reserved	01010	AN10
11001	CTMU	01001	AN9
11000	CTMU Temperature Sensor(2)	01000	AN8
10111	AN23(3)	00111	AN7
10110	AN22(3)	00110	AN6
10101	AN21(3)	00101	AN5
10100	AN20(3)	00100	AN4
10011	AN19(3)	00011	AN3
10010	AN18(3)	00010	AN2
10001	AN17(3)	00001	AN1
10000	AN16(3)	00000	AN0

Note 1: These input channels do not have corresponding memory-mapped result buffers.
2: Temperature sensor does not require AD1CTMENL<13> to be set.
3: These channels are not implemented in 64-pin devices.

REGISTER 27-12: AD1CTMENH: A/D CTMU ENABLE REGISTER (HIGH WORD)

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
—	CTMEN<30:28>			—	—	CTMEN<25:24>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN<23:16>(1)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **CTMEN<30:28>:** CTMU Enabled During Conversion bits
1 = CTMU is enabled and connected to the selected internal channel during conversion
0 = CTMU is not connected to this channel

bit 11-10 **Unimplemented:** Read as '0'

bit 9-8 **CTMEN<25:24>:** CTMU Enabled During Conversion bits
1 = CTMU is enabled and connected to the selected internal channel during conversion
0 = CTMU is not connected to this channel

bit 7-0 **CTMEN<23:16>:** CTMU Enabled During Conversion bits(1)
1 = CTMU is enabled and connected to the selected A/D channel during conversion
0 = CTMU is not connected to this channel

Note 1: These bits are unimplemented in 64-pin devices, read as '0'.

REGISTER 27-13: AD1CTMENL: A/D CTMU ENABLE REGISTER (LOW WORD)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CTMEN<15:0>:** CTMU Enabled During Conversion bits
1 = CTMU is enabled and connected to the selected A/D channel during conversion
0 = CTMU is not connected to this channel

REGISTER 33-6: FWDT: WATCHDOG TIMER CONFIGURATION WORD (CONTINUED)

bit 3-0 **WDTPS<3:0>:** Watchdog Timer Postscaler Select bits

1111 = 1:32,768
1110 = 1:16,384
1101 = 1:8,192
1100 = 1:4,096
1011 = 1:2,048
1010 = 1:1,024
1001 = 1:512
1000 = 1:256
0111 = 1:128
0110 = 1:64
0101 = 1:32
0100 = 1:16
0011 = 1:8
0010 = 1:4
0001 = 1:2
0000 = 1:1

REGISTER 33-13: DEVID: DEVICE ID REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R	R	R	R	R	R	R	R
FAMID7	FAMID6	FAMID5	FAMID4	FAMID3	FAMID2	FAMID1	FAMID0
bit 15							bit 8

R	R	R	R	R	R	R	R
DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0
bit 7							bit 0

Legend:	R = Readable bit	U = Unimplemented bit

bit 23-16 **Unimplemented:** Read as '1'

bit 15-8 **FAMID<7:0>:** Device Family Identifier bits

0110 0001 = PIC24FJ256GA412/GB412 Family

bit 7-0 **DEV<7:0>:** Individual Device Identifier bits

0000 0000 = PIC24FJ64GA406
0000 0001 = PIC24FJ64GA410
0000 0010 = PIC24FJ64GA412
0000 1000 = PIC24FJ128GA406
0000 1001 = PIC24FJ128GA410
0000 1010 = PIC24FJ128GA412
0001 0000 = PIC24FJ256GA406
0001 0001 = PIC24FJ256GA410
0001 0010 = PIC24FJ256GA412
0000 0100 = PIC24FJ64GB406
0000 0101 = PIC24FJ64GB410
0000 0110 = PIC24FJ64GB412
0000 1100 = PIC24FJ128GB406
0000 1101 = PIC24FJ128GB410
0000 1110 = PIC24FJ128GB412
0001 0100 = PIC24FJ256GB406
0001 0101 = PIC24FJ256GB410
0001 0110 = PIC24FJ256GB412

REGISTER 33-14: DEVREV: DEVICE REVISION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R	R	R	R
—	—	—	—	REV<3:0>			
bit 7							bit 0

Legend:	R = Readable bit	U = Unimplemented bit

bit 23-4 **Unimplemented:** Read as '0'

bit 3-0 **REV<3:0>:** Device Revision Identifier bits

TABLE 36-25: RESET AND BROWN-OUT RESET REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
SY10	TMCL	$\overline{\text{MCLR}}$ Pulse Width (Low)	2	—	—	μs	
SY12	TPOR	Power-on Reset Delay	—	2	—	μs	
SY13	TIOZ	I/O High-Impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	Lesser of: (3 TCY + 2) or 700	—	(3 TCY + 2)	μs	
SY25	TBOR	Brown-out Reset Pulse Width	1	—	—	μs	VDD ≤ VBOR
SY45	TRST	Internal State Reset Time	—	50	—	μs	
SY70	TDSWU	Deep Sleep Wake-up Time	—	200	—	μs	VCAP fully discharged before wake-up
SY71	TPM	Program Memory Wake-up Time	—	20	—	μs	Sleep wake-up with PMSLP = 0
			—	1	—	μs	Sleep wake-up with PMSLP = 1
SY72	TLVR	Low-Voltage Regulator Wake-up Time	—	90	—	μs	Sleep wake-up with PMSLP = 0
			—	70	—	μs	Sleep wake-up with PMSLP = 1

FIGURE 36-15: SPIx MODULE SLAVE MODE TIMING CHARACTERISTICS (CKE = 0)

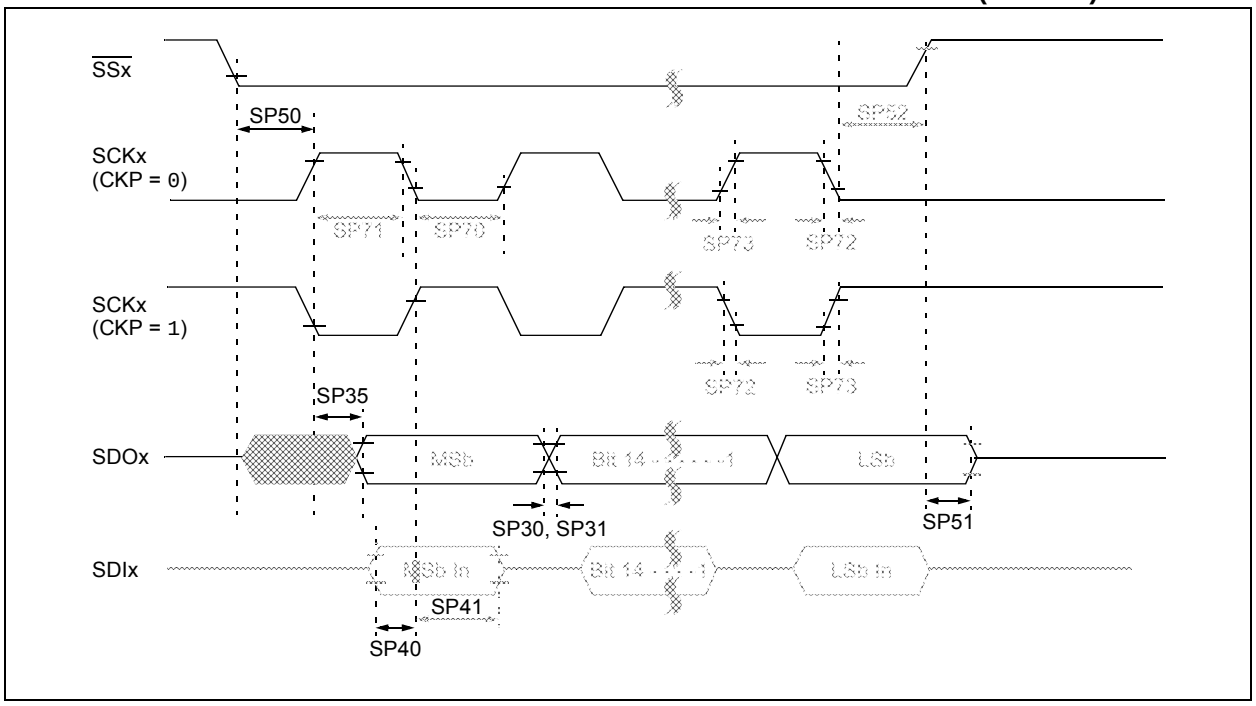


TABLE 36-36: SPIx MODULE SLAVE MODE TIMING REQUIREMENTS (CKE = 0)

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time	30	—	—	ns	
SP71	TscH	SCKx Input High Time	30	—	—	ns	
SP72	TscF	SCKx Input Fall Time(2)	—	10	25	ns	
SP73	TscR	SCKx Input Rise Time(2)	—	10	25	ns	
SP30	TdoF	SDOx Data Output Fall Time(2)	—	10	25	ns	
SP31	TdoR	SDOx Data Output Rise Time(2)	—	10	25	ns	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	—	30	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ to SCKx ↑ or SCKx Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	10	—	50	ns	
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ After SCKx Edge	1.5 TCY + 40	—	—	ns	

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Assumes 50 pF load on all SPIx pins.

FIGURE 36-16: SPIx MODULE SLAVE MODE TIMING CHARACTERISTICS (CKE = 1)

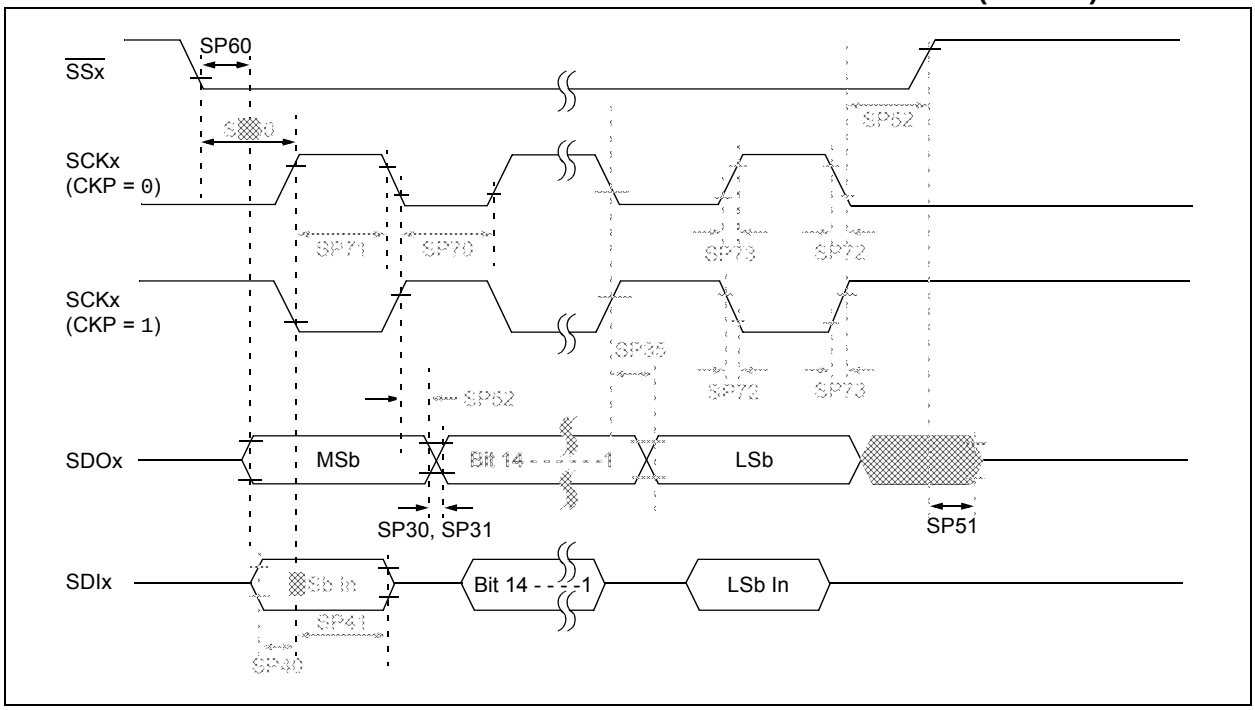


TABLE 36-37: SPIx MODULE SLAVE MODE TIMING REQUIREMENTS (CKE = 1)

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time	30	—	—	ns	
SP71	TscH	SCKx Input High Time	30	—	—	ns	
SP72	TscF	SCKx Input Fall Time(2)	—	10	25	ns	
SP73	TscR	SCKx Input Rise Time(2)	—	10	25	ns	
SP30	TdoF	SDOx Data Output Fall Time(2)	—	10	25	ns	
SP31	TdoR	SDOx Data Output Rise Time(2)	—	10	25	ns	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	—	30	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance(3)	10	—	50	ns	
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ After SCKx Edge	1.5 TCY + 40	—	—	ns	
SP60	TssL2doV	SDOx Data Output Valid After $\overline{SSx}$ Edge	—	—	50	ns	

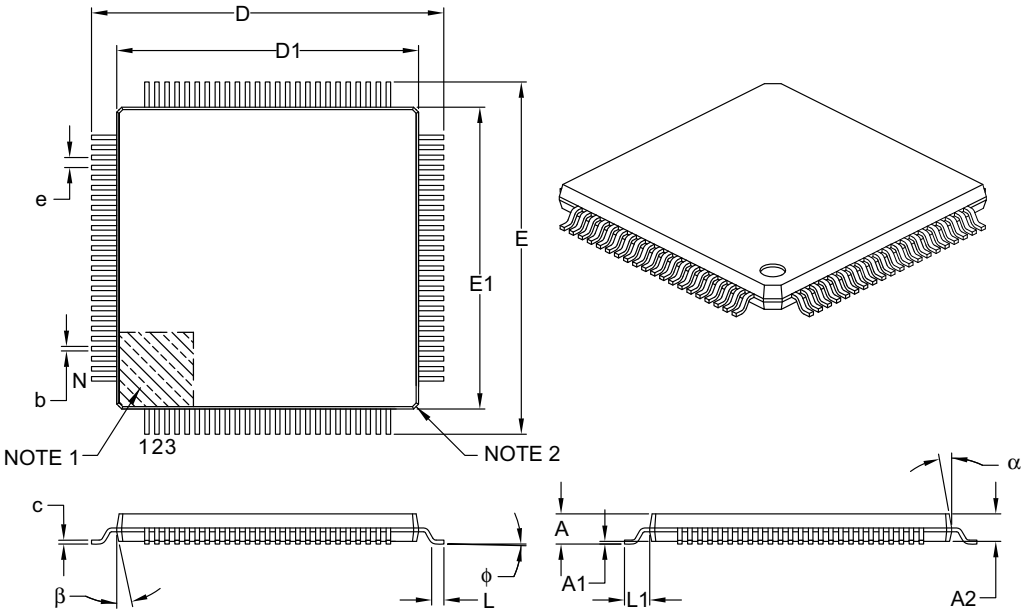
Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The minimum clock period for SCKx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

3: Assumes 50 pF load on all SPIx pins.

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		100	
Lead Pitch	e		0.40 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.13	0.18	0.23
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B