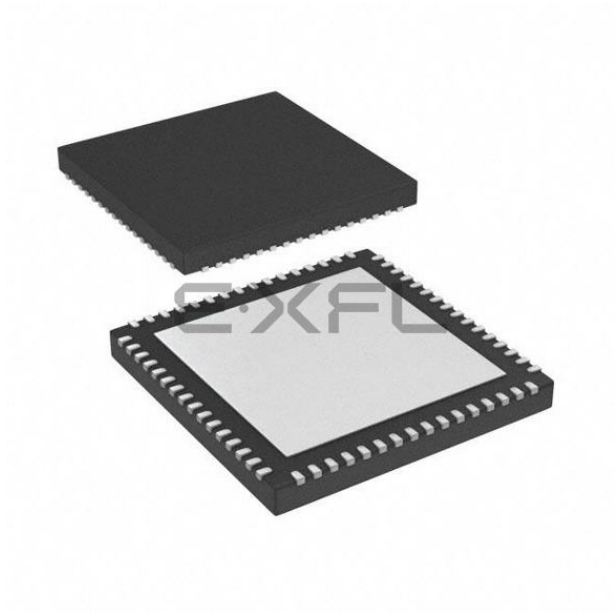
Microchip Technology - PIC24FJ64GB406-I/MR Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64gb406-i-mr

TABLE 1-5: PIC24FJ256GB412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
IOCC1	—	6	D1	I	ST	PORTC Interrupt-on-Change
IOCC2	—	7	E4	I	ST	
IOCC3	—	8	E2	I	ST	
IOCC4	—	9	E!	I	ST	
IOCC12	39	63	F9	I	ST	
IOCC13	47	73	C10	I	ST	
IOCC14	48	74	B11	I	ST	
IOCC15	40	64	F11	I	ST	
IOCD0	46	72	D9	I	ST	PORTD Interrupt-on-Change
IOCD1	49	76	A11	I	ST	
IOCD2	50	77	A10	I	ST	
IOCD3	51	78	B9	I	ST	
IOCD4	52	81	C8	I	ST	
IOCD5	53	82	B8	I	ST	
IOCD6	54	83	D7	I	ST	
IOCD7	55	84	C7	I	ST	
IOCD8	42	68	E9	I	ST	
IOCD9	43	69	E10	I	ST	
IOCD10	44	70	D11	I	ST	
IOCD11	45	71	C11	I	ST	
IOCD12	—	79	A9	I	ST	
IOCD13	—	80	D8	I	ST	
IOCD14	—	47	L9	I	ST	
IOCD15	—	48	K9	I	ST	
IOCE0	60	93	A4	I	ST	PORTE Interrupt-on-Change
IOCE1	61	94	B4	I	ST	
IOCE2	62	98	B3	I	ST	
IOCE3	63	99	A2	I	ST	
IOCE4	64	100	A1	I	ST	
IOCE5	1	3	D3	I	ST	
IOCE6	2	4	C1	I	ST	
IOCE7	3	5	D2	I	ST	
IOCE8	—	18	G1	I	ST	
IOCE9	—	19	G2	I	ST	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

TABLE 1-5: PIC24FJ256GB412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
PMRD/$\overline{\text{PMWR}}$	53	82	B8	I/O	DIG/ST/TTL	Parallel Master Port Read Strobe/Write Strobe
PMWR/PMENB	52	81	C8	I/O	DIG/ST/TTL	Parallel Master Port Write Strobe/Enable Strobe
PWRGT	21	32	K4	O	DIGMV	Real-Time Clock Power Control Output
PWRLCLK	48	74	B11	I	STMV	Real-Time Clock 50/60 Hz Clock Input
RA0	—	17	G3	I/O	DIG/ST	PORTA Digital I/Os
RA1	—	38	J6	I/O	DIG/ST	
RA2	—	58	H11	I/O	DIG/ST/TTL	
RA3	—	59	G10	I/O	DIG/ST/TTL	
RA4	—	60	G11	I/O	DIG/ST	
RA5	—	61	G9	I/O	DIG/ST	
RA6	—	91	C5	I/O	DIG/ST	
RA7	—	92	B5	I/O	DIG/ST	
RA9	—	28	L2	I/O	DIG/ST/TTL	
RA10	—	29	K3	I/O	DIG/ST	
RA14	—	66	E11	I/O	DIG/ST/TTL	
RA15	—	67	E8	I/O	DIG/ST/TTL	
RB0	16	25	K2	I/O	DIG/ST	PORTB Digital I/Os
RB1	15	24	K1	I/O	DIG/ST	
RB2	14	23	J2	I/O	DIG/ST/TTL	
RB3	13	22	J1	I/O	DIG/ST/TTL	
RB4	12	21	H2	I/O	DIG/ST/TTL	
RB5	11	20	H1	I/O	DIG/ST/TTL	
RB6	17	26	L1	I/O	DIG/ST	
RB7	18	27	J3	I/O	DIG/ST/TTL	
RB8	21	32	K4	I/O	DIG/ST	
RB9	22	33	L4	I/O	DIG/ST	
RB10	23	34	H5	I/O	DIG/ST	
RB11	24	35	K5	I/O	DIG/ST	
RB12	27	41	J7	I/O	DIG/ST	
RB13	28	42	L7	I/O	DIG/ST	
RB14	29	43	K7	I/O	DIG/ST	
RB15	30	44	L8	I/O	DIG/ST	
RC1	—	6	D1	I/O	DIG/ST	PORTC Digital I/Os
RC2	—	7	E4	I/O	DIG/ST	
RC3	—	8	E2	I/O	DIG/ST	
RC4	—	9	E!	I/O	DIG/ST	
RC12	39	63	F9	I/O	DIG/ST	
RC13	47	73	C10	I	ST	
RC14	48	74	B11	I	ST	
RC15	40	64	F11	I/O	DIG/ST	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

TABLE 1-5: PIC24FJ256GB412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
RD0	46	72	D9	I/O	DIG/ST	PORTD Digital I/Os
RD1	49	76	A11	I/O	DIG/ST	
RD2	50	77	A10	I/O	DIG/ST	
RD3	51	78	B9	I/O	DIG/ST	
RD4	52	81	C8	I/O	DIG/ST	
RD5	53	82	B8	I/O	DIG/ST	
RD6	54	83	D7	I/O	DIG/ST	
RD7	55	84	C7	I/O	DIG/ST	
RD8	42	68	E9	I/O	DIG/ST	
RD9	43	69	E10	I/O	DIG/ST	
RD10	44	70	D11	I/O	DIG/ST	
RD11	45	71	C11	I/O	DIG/ST	
RD12	—	79	A9	I/O	DIG/ST	
RD13	—	80	D8	I/O	DIG/ST	
RD14	—	47	L9	I/O	DIG/ST	
RD15	—	48	K9	I/O	DIG/ST	
RE0	60	93	A4	I/O	DIG/ST	PORTE Digital I/Os
RE1	61	94	B4	I/O	DIG/ST	
RE2	62	98	B3	I/O	DIG/ST	
RE3	63	99	A2	I/O	DIG/ST	
RE4	64	100	A1	I/O	DIG/ST	
RE5	1	3	D3	I/O	DIG/ST	
RE6	2	4	C1	I/O	DIG/ST	
RE7	3	5	D2	I/O	DIG/ST	
RE8	—	18	G1	I/O	DIG/ST	
RE9	—	19	G2	I/O	DIG/ST	
REFI1	24	35	K5	I	ST	Reference Clock Input
RF0	58	87	B6	I/O	DIG/ST	PORTF Digital I/Os
RF1	59	88	A6	I/O	DIG/ST	
RF2	—	52	K11	I/O	DIG/ST	
RF3	33	51	K10	I/O	DIG/ST/TTL	
RF4	31	49	L10	I/O	DIG/ST	
RF5	32	50	L11	I/O	DIG/ST	
RF6	—	—	—	I/O	DIG/ST	
RF7	34	54	H8	I/O	DIG/ST	
RF8	—	53	J10	I/O	DIG/ST	
RF12	—	40	K6	I/O	DIG/ST	
RF13	—	39	L6	I/O	DIG/ST	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

4.0 MEMORY ORGANIZATION

As Harvard architecture devices, PIC24F microcontrollers feature separate program and data memory spaces and buses. This architecture also allows direct access of program memory from the Data Space (DS) during code execution.

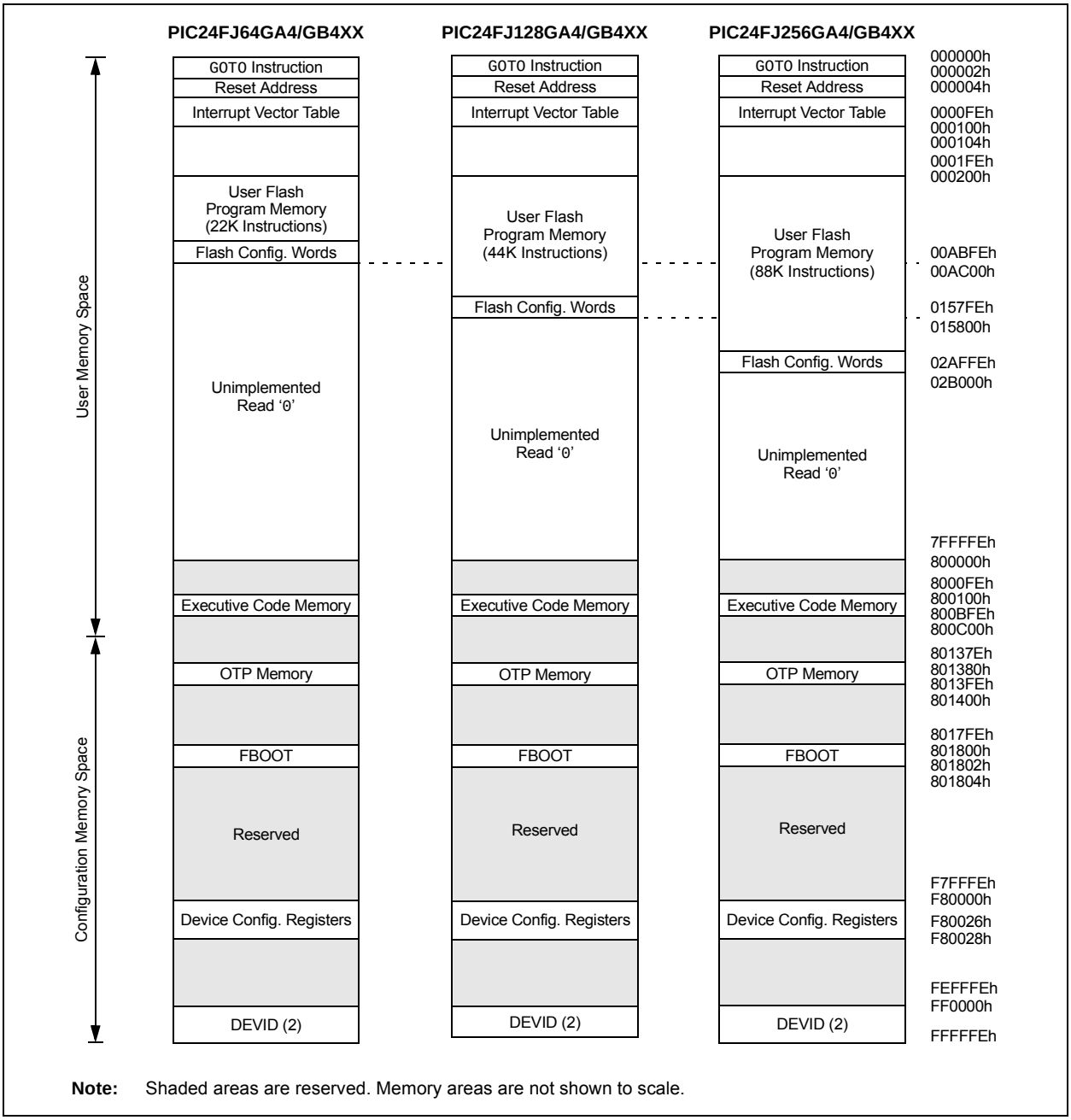
4.1 Program Memory Space

The program address memory space of the PIC24FJ256GA412/GB412 family devices is 4M instructions. The space is addressable by a 24-bit value derived from either the 23-bit Program Counter (PC) during program execution, or from table operation or Data Space remapping, as described in **Section 4.4 "Interfacing Program and Data Memory Spaces"**.

User access to the program memory space is restricted to the lower half of the address range (000000h to 7FFFFFh). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

Memory maps for PIC24FJ256GA412/GB412 family devices are shown in Figure 4-1.

FIGURE 4-1: DEFAULT PROGRAM MEMORY MAPS FOR PIC24FJ256GA412/GB412 FAMILY



Note: Shaded areas are reserved. Memory areas are not shown to scale.

TABLE 4-5: SFR BLOCK 000h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
Core			**Interrupt Controller**			IPC7	0B6	0100010001000100
WREG0	000	0000000000000000	INTCON1	080	0000000000000000	IPC8	0B8	0100010001000100
WREG1	002	0000000000000000	INTCON2	082	1000000000000000	IPC9	0BA	0100010001000100
WREG2	004	0000000000000000	INTCON4	086	0000000000000000	IPC10	0BC	0100010001000100
WREG3	006	0000000000000000	IFS0	088	0000000000000000	IPC11	0BE	0100010001000100
WREG4	008	0000000000000000	IFS1	08A	0000000000000000	IPC12	0C0	0100010001000100
WREG5	00A	0000000000000000	IFS2	08C	0000000000000000	IPC13	0C2	0100010001000000
WREG6	00C	0000000000000000	IFS3	08E	0000000000000000	IPC14	0C4	0100010001000100
WREG7	00E	0000000000000000	IFS4	090	0000000000000000	IPC15	0C6	0100010001000100
WREG8	010	0000000000000000	IFS5	092	0000000000000000	IPC16	0C8	0100010001000100
WREG9	012	0000000000000000	IFS6	094	0000000000000000	IPC17	0CA	0100010000000000
WREG10	014	0000000000000000	IFS7	096	0000000000000000	IPC18	0CC	0000000001000100
WREG11	016	0000000000000000	IEC0	098	0000000000000000	IPC19	0CE	0000010001000000
WREG12	018	0000000000000000	IEC1	09A	0000000000000000	IPC20	0D0	0100010001000000
WREG13	01A	0000000000000000	IEC2	09C	0000000000000000	IPC21	0D2	0100010001000100
WREG14	01C	0000000000000000	IEC3	09E	0000000000000000	IPC22	0D4	0100010001000100
WREG15	01E	0000000000000000	IEC4	0A0	0000000000000000	IPC23	0D6	0100010001000100
SPLIM	020	xxxxxxxxxxxxxxx0	IEC5	0A2	0000000000000000	IPC24	0D8	0100010001000100
PCL	02E	0000000000000000	IEC6	0A4	0000000000000000	IPC25	0DA	0000010001000100
PCH	030	0000000000000000	IEC7	0A6	0000000000000000	IPC26	0DC	0000010000000000
DSRPAG	032	0000000000000000	IPC0	0A8	0100010001000100	IPC27	0DE	0100010001000000
DSWPAG	034	0000000000000000	IPC1	0AA	0100010001000100	IPC28	0E0	0100010001000100
RCOUNT	036	xxxxxxxxxxxxxxxx	IPC2	0AC	0100010001000100	IPC29	0E2	0000000001000100
SR	042	0000000000000000	IPC3	0AE	0100010001000100	INTTREG	0E4	0000000000000000
CORCON	044	0000000000000100	IPC4	0B0	0100010001000100			
DISICNT	052	00xxxxxxxxxxxxxx	IPC5	0B2	0100010000000100			
TBLPAG	054	0000000000000000	IPC6	0B4	0100010001000100			

Legend: x = unknown or indeterminate value. Reset and address values are in hexadecimal.

REGISTER 5-1: DMACON: DMA ENGINE CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
DMAEN	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PRSSEL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **DMAEN:** DMA Module Enable bit
1 = Enables module
0 = Disables module and terminates all active DMA operation(s)

bit 14-1 **Unimplemented:** Read as '0'

bit 0 **PRSSEL:** Channel Priority Scheme Selection bit
1 = Round robin scheme
0 = Fixed priority scheme

TABLE 8-2: IMPLEMENTED INTERRUPT VECTORS

Interrupt Source	Vector Number	IRQ #	IVT Address	Interrupt Bit Locations		
				Flag	Enable	Priority
ADC1 Interrupt	21	13	00002Eh	IFS0<13>	IEC0<13>	IPC3<6:4>
CLC1	104	96	0000D4h	IFS6<0>	IEC6<0>	IPC24<2:0>
CLC2	105	97	0000D6h	IFS6<1>	IEC6<1>	IPC24<6:4>
CLC3	106	98	0000D8h	IFS6<2>	IEC6<2>	IPC24<10:8>
CLC4	107	99	0000DAh	IFS6<3>	IEC6<3>	IPC24<14:12>
Comparator Event	26	18	000038h	IFS1<2>	IEC1<2>	IPC4<10:8>
CRC Generator	75	67	00009Ah	IFS4<3>	IEC4<3>	IPC16<14:12>
Crypto Buffer Ready	42	34	000058h	IFS2<2>	IEC2<2>	IPC8<10:8>
Crypto Operation Done	63	55	000082h	IFS3<7>	IEC3<7>	IPC13<14:12>
Crypto Key Store Program Done	64	56	000084h	IFS3<8>	IEC3<8>	IPC14<2:0>
Crypto Rollover	43	35	00005Ah	IFS2<3>	IEC2<3>	IPC8<14:12>
CTMU Event	85	77	0000AEh	IFS4<13>	IEC4<13>	IPC19<6:4>
DAC	86	78	0000B0h	IFS4<14>	IEC4<14>	IPC19<10:8>
DMA Channel 0	12	4	00001Ch	IFS0<4>	IEC0<4>	IPC1<2:0>
DMA Channel 1	22	14	000030h	IFS0<14>	IEC0<14>	IPC3<10:8>
DMA Channel 2	32	24	000044h	IFS1<8>	IEC1<8>	IPC6<2:0>
DMA Channel 3	44	36	00005Ch	IFS2<4>	IEC2<4>	IPC9<2:0>
DMA Channel 4	54	46	000070h	IFS2<14>	IEC2<14>	IPC11<10:8>
DMA Channel 5	69	61	00008Eh	IFS3<13>	IEC3<13>	IPC15<6:4>
Enhanced Parallel Master Port (EPMP)	53	45	00006Eh	IFS2<13>	IEC2<13>	IPC11<6:4>
External Interrupt 0	8	0	000014h	IFS0<0>	IEC0<0>	IPC0<2:0>
External Interrupt 1	28	20	00003Ch	IFS1<4>	IEC1<4>	IPC5<2:0>
External Interrupt 2	37	29	00004Eh	IFS1<13>	IEC1<13>	IPC7<6:4>
External Interrupt 3	61	53	00007Eh	IFS3<5>	IEC3<5>	IPC13<6:4>
External Interrupt 4	62	54	000080h	IFS3<6>	IEC3<6>	IPC13<10:8>
Flash Write/Program Done	23	15	000032h	IFS0<15>	IEC0<15>	IPC3<14:12>
FRC Self-Tune	114	106	0000E8h	IFS6<10>	IEC6<10>	IPC26<10:8>
High/Low-Voltage Detect (HLVD)	80	72	0000A4h	IFS4<8>	IEC4<8>	IPC18<2:0>
I2C1 Bus Collision	92	84	0000BCh	IFS5<4>	IEC5<4>	IPC21<2:0>
I2C1 Master Event	25	17	000036h	IFS1<1>	IEC1<1>	IPC4<6:4>
I2C1 Slave Event	24	16	000034h	IFS1<0>	IEC1<0>	IPC4<2:0>
I2C2 Bus Collision	93	85	0000BEh	IFS5<5>	IEC5<5>	IPC21<6:4>
I2C2 Master Event	58	50	000078h	IFS3<2>	IEC3<2>	IPC12<10:8>
I2C2 Slave Event	57	49	000076h	IFS3<1>	IEC3<1>	IPC12<6:4>
I2C3 Master Event	79	71	0000A2h	IFS4<7>	IEC4<7>	IPC17<14:12>
I2C3 Slave Event	78	70	0000A0h	IFS4<6>	IEC4<6>	IPC17<10:8>
IC23 Collision	117	109	0000EEh	IFS6<13>	IEC6<13>	IPC27<6:4>
Input Capture 1	9	1	000016h	IFS0<1>	IEC0<1>	IPC0<6:4>
Input Capture 2	13	5	00001Eh	IFS0<5>	IEC0<5>	IPC1<6:4>
Input Capture 3	45	37	00005Eh	IFS2<5>	IEC2<5>	IPC9<6:4>
Input Capture 4	46	38	000060h	IFS2<6>	IEC2<6>	IPC9<10:8>
Input Capture 5	47	39	000062h	IFS2<7>	IEC2<7>	IPC9<14:12>
Input Capture 6	48	40	000064h	IFS2<8>	IEC2<8>	IPC10<2:0>
Interrupt-on-Change (IOC)	27	19	00003Ah	IFS1<3>	IEC1<3>	IPC4<14:12>
JTAG	125	117	0000FEh	IFS7<5>	IEC7<5>	IPC29<6:4>
LCD	108	100	0000DCh	IFS6<4>	IEC6<4>	IPC25<2:0>

REGISTER 9-4: REFOCONL: REFERENCE CLOCK CONTROL LOW REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HSC
ROEN	—	ROSIDL	ROOUT	ROSLP	—	ROSWEN	ROACTIV
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	ROSEL3	ROSEL2	ROSEL1	ROSEL0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROEN:** Reference Clock Enable bit
1 = Reference Oscillator is enabled on the REFO pin
0 = Reference Oscillator is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSIDL:** Reference Clock Stop in Idle bit
1 = Reference Oscillator continues to run in Idle mode
0 = Reference Oscillator is disabled in Idle mode

bit 12 **ROOUT:** Reference Clock Output Enable bit
1 = Reference clock external output is enabled and available on the REFO pin
0 = Reference clock external output is disabled

bit 11 **ROSLP:** Reference Clock Stop in Sleep bit
1 = Reference Oscillator continues to run in Sleep modes
0 = Reference Oscillator is disabled in Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **ROSWEN:** Reference Clock Output Enable bit
1 = Clock divider change (requested by changes to ROTRIMx and/or RODIVx) is requested or is in progress (set in software, cleared by hardware upon completion)
0 = Clock divider change has completed or is not pending

bit 8 **ROACTIV:** Reference Clock Status bit
1 = Reference clock is active; do not change clock source
0 = Reference clock is stopped; clock source and configuration may be safely changed

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **ROSEL<3:0>:** Reference Clock Source Select bits
1111 =
• • • = Reserved
1001 =
1000 = REFI pin
0111 = Reserved
0110 = PLL block (Fixed PLL output frequency or 96 MHz PLL output)
0101 = Secondary Oscillator
0100 = LPRC
0011 = FRC
0010 = Primary Oscillator
0001 = Peripheral clock (FCY)
0000 = CPU clock

NOTES:

REGISTER 10-6: PMD3: PERIPHERAL MODULE DISABLE REGISTER 3

U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0
—	—	—	—	—	CMPMD	—	PMMD
bit 15							bit 8

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0
CRCMD	DACMD	—	—	U3MD	I2C3MD	I2C2MD	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **CMPMD:** Triple Comparator Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 9 **Unimplemented:** Read as '0'

bit 8 **PMMD:** Enhanced Parallel Master Port Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 7 **CRCMD:** CRC Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 6 **DACMD:** DAC Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **U3MD:** UART3 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 2 **I2C3MD:** I2C3 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 1 **I2C2MD:** I2C2 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 0 **Unimplemented:** Read as '0'

14.4 Input Capture Mode

Input Capture mode is used to capture a timer value from an independent timer base upon an event on an input pin or other internal trigger source. The input capture features are useful in applications requiring frequency (time period) and pulse measurement. Figure 14-6 depicts a simplified block diagram of Input Capture mode.

Input Capture mode uses a dedicated 16/32-bit, synchronous, up counting timer for the capture function. The timer value is written to the FIFO when a capture event occurs. The internal value may be read (with a synchronization delay) using the CCPxTMRH/L register.

To use Input Capture mode, the CCSEL bit (CCPxCON1L<4>) must be set. The T32 and the MOD<3:0> bits are used to select the proper Capture mode, as shown in Table 14-3.

TABLE 14-3: INPUT CAPTURE MODES

MOD<3:0> (CCPxCON1L<3:0>)	T32 (CCPxCON1L<5>)	Operating Mode
0000	0	Edge Detect (16-bit capture)
0000	1	Edge Detect (32-bit capture)
0001	0	Every Rising (16-bit capture)
0001	1	Every Rising (32-bit capture)
0010	0	Every Falling (16-bit capture)
0010	1	Every Falling (32-bit capture)
0011	0	Every Rise/Fall (16-bit capture)
0011	1	Every Rise/Fall (32-bit capture)
0100	0	Every 4th Rising (16-bit capture)
0100	1	Every 4th Rising (32-bit capture)
0101	0	Every 16th Rising (16-bit capture)
0101	1	Every 16th Rising (32-bit capture)

FIGURE 14-6: INPUT CAPTURE x BLOCK DIAGRAM

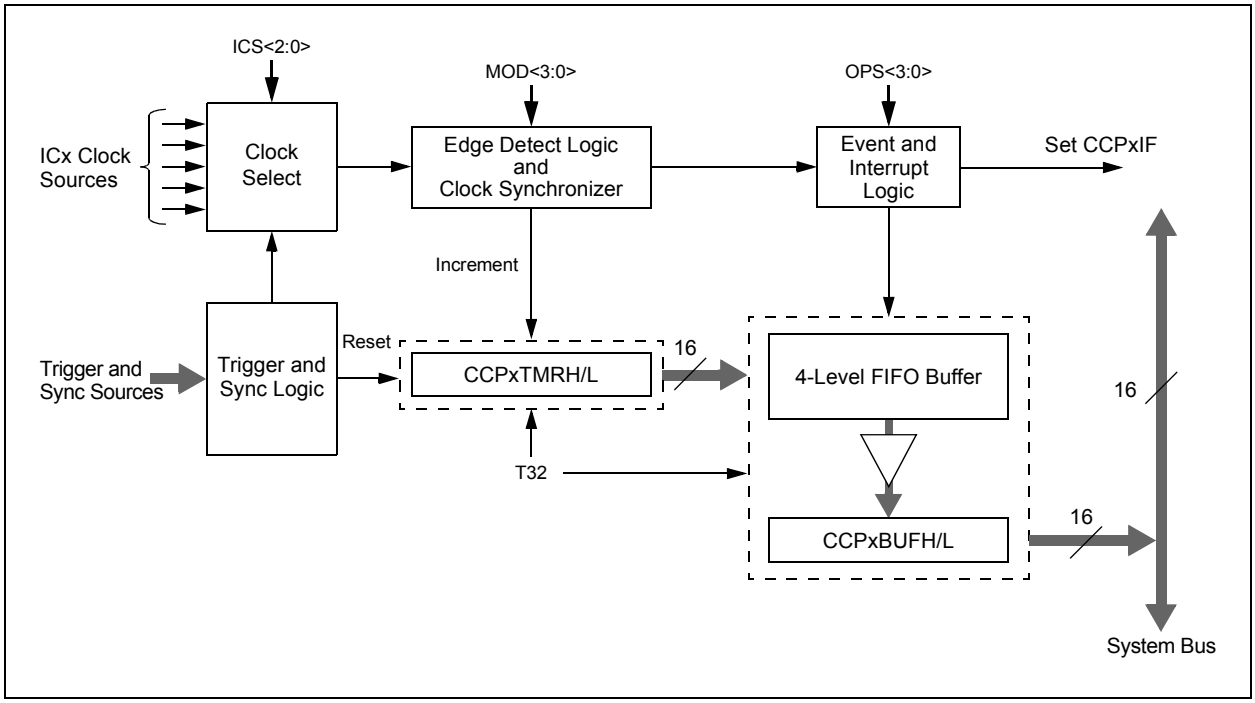
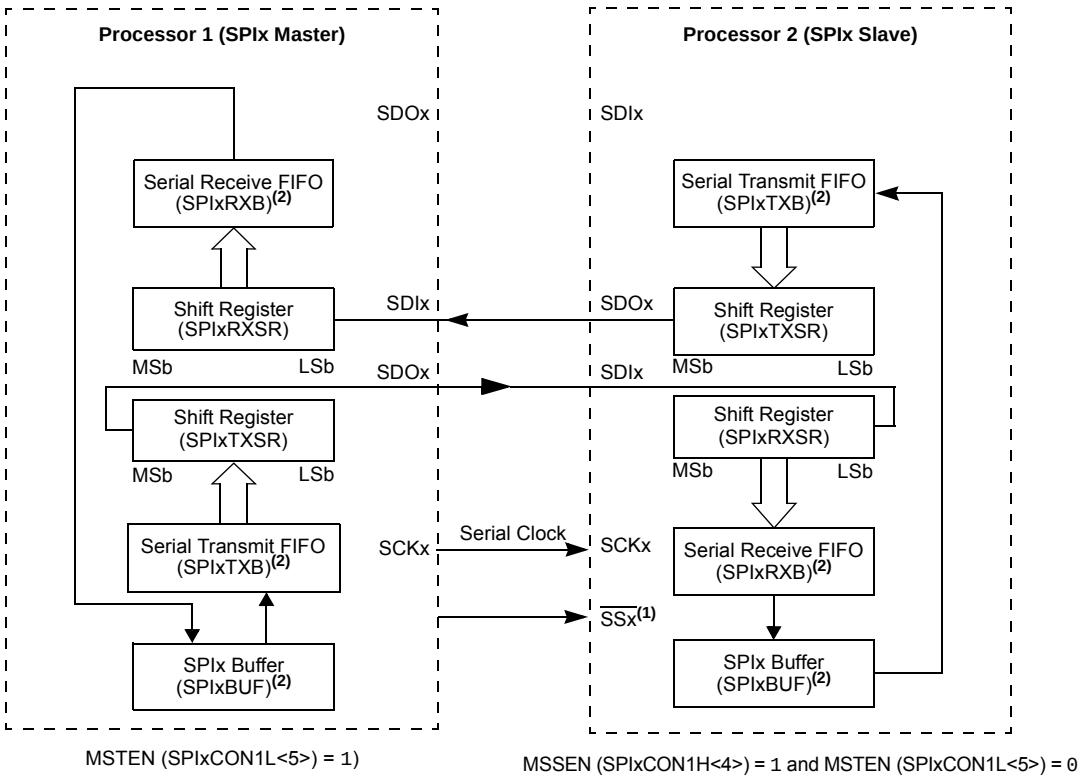


FIGURE 17-4: SPIx MASTER/SLAVE CONNECTION (ENHANCED BUFFER MODES)



Note 1: Using the $\overline{SSx}$ pin in Slave mode of operation is optional.

2: User must write transmit data to read the received data from SPIxBUF. The SPIxTXB and SPIxRXB registers are memory-mapped to SPIxBUF.

FIGURE 17-5: SPIx MASTER, FRAME MASTER CONNECTION DIAGRAM

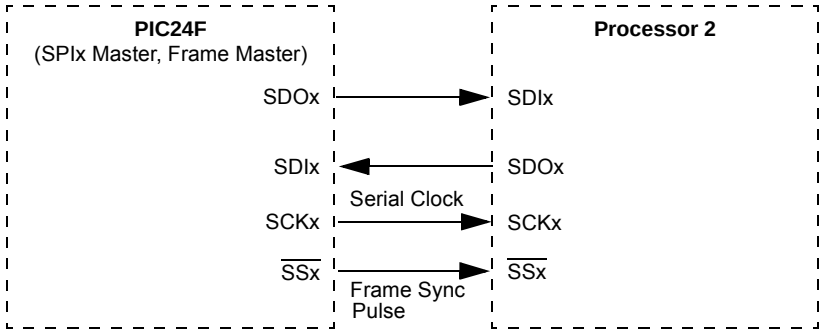
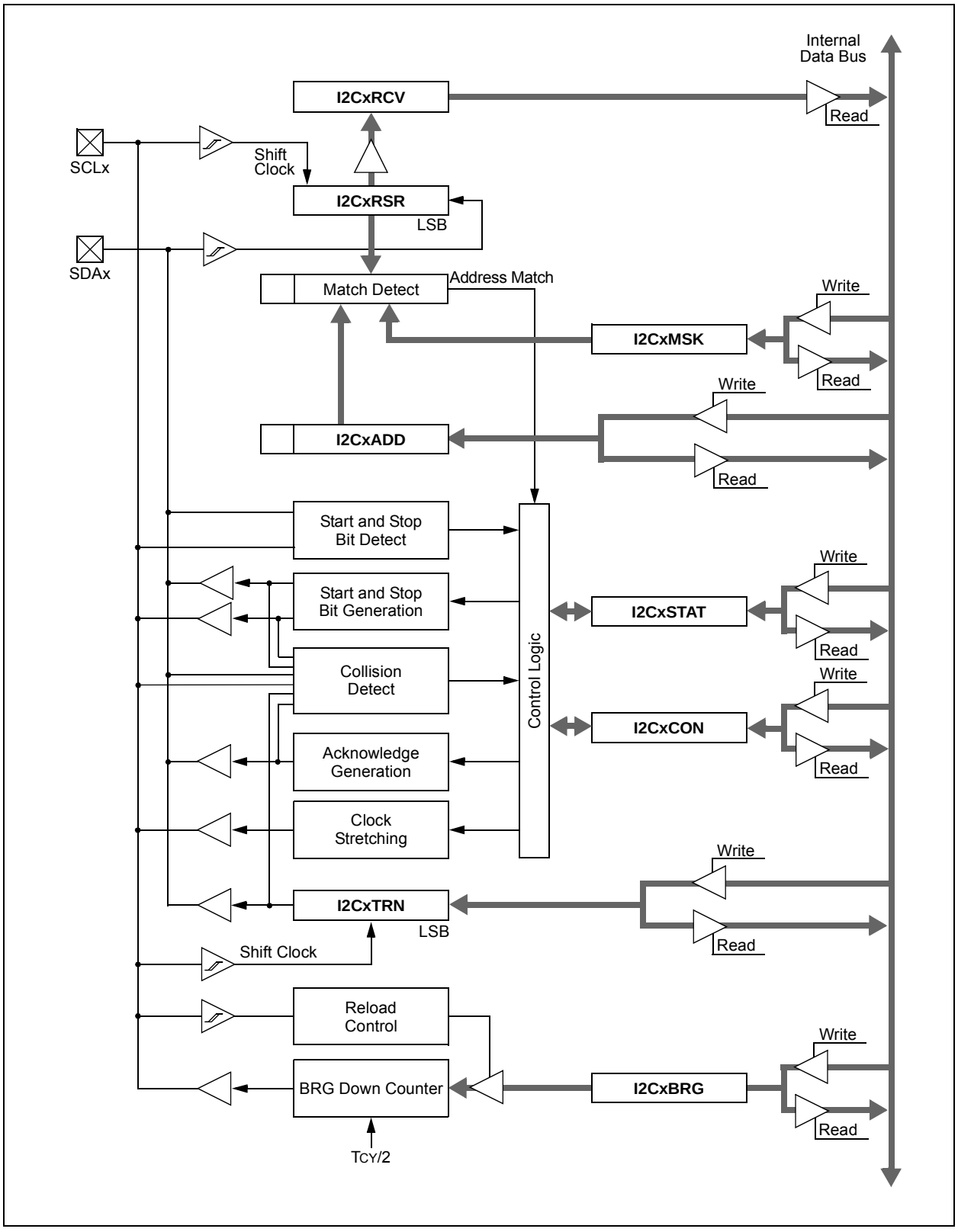


FIGURE 18-1: I2Cx BLOCK DIAGRAM



REGISTER 18-1: I2CxCONL: I2Cx CONTROL REGISTER LOW (CONTINUED)

bit 7 **GCEN:** General Call Enable bit (I^2C Slave mode only)
1 = Enables interrupt when a general call address is received in I2CxRSR; module is enabled for reception
0 = General call address is disabled.

bit 6 **STREN:** SCLx Clock Stretch Enable bit
In I^2C Slave mode only; used in conjunction with the SCKREL bit.
1 = Enables clock stretching
0 = Disables clock stretching

bit 5 **ACKDT:** Acknowledge Data bit
In I^2C Master mode during Master Receive mode. The value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
In I^2C Slave mode when AHEN = 1 or DHEN = 1. The value that the slave will transmit when it initiates an Acknowledge sequence at the end of an address or data reception.
1 = NACK is sent
0 = ACK is sent

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
In I^2C Master mode only; applicable during Master Receive mode.
1 = Initiates Acknowledge sequence on SDAx and SCLx pins, and transmits ACKDT data bit
0 = Acknowledge sequence is Idle

bit 3 **RCEN:** Receive Enable bit (I^2C Master mode only)
1 = Enables Receive mode for I^2C; automatically cleared by hardware at end of 8-bit receive data byte
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (I^2C Master mode only)
1 = Initiates Stop condition on SDAx and SCLx pins
0 = Stop condition is Idle

bit 1 **RSEN:** Restart Condition Enable bit (I^2C Master mode only)
1 = Initiates Restart condition on SDAx and SCLx pins
0 = Restart condition is Idle

bit 0 **SEN:** Start Condition Enable bit (I^2C Master mode only)
1 = Initiates Start condition on SDAx and SCLx pins
0 = Start condition is Idle

Note 1: Automatically cleared to '0' at the beginning of slave transmission; automatically cleared to '0' at the end of slave reception.

2: Automatically cleared to '0' at the beginning of slave transmission.

19.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582). The information in this data sheet supersedes the information in the FRM.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the PIC24F device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins. The UART module includes IrDA® encoder/decoder unit.

The PIC24FJ256GA412/GB412 family devices are equipped with six UART modules, referred to as UART1 through UART6.

The primary features of the UARTx modules are:

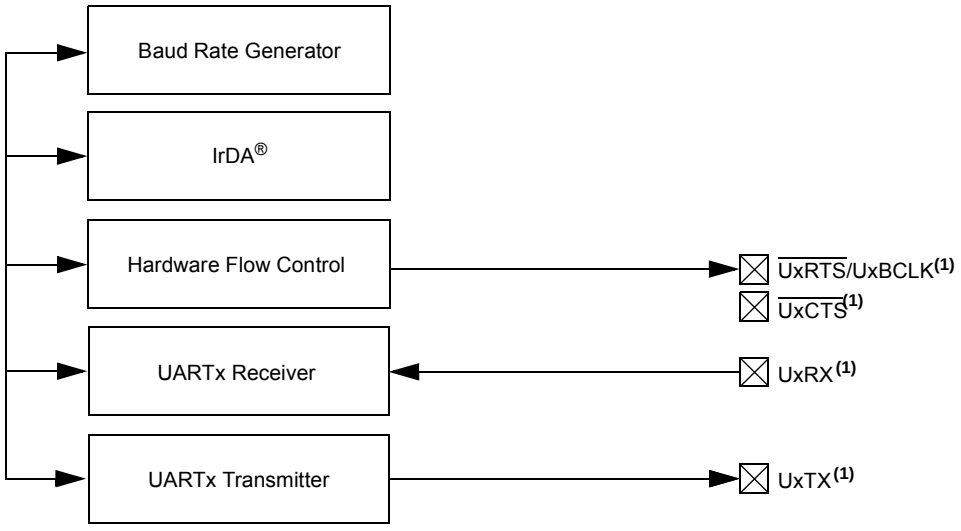
- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Range from up to 2.5 Mbps and Down to 38 Hz at 40 MIPS in 16x Mode
- Baud Rates Range from up to 10 Mbps and Down to 152 Hz at 40 MIPS in 4x Mode
- 4-Deep, First-In-First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-Bit Mode with Address Detect (9^{th} bit = 1)
- Separate Transmit and Receive Interrupts
- Loopback Mode for Diagnostic Support
- Polarity Control for Transmit and Receive Lines
- Support for Sync and Break Characters
- Supports Automatic Baud Rate Detection
- IrDA® Encoder and Decoder Logic
- Includes DMA Support
- 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UARTx module is shown in Figure 19-1. The UARTx module consists of these key important hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

Note: Throughout this section, references to register and bit names that may be associated with a specific UART module are referred to generically by the use of 'x' in place of the specific module number. Thus, "UxSTAL" might refer to the Status Low register for either UART1, UART2, UART3 or UART4.

FIGURE 19-1: UARTx SIMPLIFIED BLOCK DIAGRAM



Note 1: For UARTs that use Peripheral Pin Select (PPS), their inputs and outputs must all be assigned to available RPn/RPIn pins before use. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

REGISTER 22-6: LCDREF: LCD REFERENCE LADDER CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LCDIRE	—	LCDCST2	LCDCST1	LCDCST0	VLCD3PE	VLCD2PE	VLCD1PE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
LRLAP1	LRLAP0	LRLBP1	LRLBP0	—	LRLAT2	LRLAT1	LRLAT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **LCDIRE**: LCD Internal Reference Enable bit
1 = Internal LCD reference is enabled and connected to the internal contrast control circuit
0 = Internal LCD reference is disabled

bit 14 **Unimplemented**: Read as '0'

bit 13-11 **LCDCST<2:0>**: LCD Contrast Control bits
Selects the Resistance of the LCD Contrast Control Resistor Ladder:
111 = Resistor ladder is at maximum resistance (minimum contrast)
110 = Resistor ladder is at 6/7th of maximum resistance
101 = Resistor ladder is at 5/7th of maximum resistance
100 = Resistor ladder is at 4/7th of maximum resistance
011 = Resistor ladder is at 3/7th of maximum resistance
010 = Resistor ladder is at 2/7th of maximum resistance
001 = Resistor ladder is at 1/7th of maximum resistance
000 = Minimum resistance (maximum contrast); resistor ladder is shorted

bit 10 **VLCD3PE**: LCD Bias 3 Pin Enable bit
1 = Bias 3 level is connected to the external pin, LCDBIAS3
0 = Bias 3 level is internal (internal resistor ladder)

bit 9 **VLCD2PE**: LCD Bias 2 Pin Enable bit
1 = Bias 2 level is connected to the external pin, LCDBIAS2
0 = Bias 2 level is internal (internal resistor ladder)

bit 8 **VLCD1PE**: LCD Bias 1 Pin Enable bit
1 = Bias 1 level is connected to the external pin, LCDBIAS1
0 = Bias 1 level is internal (internal resistor ladder)

bit 7-6 **LRLAP<1:0>**: LCD Reference Ladder A Time Power Control bits
During Time Interval A:
11 = Internal LCD reference ladder is powered in High-Power mode
10 = Internal LCD reference ladder is powered in Medium Power mode
01 = Internal LCD reference ladder is powered in Low-Power mode
00 = Internal LCD reference ladder is powered down and unconnected

bit 5-4 **LRLBP<1:0>**: LCD Reference Ladder B Time Power Control bits
During Time Interval B:
11 = Internal LCD reference ladder is powered in High-Power mode
10 = Internal LCD reference ladder is powered in Medium Power mode
01 = Internal LCD reference ladder is powered in Low-Power mode
00 = Internal LCD reference ladder is powered down and unconnected

bit 3 **Unimplemented**: Read as '0'

REGISTER 23-5: CLCxGLSH: CLCx GATE LOGIC INPUT SELECT HIGH REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **G4D4T:** Gate 4 Data Source 4 True Enable bit
1 = Data Source 4 inverted signal is enabled for Gate 4
0 = Data Source 4 inverted signal is disabled for Gate 4

bit 14 **G4D4N:** Gate 4 Data Source 4 Negated Enable bit
1 = Data Source 4 inverted signal is enabled for Gate 4
0 = Data Source 4 inverted signal is disabled for Gate 4

bit 13 **G4D3T:** Gate 4 Data Source 3 True Enable bit
1 = Data Source 3 inverted signal is enabled for Gate 4
0 = Data Source 3 inverted signal is disabled for Gate 4

bit 12 **G4D3N:** Gate 4 Data Source 3 Negated Enable bit
1 = Data Source 3 inverted signal is enabled for Gate 4
0 = Data Source 3 inverted signal is disabled for Gate 4

bit 11 **G4D2T:** Gate 4 Data Source 2 True Enable bit
1 = Data Source 2 inverted signal is enabled for Gate 4
0 = Data Source 2 inverted signal is disabled for Gate 4

bit 10 **G4D2N:** Gate 4 Data Source 2 Negated Enable bit
1 = Data Source 2 inverted signal is enabled for Gate 4
0 = Data Source 2 inverted signal is disabled for Gate 4

bit 9 **G4D1T:** Gate 4 Data Source 1 True Enable bit
1 = Data Source 1 inverted signal is enabled for Gate 4
0 = Data Source 1 inverted signal is disabled for Gate 4

bit 8 **G4D1N:** Gate 4 Data Source 1 Negated Enable bit
1 = Data Source 1 inverted signal is enabled for Gate 4
0 = Data Source 1 inverted signal is disabled for Gate 4

bit 7 **G3D4T:** Gate 3 Data Source 4 True Enable bit
1 = Data Source 4 inverted signal is enabled for Gate 3
0 = Data Source 4 inverted signal is disabled for Gate 3

bit 6 **G3D4N:** Gate 3 Data Source 4 Negated Enable bit
1 = Data Source 4 inverted signal is enabled for Gate 3
0 = Data Source 4 inverted signal is disabled for Gate 3

bit 5 **G3D3T:** Gate 3 Data Source 3 True Enable bit
1 = Data Source 3 inverted signal is enabled for Gate 3
0 = Data Source 3 inverted signal is disabled for Gate 3

bit 4 **G3D3N:** Gate 3 Data Source 3 Negated Enable bit
1 = Data Source 3 inverted signal is enabled for Gate 3
0 = Data Source 3 inverted signal is disabled for Gate 3

24.5.3 TIME/ALARM/TIMESTAMP VALUE REGISTERS

REGISTER 24-7: TIMEL/ALMTIMEL/TSATIMEL/TSBTIMEL: TIME REGISTER (LOW)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **SECTEN<2:0>:** Binary Coded Decimal Value of Seconds ‘10’ Digit bits
Contains a value from 0 to 5.

bit 11-8 **SECONE<3:0>:** Binary Coded Decimal Value of Seconds ‘1’ Digit bits
Contains a value from 0 to 9.

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 24-8: TIMEH/ALMTIMEH/TSATIMEH/TSBTIMEH: TIME REGISTER (HIGH)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-12 **HRTEN<1:0>:** Binary Coded Decimal Value of Hours ‘10’ Digit bits
Contains a value from 0 to 2.

bit 11-8 **HRONE<3:0>:** Binary Coded Decimal Value of Hours ‘1’ Digit bits
Contains a value from 0 to 9.

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **MINTEN<2:0>:** Binary Coded Decimal Value of Minutes ‘10’ Digit bits
Contains a value from 0 to 5.

bit 3-0 **MINONE<3:0>:** Binary Coded Decimal Value of Minutes ‘1’ Digit bits
Contains a value from 0 to 9.

REGISTER 33-6: FWDT: WATCHDOG TIMER CONFIGURATION WORD

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	R/PO-1	R/PO-1	U-1	R/PO-1	U-1	R/PO-1	R/PO-1
—	WDTCLK1	WDTCLK0	—	WDTCMX	—	WDTWIN1	WDTWIN0
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
WINDIS	FWDTEN1	FWDTEN0	FWPSA	WDTPS3	WDTPS2	WDTPS1	WDTPS0
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-15 **Unimplemented:** Read as '1'

bit 14-13 **WDTCLK<1:0>:** WDT Clock Source Select bits

When WDTCMX = 1:

11 = Always uses LPRC

10 = Uses FRC when WINDIS = 0, system clock is not LPRC and device is not in Sleep; otherwise, uses LPRC

01 = Always uses SOSC

00 = Uses FOSC/2 when system clock is not LPRC and device is not in Sleep; otherwise, uses LPRC

When WDTCMX = 0:

LPRC is always the WDT clock source.

bit 12 **Unimplemented:** Read as '1'

bit 11 **WDTCMX:** WDT Clock Multiplexer Control bit

1 = Enables WDT clock multiplexing

0 = WDT clock multiplexing is disabled

bit 10 **Unimplemented:** Read as '1'

bit 9-8 **WDTWIN<1:0>:** Watchdog Timer Window Width Select bits

11 = 25%

10 = 37.5%

01 = 50%

00 = 75%

bit 7 **WINDIS:** Windowed Watchdog Timer Disable bit

1 = Standard Watchdog Timer is enabled

0 = Windowed Watchdog Timer is enabled (FWDTEN<1:0> must not be '00')

bit 6-5 **FWDTEN<1:0>:** Watchdog Timer Configuration bits

11 = WDT is always enabled; SWDTEN bit has no effect

10 = WDT is enabled and controlled in firmware by the SWDTEN bit

01 = WDT is enabled only in Run mode and disabled in Sleep modes; SWDTEN bit is disabled

00 = WDT is disabled; SWDTEN bit is disabled

bit 4 **FWPSA:** WDT Prescaler Ratio Select bit

1 = Prescaler ratio of 1:128

0 = Prescaler ratio of 1:32