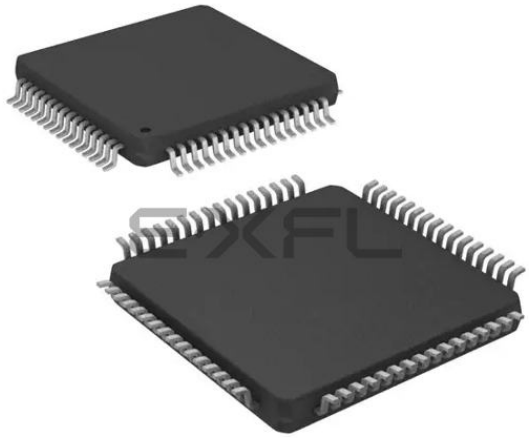

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64gb406-i-pt

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC24FJ64GA406
- PIC24FJ128GA406
- PIC24FJ256GA406
- PIC24FJ64GA410
- PIC24FJ128GA410
- PIC24FJ256GA410
- PIC24FJ64GA412
- PIC24FJ128GA412
- PIC24FJ256GA412
- PIC24FJ64GB406
- PIC24FJ128GB406
- PIC24FJ256GB406
- PIC24FJ64GB410
- PIC24FJ128GB410
- PIC24FJ256GB410
- PIC24FJ64GB412
- PIC24FJ128GB412
- PIC24FJ256GB412

The PIC24FJ256GA412/GB412 family expands the capabilities of the PIC24F family by adding a complete selection of advanced analog peripherals to its existing digital features. This combination, along with its ultra low-power features, Direct Memory Access (DMA) for peripherals, USB On-The-Go (OTG) and a built-in LCD Controller and driver, makes this family the new standard for mixed-signal PIC® microcontrollers in one economical and power-saving package.

1.1 Core Features

1.1.1 16-BIT ARCHITECTURE

Central to all PIC24F devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC® Digital Signal Controllers (DSCs). The PIC24F CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths with the ability to move information between data and memory spaces
- Linear addressing of up to 12 Mbytes (program space) and 32 Kbytes (data)
- A 16-element Working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32 by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages, such as 'C'
- Operational performance up to 16 MIPS

1.1.2 XLP POWER-SAVING TECHNOLOGY

The PIC24FJ256GA412/GB412 family of devices incorporates a greatly expanded range of power-saving operating modes for the ultimate in power conservation. The new modes include:

- Retention Sleep, with essential circuits being powered from a separate low-voltage regulator
- Deep Sleep without RTCC, for the lowest possible power consumption under software control
- V_{BAT} mode (with or without RTCC), to continue limited operation from a backup battery when V_{DD} is removed

Many of these new low-power modes also support the continuous operation of the low-power, on-chip Real-Time Clock/Calendar (RTCC), making it possible for an application to keep time while the device is otherwise asleep.

Aside from these new features, the PIC24FJ256GA412/GB412 devices also include all of the legacy power-saving features of previous PIC24F microcontrollers, such as:

- On-the-Fly Clock Switching, allowing the selection of a lower power clock during run time
- Doze Mode Operation, for maintaining peripheral clock speed while slowing the CPU clock
- Instruction-Based Power-Saving Modes, for quick invocation of Idle and the many Sleep modes

1.1.3 DUAL PARTITION FLASH PROGRAM MEMORY

A brand new feature to the PIC24F family is the use of Dual Partition Flash program memory technology. This allows PIC24FJ256GA412/GB412 family devices a range of new operating options not available before:

- Dual Partition Operation, which can store two different applications in their own code partition, and allows for the support of robust bootloader applications and enhanced security
- Live Update Operation, which allows the main application to continue operation while the second Flash partition is being reprogrammed – all without adding Wait states to code execution
- Direct Run-Time Programming from Data RAM, with the option of data compression in the RAM image

PIC24FJ256GA412/GB412 family devices can also operate with their two Flash partitions as one large program memory, providing space for large and complex applications.

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
AN0	16	25	K2	I	ANA	A/D Analog Inputs
AN1	15	24	K1	I	ANA	
AN1-	15	24	K1	I	ANA	
AN2	14	23	J2	I	ANA	
AN3	13	22	J1	I	ANA	
AN4	12	21	H2	I	ANA	
AN5	11	20	H1	I	ANA	
AN6	17	26	L1	I	ANA	
AN7	18	27	J3	I	ANA	
AN8	21	32	K4	I	ANA	
AN9	22	33	L4	I	ANA	
AN10	23	34	H5	I	ANA	
AN11	24	35	K5	I	ANA	
AN12	27	41	J7	I	ANA	
AN13	28	42	L7	I	ANA	
AN14	29	43	K7	I	ANA	
AN15	30	44	L8	I	ANA	
AN16	—	9	E1	I	ANA	
AN17	—	10	E3	I	ANA	
AN18	—	11	F4	I	ANA	
AN19	—	12	F2	I	ANA	
AN20	—	14	F3	I	ANA	
AN21	—	19	G2	I	ANA	
AN22	—	92	E11	I	ANA	
AN23	—	91	E10	I	ANA	
AVDD	19	30	J4	P	—	Positive Supply for Analog modules
AVSS	20	31	L3	P	—	Ground Reference for Analog modules
C1INA	11	20	H1	I	ANA	Comparator 1 Input A
C1INB	12	21	H2	I	ANA	Comparator 1 Input B
C1INC	5,8	11,14	F4,F3	I	ANA	Comparator 1 Input C
C1IND	4	10	E3	I	ANA	Comparator 1 Input D
C2INA	13	22	J1	I	ANA	Comparator 2 Input A
C2INB	14	23	J2	I	ANA	Comparator 2 Input B
C2INC	8	14	F3	I	ANA	Comparator 2 Input C
C2IND	6	12	F2	I	ANA	Comparator 2 Input D
C3INA	55	84	C7	I	ANA	Comparator 3 Input A
C3INB	54	83	D7	I	ANA	Comparator 3 Input B
C3INC	8,45	14,71	F3,C11	I	ANA	Comparator 3 Input C
C3IND	44	70	D11	I	ANA	Comparator 3 Input D
CLC3OUT	46	72	D9	O	DIG	CLC3 Output
CLC4OUT	42	68	E9	O	DIG	CLC4 Output

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
IOCG0	—	90	A5	I	ST	PORTG Interrupt-on-Change
IOCG1	—	89	E6	I	ST	
IOCG2	37	57	H10	I	ST	
IOCG3	36	56	J11	I	ST	
IOCG6	4	10	E3	I	ST	
IOCG7	5	11	F4	I	ST	
IOCG8	6	12	F2	I	ST	
IOCG9	8	14	F3	I	ST	
IOCG12	—	96	E17	I	ST	
IOCG13	—	97	E18	I	ST	
IOCG14	—	95	E16	I	ST	
IOCG15	—	1	B2	I	ST	
IOCH1	—	—	B1	I	ST	PORTH Interrupt-on-Change
IOCH2	—	—	D4	I	ST	
IOCH3	—	—	G4	I	ST	
IOCH4	—	—	H3	I	ST	
IOCH5	—	—	H4	I	ST	
IOCH6	—	—	L5	I	ST	
IOCH7	—	—	J5	I	ST	
IOCH8	—	—	H7	I	ST	
IOCH9	—	—	J8	I	ST	
IOCH10	—	—	J9	I	ST	
IOCH11	—	—	G8	I	ST	
IOCH12	—	—	F7	I	ST	
IOCH13	—	—	C9	I	ST	
IOCH14	—	—	A8	I	ST	
IOCH15	—	—	F6	I	ST	
IOCJ0	—	—	E13	I	ST	PORTJ Interrupt-on-Change
IOCJ1	—	—	E14	I	ST	
LCDBIAS0	3	5	D2	O	ANA	Bias Inputs for LCD Driver Charge Pump
LCDBIAS1	2	4	C1	O	ANA	
LCDBIAS2	1	3	D3	O	ANA	
LCDBIAS3	17	26	L1	O	ANA	
LVDIN	64	100	E31	I	ANA	Low-Voltage Detect Input
$\overline{MCLR}$	7	13	F1	I	ST/STMV	Master Clear (device Reset) Input. This line is brought low to cause a Reset.
OC4	54	83	D7	O	DIG	Output Compare 4 Output
OC5	55	84	C7	O	DIG	Output Compare 5 Output
OC6	58	87	B6	O	DIG	Output Compare 6 Output

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

3.2 CPU Control Registers

REGISTER 3-1: SR: ALU STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	DC
bit 15							bit 8

R/W-0(1)	R/W-0(1)	R/W-0(1)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2(2)	IPL1(2)	IPL0(2)	RA	N	OV	Z	C
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **DC:** ALU Half Carry/Borrow bit
- 1 = A carry out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
- 0 = No carry out from the 4th or 8th low-order bit of the result has occurred

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits(1,2)
- 111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
- 110 = CPU Interrupt Priority Level is 6 (14)
- 101 = CPU Interrupt Priority Level is 5 (13)
- 100 = CPU Interrupt Priority Level is 4 (12)
- 011 = CPU Interrupt Priority Level is 3 (11)
- 010 = CPU Interrupt Priority Level is 2 (10)
- 001 = CPU Interrupt Priority Level is 1 (9)
- 000 = CPU Interrupt Priority Level is 0 (8)

bit 4 **RA:** REPEAT Loop Active bit
- 1 = REPEAT loop is in progress
- 0 = REPEAT loop is not in progress

bit 3 **N:** ALU Negative bit
- 1 = Result was negative
- 0 = Result was not negative (zero or positive)

bit 2 **OV:** ALU Overflow bit
- 1 = Overflow occurred for signed (2's complement) arithmetic in this arithmetic operation
- 0 = No overflow has occurred

bit 1 **Z:** ALU Zero bit
- 1 = An operation, which affects the Z bit, has set it at some time in the past
- 0 = The most recent operation, which affects the Z bit, has cleared it (i.e., a non-zero result)

bit 0 **C:** ALU Carry/$\overline{\text{Borrow}}$ bit
- 1 = A carry out from the Most Significant bit (MSb) of the result occurred
- 0 = No carry out from the Most Significant bit of the result occurred

Note 1: The IPLx Status bits are read-only when NSTDIS (INTCON1<15>) = 1.

2: The IPLx Status bits are concatenated with the IPL3 Status (CORCON<3>) bit to form the CPU Interrupt Priority Level (IPL). The value in parentheses indicates the IPL when IPL3 = 1.

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4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-2).

Program memory addresses are always word-aligned on the lower word and addresses are incremented or decremented by two during code execution. This arrangement also provides compatibility with data memory space addressing and makes it possible to access data in the program memory space.

4.1.2 HARD MEMORY VECTORS

All PIC24F devices reserve the addresses between 000000h and 000200h for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user at 000000h with the actual address for the start of code at 000002h.

PIC24F devices also have two Interrupt Vector Tables (IVTs). The main IVT has a static location, from 000004h to 0000FFh. The Alternate IVT has a configurable location and is optionally enabled. A more detailed discussion of the Interrupt Vector Tables is provided in **Section 8.0 "Interrupt Controller"**.

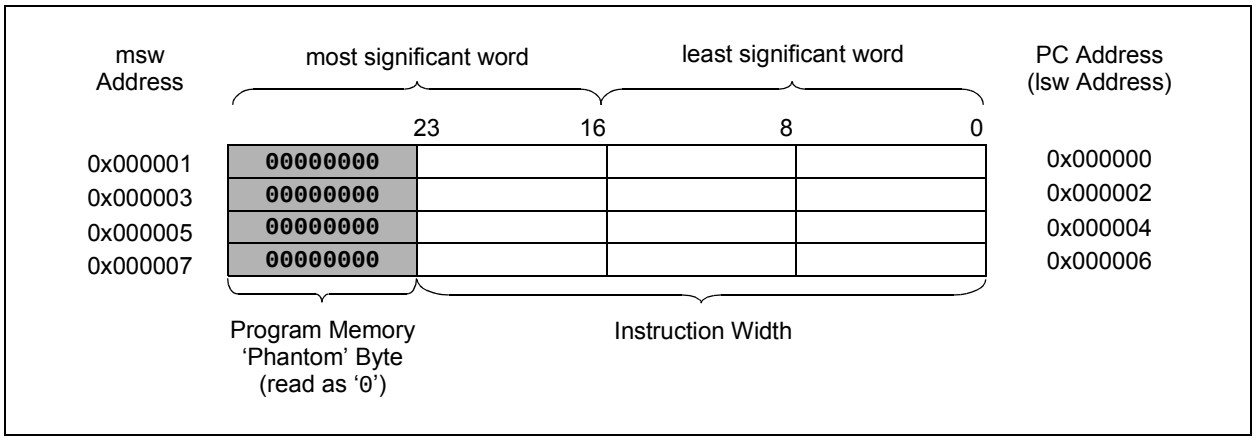
4.1.3 SINGLE AND DUAL PARTITION MEMORY ORGANIZATION

The PIC24FJ256GA412/GB412 family of devices supports a Single Partition Flash mode and two Dual Partition Flash modes. The Dual Partition modes allow the device to be programmed with two separate applications to facilitate bootloading or to allow an application to be programmed at run-time without stalling the CPU.

In the Dual Partition modes, the device's memory is divided evenly into two physical sections, known as Partition 1 and Partition 2. Each of these partitions contains its own program memory and Configuration Words. During program execution, the code on only one of these panels is executed; this is the Active Partition. The other partition, or the Inactive Partition, is not used, but can be programmed.

The Active Partition is always mapped to logical address, 000000h, while the Inactive Partition will always be mapped to logical address, 400000h. Note that even when the code partitions are switched between active and inactive by the user, the address of the Active Partition will still be 000000h and the address of the Inactive Partition will still be at 400000h. Figure 4-3 compares the mapping of the user memory space in Single and Dual Partition devices.

FIGURE 4-2: PROGRAM MEMORY ORGANIZATION



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REGISTER 8-10: IFS4: INTERRUPT FLAG STATUS REGISTER 4

U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
—	DAC1IF	CTMUIF	—	—	—	CCP7IF	HLVDIF
bit 15							bit 8

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
MI2C3IF	SI2C3IF	—	—	CRCIF	U2ERIF	U1ERIF	CCP2IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **DAC1IF:** DAC Converter Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13 **CTMUIF:** CTMU Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CCP7IF:** SCCP7 Capture/Compare Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 8 **HLVDIF:** High/Low-Voltage Detect Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 7 **MI2C3IF:** Master I2C3 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6 **SI2C3IF:** Slave I2C3 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **CRCIF:** CRC Generator Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **U2ERIF:** UART2 Error Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **U1ERIF:** UART1 Error Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **CCP2IF:** SCCP2 Capture/Compare Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

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REGISTER 8-19: IEC5: INTERRUPT ENABLE CONTROL REGISTER 5 (CONTINUED)

bit 3 **U3TXIE:** UART3 Transmitter Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **U3RXIE:** UART3 Receiver Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **U3ERIE:** UART3 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **Unimplemented:** Read as '0'

REGISTER 8-25: IPC3: INTERRUPT PRIORITY CONTROL REGISTER 3

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	NVMIP2	NVMIP1	NVMIP0	—	DMA1IP2	DMA1IP1	DMA1IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	AD1IP2	AD1IP1	AD1IP0	—	U1TXIP2	U1TXIP1	U1TXIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-11 **NVMIP<2:0>:** Flash Memory Write/Program Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 10-8 **DMA1IP<2:0>:** DMA Channel 1 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **AD1IP<2:0>:** 12-Bit Pipeline A/D Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **U1TXIP<2:0>:** UART1 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-29: IPC7: INTERRUPT PRIORITY CONTROL REGISTER 7

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	INT2IP2	INT2IP1	INT2IP0	—	T5IP2	T5IP1	T5IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **U2TXIP<2:0>:** UART2 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **U2RXIP<2:0>:** UART2 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **INT2IP<2:0>:** External Interrupt 2 Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **T5IP<2:0>:** Timer5 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit
If FSCM is enabled (FCKSM1 = 1):
1 = Clock and PLL selections are locked
0 = Clock and PLL selections are not locked and may be modified by setting the OSWEN bit
If FSCM is disabled (FCKSM1 = 0):
Clock and PLL selections are never locked and may be modified by setting the OSWEN bit.

bit 6 **IOLOCK:** I/O Lock Enable bit(2)
1 = I/O lock is active
0 = I/O lock is not active

bit 5 **LOCK:** PLL Lock Status bit(3)
1 = PLL module is in lock or PLL module start-up timer is satisfied
0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled

bit 4 **Unimplemented:** Read as '0'

bit 3 **CF:** Clock Fail Detect bit
1 = FSCM has detected a clock failure
0 = No clock failure has been detected

bit 2 **POSCEN:** Primary Oscillator Sleep Enable bit
1 = Primary Oscillator continues to operate during Sleep mode
0 = Primary Oscillator is disabled during Sleep mode

bit 1 **SOSCEN:** 32 kHz Secondary Oscillator (SOSC) Enable bit
1 = Enables Secondary Oscillator
0 = Disables Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit
1 = Initiates an oscillator switch to a clock source specified by the NOSC<2:0> bits
0 = Oscillator switch is complete

Note 1: Reset values for these bits are determined by the FNOSCx Configuration bits.
2: The state of the IOLOCK bit can only be changed once an unlocking sequence has been executed. In addition, if the IOL1WAY Configuration bit is '1' once the IOLOCK bit is set, it cannot be cleared.
3: This bit also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.
4: The default divisor of the postscaler is 2, which will generate a 4 MHz clock to the PLL module.

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A recommended code sequence for a clock switch includes the following:

1. Disable interrupts during the OSCCON register unlock and write sequence.
2. Execute the unlock sequence for the OSCCON high byte by writing 78h and 9Ah to OSCCON<15:8> in two back-to-back instructions.
3. Write the new oscillator source to the NOSCx bits in the instruction immediately following the unlock sequence.
4. Execute the unlock sequence for the OSCCON low byte by writing 46h and 57h to OSCCON<7:0> in two back-to-back instructions.
5. Set the OSWEN bit in the instruction immediately following the unlock sequence.
6. Continue to execute code that is not clock-sensitive (optional).
7. Invoke an appropriate amount of software delay (cycle counting) to allow the selected oscillator and/or PLL to start and stabilize.
8. Check to see if OSWEN is '0'. If it is, the switch was successful. If OSWEN is still set, then check the LOCK bit to determine the cause of the failure.

The core sequence for unlocking the OSCCON register and initiating a clock switch is shown in Example 9-1.

EXAMPLE 9-1: BASIC CODE SEQUENCE FOR CLOCK SWITCHING

```
;Place the new oscillator selection in W0
;OSCCONH (high byte) Unlock Sequence
MOV         #OSCCONH, w1
MOV         #0x78, w2
MOV         #0x9A, w3
MOV.b       w2, [w1]
MOV.b       w3, [w1]
;Set new oscillator selection
MOV.b       WREG, OSCCONH
;OSCCONL (low byte) unlock sequence
MOV         #OSCCONL, w1
MOV         #0x46, w2
MOV         #0x57, w3
MOV.b       w2, [w1]
MOV.b       w3, [w1]
;Start oscillator switch operation
BSET        OSCCON,#0
```

9.5 FRC Active Clock Tuning

PIC24FJ256GA412/GB412 family devices include an automatic mechanism to calibrate the FRC during run time. This system uses active clock tuning from a source of known accuracy to maintain the FRC within a very narrow margin of its nominal 8 MHz frequency. This allows for a frequency accuracy that is well within the requirements of the *"USB 2.0 Specification"*, regarding full-speed USB devices.

Note:	The self-tune feature maintains sufficient accuracy for operation in USB Device mode. For applications that function as a USB host, a high-accuracy clock source (±0.05%) is still required.

The self-tune system is controlled by the bits in the upper half of the OSCTUN register. Setting the STEN bit (OSCTUN<15>) enables the self-tuning feature, allowing the hardware to calibrate to a source selected by the STSRC bit (OSCTUN<12>). When STSRC = 1, the system uses the Start-of-Frame (SOF) packets from an external USB host for its source. When STSRC = 0, the system uses the crystal-controlled SOSC for its calibration source. Regardless of the source, the system uses the TUN<5:0> bits (OSCTUN<5:0>) to change the FRC Oscillator's frequency. Frequency monitoring and adjustment is dynamic, occurring continuously during run time. While the system is active, the TUNx bits cannot be written to by software.

Note:	To use the USB as a reference clock tuning source (STSRC = 1), the microcontroller must be configured for USB device operation and connected to a non-suspended USB host or hub port. If the SOSC is to be used as the reference clock tuning source (STSRC = 0), the SOSC must also be enabled for clock tuning to occur.

The self-tune system can generate a hardware interrupt, FSTIF. The interrupt can result from a drift of the FRC from the reference by greater than 0.2%, in either direction, or whenever the frequency deviation is beyond the ability of the TUNx bits to correct (i.e., greater than 1.5%). The STLOCK and STOR status bits (OSCTUN<11,9>) are used to indicate these conditions.

The STLPOL and STORPOL bits (OSCTUN<10,8>) configure the FSTIF interrupt to occur in the presence or the absence of the conditions. It is the user's responsibility to monitor both the STLOCK and STOR bits to determine the exact cause of the interrupt.

Note:	The STLPOL and STORPOL bits should be ignored when the self-tune system is disabled (STEN = 0).

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REGISTER 11-2: IOCSTAT: INTERRUPT-ON-CHANGE STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0, HSC
—	—	—	—	—	—	—	IOCPJF(1)
bit 15							bit 8

R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IOCPHF(1)	IOCPGF	IOCPFF	IOCPEF	IOCPDF	IOCPCF	IOCPBF	IOCPAF(2)
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **IOCPJF:** Interrupt-on-Change PORTJ Flag bit(1)
1 = A change was detected on an IOC-enabled pin on PORTJ
0 = No change was detected or the user has cleared all detected changes

bit 7 **IOCPHF:** Interrupt-on-Change PORTH Flag bit(1)
1 = A change was detected on an IOC-enabled pin on PORTH
0 = No change was detected or the user has cleared all detected changes

bit 6 **IOCPGF:** Interrupt-on-Change PORTG Flag bit
1 = A change was detected on an IOC-enabled pin on PORTG
0 = No change was detected or the user has cleared all detected changes

bit 5 **IOCPFF:** Interrupt-on-Change PORTF Flag bit
1 = A change was detected on an IOC-enabled pin on PORTF
0 = No change was detected or the user has cleared all detected changes

bit 4 **IOCPEF:** Interrupt-on-Change PORTE Flag bit
1 = A change was detected on an IOC-enabled pin on PORTE
0 = No change was detected or the user has cleared all detected changes

bit 3 **IOCPDF:** Interrupt-on-Change PORTD Flag bit
1 = A change was detected on an IOC-enabled pin on PORTD
0 = No change was detected or the user has cleared all detected changes

bit 2 **IOCPCF:** Interrupt-on-Change PORTC Flag bit
1 = A change was detected on an IOC-enabled pin on PORTC
0 = No change was detected or the user has cleared all detected changes

bit 1 **IOCPBF:** Interrupt-on-Change PORTB Flag bit
1 = A change was detected on an IOC-enabled pin on PORTB
0 = No change was detected or the user has cleared all detected changes

bit 0 **IOCPAF:** Interrupt-on-Change PORTA Flag bit(2)
1 = A change was detected on an IOC-enabled pin on PORTA
0 = No change was detected, or the user has cleared all detected change

Note 1: These ports are not available on 64-pin or 100-pin devices.
2: This port is not available on 64-pin devices.

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11.5 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. In an application that needs to use more than one peripheral multiplexed on a single pin, inconvenient work arounds in application code, or a complete redesign, may be the only option.

The Peripheral Pin Select (PPS) feature provides an alternative to these choices by enabling the user's peripheral set selection and its placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the microcontroller to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of any one of many digital peripherals to any one of these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.5.1 AVAILABLE PINS

The PPS feature is used with a range of up to 44 pins, depending on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the designation, "RPn" or "RPIn", in their full pin designation, where "n" is the remappable pin number. "RP" is used to designate pins that support both remappable input and output functions, while "RPI" indicates pins that support remappable input functions only.

PIC24FJ256GA412/GB412 family devices support a larger number of remappable input only pins than remappable input/output pins. In this device family, there are up to 32 remappable input/output pins, depending on the pin count of the particular device selected. These pins are numbered: RP0 through RP31. See Table 1-4 and Table 1-5 for a summary of pinout options in each package offering.

11.5.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer related peripherals (input capture and output compare) and external interrupt inputs. Also included are the outputs of the comparator module, since these are discrete digital signals.

PPS is not available for analog peripherals or these digital peripherals:

- I^2C (input and output)
- RTCC Alarm and Power Gate Outputs
- EPMP Signals (input and output)
- INT0

A key difference between pin select and non-pin select peripherals is that pin select peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-pin select peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

11.5.2.1 Peripheral Pin Select Function Priority

Pin-selectable peripheral outputs (e.g., output compare, UART transmit) will take priority over general purpose digital functions on a pin, such as EPMP and port I/O. Specialized digital outputs will take priority over PPS outputs on the same pin. The pin diagrams list peripheral outputs in the order of priority. Refer to them for priority concerns on a particular pin.

Unlike PIC24F devices with fixed peripherals, pin-selectable peripheral inputs will never take ownership of a pin. The pin's output buffer will be controlled by the TRISx setting or by a fixed peripheral on the pin. If the pin is configured in Digital mode, then the PPS input will operate correctly. If an analog function is enabled on the pin, the PPS input will be disabled.

11.5.3 CONTROLLING PERIPHERAL PIN SELECT

PPS features are controlled through two sets of Special Function Registers (SFRs): one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on if an input or an output is being mapped.

11.5.3.1 Input Mapping

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral; that is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers (Register 11-3 through Register 11-22) are used to configure peripheral input mapping. Each register contains two sets of 6-bit fields, with each set associated with one of the pin-selectable peripherals. Programming a given peripheral's bit field with an appropriate 6-bit value maps the RPn/RPIn pin with that value to that peripheral.

Table 11-11 summarizes the remappable inputs available with Peripheral Pin Select. For any given device, the valid range of values for any of the bit fields corresponds to the maximum number of Peripheral Pin Selections supported by the device.

Note:	Unless otherwise noted, all remappable inputs utilize Schmitt Trigger buffers.

14.5 Auxiliary Output

The MCCPx and SCCPx modules have an auxiliary (secondary) output that provides other peripherals access to internal module signals. The auxiliary output is intended to connect to other MCCP or SCCP modules, or other digital peripherals, to provide these types of functions:

- Time Base Synchronization
- Peripheral Trigger and Clock Inputs
- Signal Gating

The type of output signal is selected using the AUXOUT<1:0> control bits (CCPxCON2H<4:3>). The type of output signal is also dependent on the module operating mode.

On the PIC24FJ256GA412/GB412 family of devices, only the CTMU discharge trigger has access to the auxiliary output signal.

TABLE 14-4: AUXILIARY OUTPUT

AUXOUT<1:0>	CCSEL	MOD<3:0>	Comments	Signal Description
00	x	xxxx	Auxiliary output disabled	No Output
01	0	0000	Time Base modes	Time Base Period Reset or Rollover
10				Special Event Trigger Output
11				No Output
01	0	0001 through 1111	Output Compare modes	Time Base Period Reset or Rollover
10				Output Compare Event Signal
11				Output Compare Signal
01	1	xxxx	Input Capture modes	Time Base Period Reset or Rollover
10				Reflects the Value of the ICDIS bit
11				Input Capture Event Signal

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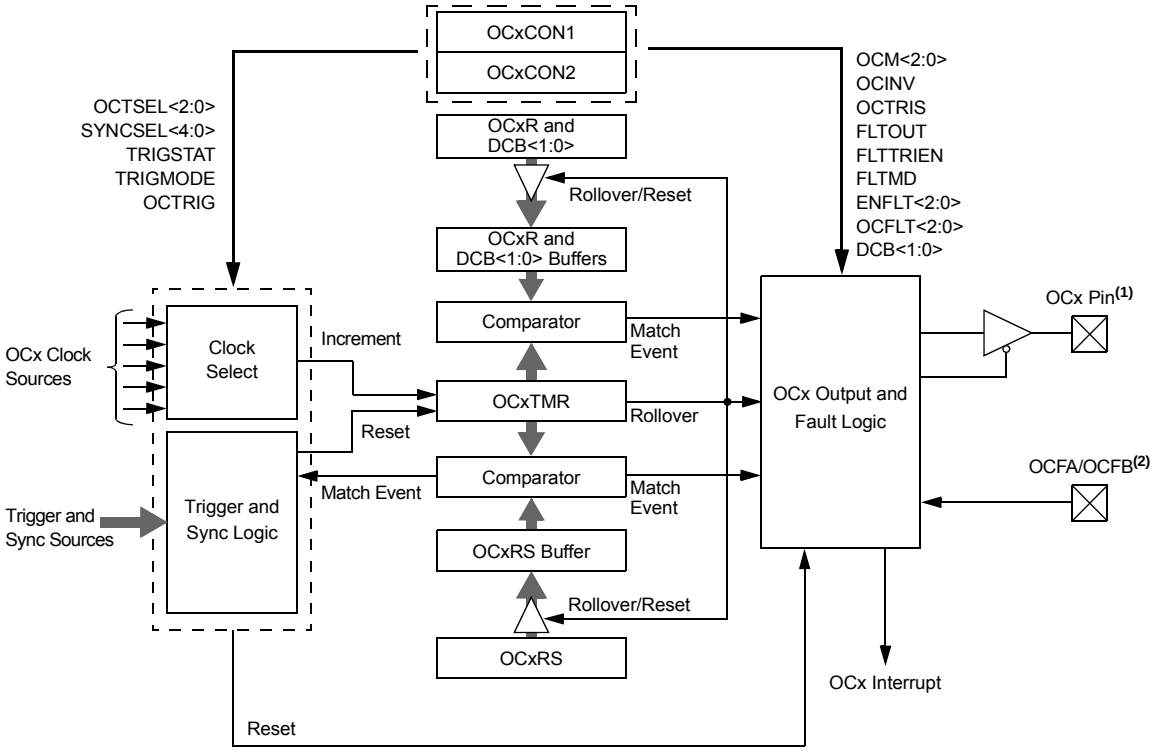
FIGURE 16-2: OUTPUT COMPARE x BLOCK DIAGRAM (DOUBLE-BUFFERED, 16-BIT PWM MODE)



Note 1: The OCx outputs must be assigned to an available RPn pin before use. For more information, see **Section 11.5 "Peripheral Pin Select (PPS)"**.

2: The OCFA/OCFB Fault inputs must be assigned to an available RPn/RPIn pin before use. For more information, see **Section 11.5 "Peripheral Pin Select (PPS)"**.

16.3.1 PWM PERIOD

The PWM period is specified by writing to PRy, the Timery Period register. The PWM period can be calculated using Equation 16-1.

EQUATION 16-1: CALCULATING THE PWM PERIOD(1)

PWM Period = [(PRy) + 1] • TCY • (Timer Prescale Value)

where: PWM Frequency = 1/[PWM Period]

Note 1: Based on TCY = TOSC * 2; Doze mode and PLL are disabled.

Note: A PRy value of N will produce a PWM period of N + 1 time base count cycles. For example, a value of 7 written into the PRy register, will yield a period consisting of 8 time base cycles.

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NOTES:

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TABLE 22-1: LCDDATA REGISTERS AND BITS FOR SEGMENT AND COM COMBINATIONS

COM Lines	Segments			
	0 to 15	16 to 31	32 to 47	48 to 64
0	LCDDATA0 S00C0:S15C0	LCDDATA1 S16C0:S31C0	LCDDATA2 S32C0:S47C0	LCDDATA3 S48C0:S63C0
1	LCDDATA4 S00C1:S15C1	LCDDATA5 S16C1:S31C1	LCDDATA6 S32C1:S47C1	LCDDATA7 S48C1:S63C1
2	LCDDATA8 S00C2:S15C2	LCDDATA9 S16C2:S31C2	LCDDATA10 S32C2:S47C2	LCDDATA11 S48C2:S63C2
3	LCDDATA12 S00C3:S15C3	LCDDATA13 S16C3:S31C3	LCDDATA14 S32C3:S47C3	LCDDATA15 S48C3:S63C3
4	LCDDATA16 S00C4:S15C4	LCDDATA17 S16C4:S31C4	LCDDATA18 S32C4:S47C4	LCDDATA19 S48C4:S59C4
5	LCDDATA20 S00C5:S15C5	LCDDATA21 S16C5:S31C5	LCDDATA22 S32C5:S47C5	LCDDATA23 S48C5:S69C5
6	LCDDATA24 S00C6:S15C6	LCDDATA25 S16C6:S31C6	LCDDATA26 S32C6:S47C6	LCDDATA27 S48C6:S59C6
7	LCDDATA28 S00C7:S15C7	LCDDATA29 S16C7:S31C7	LCDDATA30 S32C7:S47C7	LCDDATA31 S48C7:S59C7

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34.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

34.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

34.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

34.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

34.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

TABLE 36-21: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
OS50	FPLLI	PLL Input Frequency Range(1)	1.97	4	4.04	MHz	ECPLL, XTPLL, HSPLL or FRCPLL modes
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	128	µs	
OS53	DCLK	CLKO Stability (Jitter)	-0.25	—	0.25	%	

Note 1: The PLL accepts a 1.97 MHz to 4.04 MHz input frequency. Higher input frequencies, up to 48 MHz, may be supplied to the PLL if they are prescaled down by the PLLMODE<3:0> Configuration bits into the 1.97 MHz to 4.04 MHz range.

TABLE 36-22: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Characteristic	Min	Typ	Max	Units	Conditions
F20	FRC Accuracy @ 8 MHz(4)	-1	±0.15	1	%	2.0V ≤ VDD ≤ 3.6V, 0°C ≤ TA ≤ +85°C **(Note 1)**
		-1.5	—	1.5	%	2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA < 0°C
		-0.20	±0.05	0.20	%	2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C, self-tune is enabled and locked **(Note 2)**
F21	LPRC @ 31 kHz	-20	—	20	%	
F22	OSCTUN Step-Size	—	0.05	—	%/bit	
F23	FRC Self-Tune Lock Time	—	<5	8	ms	**(Note 3)**

Note 1: To achieve this accuracy, physical stress applied to the microcontroller package (ex., by flexing the PCB) must be kept to a minimum.

2: Accuracy measured with respect to reference source accuracy.

3: Time from when the reference clock is stable and in range until the FRC is tuned within the range specified by F20 (with self-tune).

4: Other frequencies that are derived from the FRC (either through digital division by prescalers or multiplication through a PLL) will also have the same accuracy tolerance specifications as provided here.

TABLE 36-23: RC OSCILLATOR START-UP TIME

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
FR0	TFRC	FRC Oscillator Start-up Time	—	15	—	µs	
FR1	TLPRC	Low-Power RC Oscillator Start-up Time	—	50	—	µs	

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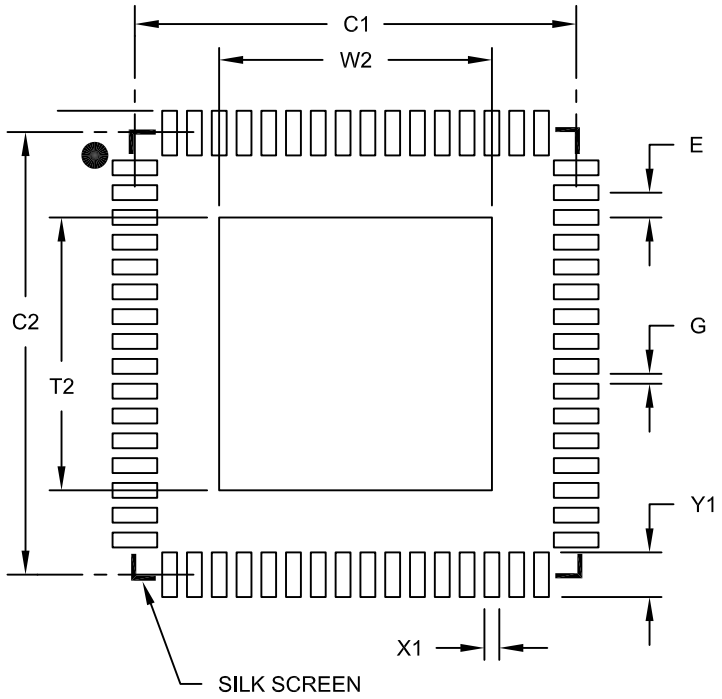
64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length and 5.40x5.40mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			5.50
Optional Center Pad Length	T2			5.50
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2154A