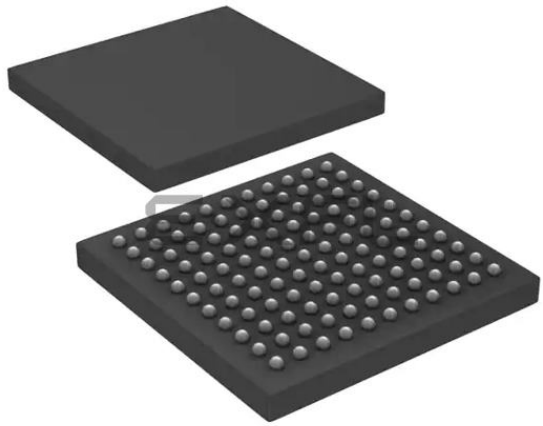
Microchip Technology - PIC24FJ64GB412T-I/BG Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP/PSP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	101
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64gb412t-i-bg

1.6 Other Special Features

- **Integrated Interrupt-on-Change:** All digital I/O ports now feature Interrupt-on-Change (IOC) functionality for convenient Change Notification interrupt generation on any I/O pin. IOC can be individually enabled or disabled on each pin, and configured for both edge detection polarity and the use of pull-ups or pull-downs.
- **Peripheral Pin Select (PPS):** The Peripheral Pin Select feature allows most digital peripherals to be mapped over a fixed set of digital I/O pins. Users may independently map the input and/or output of any one of the many digital peripherals to any one of the I/O pins.
- **Communications:** The PIC24FJ256GA412/GB412 family incorporates multiple serial communication peripherals to handle a range of application requirements. All devices have six independent UARTs with built-in IrDA® encoders/decoders. There are also three independent I^2C modules that support both Master and Slave modes of operation, and three SPI modules with I^2S and variable data width support.
- **Analog Features:** All members of the PIC24FJ256GA412/GB412 family include a 12-bit A/D Converter module, a triple comparator module and the CTMU interface. The A/D module incorporates a range of features that allow the converter to assess and make decisions on incoming data, reducing CPU overhead for routine A/D conversions.
  The comparator module includes three analog comparators that are configurable for a wide range of operations. The CTMU provides a convenient method for precision time measurement and pulse generation, and can serve as an interface for capacitive sensors.
- **Enhanced Parallel Master/Parallel Slave Port:** This module allows rapid and transparent access to the microcontroller data bus, and enables the CPU to directly address external data memory. The parallel port can function in Master or Slave mode, accommodating data widths of 4, 8 or 16 bits, and address widths of up to 23 bits in Master modes.
- **Real-Time Clock and Calendar (RTCC):** This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.

1.7 Details on Individual Family Members

Devices in the PIC24FJ256GA412/GB412 family are available in 64-pin, 100-pin and 121-pin packages. General block diagrams for general purpose and USB devices are shown in Figure 1-1 and Figure 1-2, respectively.

The devices are differentiated from each other in five ways:

1. USB On-The-Go functionality (present only in PIC24FJXXXGB4XX devices).
2. Available I/O pins and ports (up to 53 pins on 6 ports for 64-pin devices, up to 85 pins on 7 ports for 100-pin devices and up to 102 pins on 9 ports for 121-pin devices).
3. Available remappable pins (29 pins on 64-pin devices and 44 pins on 100/121-pin devices).
4. Maximum available drivable LCD pixels (up to 248 for 64-pin devices and 512 on 100/121-pin devices.)
5. Analog input channels for the A/D Converter (16 channels for 64-pin devices and 24 channels for 100/121-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1, Table 1-2 and Table 1-3.

A list of pin features available on the PIC24FJ256GA412/GB412 family devices, sorted by function, is shown in Table 1-4 (for general purpose devices) or Table 1-5 (for USB devices). Note that these tables show the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams in the beginning of this data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

TABLE 1-2: DEVICE FEATURES FOR THE PIC24FJ256GA412/GB412 FAMILY: 100-PIN

Features	PIC24FJXXXGA/GB410					
	64GA	128GA	256GA	64GB	128GB	256GB
Operating Frequency	DC – 32 MHz					
Program Memory (bytes)	64K	128K	256K	64K	128K	256K
Program Memory (instructions)	22,016	44,032	88,064	22,016	44,032	88,064
Data Memory (bytes)	8K	16K		8K	16K	
Interrupt Sources (soft vectors/ NMI traps)	113 (107/6)					
I/O Ports	Ports A, B, C, D, E, F, G					
Total I/O Pins	85			84		
Remappable Pins	44 (32 I/Os, 12 input only)					
Timers:						
Total Number (16-bit)	19(1,2)					
32-Bit (from paired 16-bit timers)	9					
Input Capture w/Timer Channels	6(2)					
Output Compare/PWM Channels	6(2)					
Capture/Compare/PWM/Timer:						
Single Output (SCCP)	6(2)					
Multiple Output (MCCP)	1(2)					
Serial Communications:						
UART	6(2)					
SPI (3-wire/4-wire)	4(2)					
I^2C	3					
USB On-The-Go	No			Yes		
Cryptographic Engine	Yes					
Parallel Communications (EPMP/PSP)	Yes					
10/12-Bit Analog-to-Digital Converter (A/D) (input channels)	24					
Digital-to-Analog Converter (DAC)	1					
Analog Comparators	3					
CTMU Interface	Yes					
LCD Controller (available pixels)	512 (64 SEG x 8 COM)					
JTAG Boundary Scan	Yes					
Resets (and delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, $\overline{MCLR}$, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)					
Instruction Set	77 Base Instructions, Multiple Addressing Mode Variations					
Packages	100-Pin TQFP					

Note 1: Includes the Timer modes of the SCCP and MCCP modules.

2: Some instantiations of these modules are only available through remappable pins.

TABLE 1-3: DEVICE FEATURES FOR THE PIC24FJ256GA412/GB412 FAMILY: 121-PIN

Features	PIC24FJXXXGA/GB412					
	64GA	128GA	256GA	64GB	128GB	256GB
Operating Frequency	DC – 32 MHz					
Program Memory (bytes)	64K	128K	256K	64K	128K	256K
Program Memory (instructions)	22,016	44,032	88,064	22,016	44,032	88,064
Data Memory (bytes)	8K	16K		8K	16K	
Interrupt Sources (soft vectors/ NMI traps)	113 (107/6)					
I/O Ports	Ports A, B, C, D, E, F, G, H, J					
Total I/O Pins	102			101		
Remappable Pins	44 (32 I/O, 12 input only)					
Timers:						
Total Number (16-bit)	19(1,2)					
32-Bit (from paired 16-bit timers)	9					
Input Capture w/Timer Channels	6(2)					
Output Compare/PWM Channels	6(2)					
Single Output CCP (SCCP)	6					
Multiple Output CCP (MCCP)	1					
Serial Communications:						
UART	6(2)					
SPI (3-wire/4-wire)	4(2)					
I^2C	3					
USB On-The-Go	No			Yes		
Cryptographic Engine	Yes					
Parallel Communications (EPMP/PSP)	Yes					
10/12-Bit Analog-to-Digital Converter (A/D) (input channels)	24					
Digital-to-Analog Converter (DAC)	1					
Analog Comparators	3					
CTMU Interface	Yes					
LCD Controller (available pixels)	512 (64 SEG x 8 COM)					
JTAG Boundary Scan	Yes					
Resets (and delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)					
Instruction Set	77 Base Instructions, Multiple Addressing Mode Variations					
Packages	121-Pin TFBGA					

Note 1: Includes the Timer modes of SCCP and MCCP modules.

2: Some instantiations of these modules are only available through remappable pins.

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
AN0	16	25	K2	I	ANA	A/D Analog Inputs
AN1	15	24	K1	I	ANA	
AN1-	15	24	K1	I	ANA	
AN2	14	23	J2	I	ANA	
AN3	13	22	J1	I	ANA	
AN4	12	21	H2	I	ANA	
AN5	11	20	H1	I	ANA	
AN6	17	26	L1	I	ANA	
AN7	18	27	J3	I	ANA	
AN8	21	32	K4	I	ANA	
AN9	22	33	L4	I	ANA	
AN10	23	34	H5	I	ANA	
AN11	24	35	K5	I	ANA	
AN12	27	41	J7	I	ANA	
AN13	28	42	L7	I	ANA	
AN14	29	43	K7	I	ANA	
AN15	30	44	L8	I	ANA	
AN16	—	9	E1	I	ANA	
AN17	—	10	E3	I	ANA	
AN18	—	11	F4	I	ANA	
AN19	—	12	F2	I	ANA	
AN20	—	14	F3	I	ANA	
AN21	—	19	G2	I	ANA	
AN22	—	92	E11	I	ANA	
AN23	—	91	E10	I	ANA	
AVDD	19	30	J4	P	—	Positive Supply for Analog modules
AVSS	20	31	L3	P	—	Ground Reference for Analog modules
C1INA	11	20	H1	I	ANA	Comparator 1 Input A
C1INB	12	21	H2	I	ANA	Comparator 1 Input B
C1INC	5,8	11,14	F4,F3	I	ANA	Comparator 1 Input C
C1IND	4	10	E3	I	ANA	Comparator 1 Input D
C2INA	13	22	J1	I	ANA	Comparator 2 Input A
C2INB	14	23	J2	I	ANA	Comparator 2 Input B
C2INC	8	14	F3	I	ANA	Comparator 2 Input C
C2IND	6	12	F2	I	ANA	Comparator 2 Input D
C3INA	55	84	C7	I	ANA	Comparator 3 Input A
C3INB	54	83	D7	I	ANA	Comparator 3 Input B
C3INC	8,45	14,71	F3,C11	I	ANA	Comparator 3 Input C
C3IND	44	70	D11	I	ANA	Comparator 3 Input D
CLC3OUT	46	72	D9	O	DIG	CLC3 Output
CLC4OUT	42	68	E9	O	DIG	CLC4 Output

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

TABLE 1-4: PIC24FJ256GA412 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin/Pad Number			I/O	Input Buffer	Description
	64-Pin TQFP	100-Pin TQFP	121-Pin TFBGA			
INT0	46	72	D9	I	ST/STMV	External Interrupt Input 0
IOCA0	—	17	G3	I	ST	PORTA Interrupt-on-Change
IOCA1	—	38	J6	I	ST	
IOCA2	—	58	H11	I	ST	
IOCA3	—	59	G10	I	ST	
IOCA4	—	60	G11	I	ST	
IOCA5	—	61	G9	I	ST	
IOCA6	—	91	E10	I	ST	
IOCA7	—	92	E11	I	ST	
IOCA9	—	28	L2	I	ST	
IOCA10	—	29	K3	I	ST	
IOCA14	—	66	E11	I	ST	
IOCA15	—	67	E8	I	ST	
IOCB0	16	25	K2	I	ST	PORTB Interrupt-on-Change
IOCB1	15	24	K1	I	ST	
IOCB2	14	23	J2	I	ST	
IOCB3	13	22	J1	I	ST	
IOCB4	12	21	H2	I	ST	
IOCB5	11	20	H1	I	ST	
IOCB6	17	26	L1	I	ST	
IOCB7	18	27	J3	I	ST	
IOCB8	21	32	K4	I	ST	
IOCB9	22	33	L4	I	ST	
IOCB10	23	34	H5	I	ST	
IOCB11	24	35	K5	I	ST	
IOCB12	27	41	J7	I	ST	
IOCB13	28	42	L7	I	ST	
IOCB14	29	43	K7	I	ST	
IOCB15	30	44	L8	I	ST	
IOCC1	—	6	D1	I	ST	PORTC Interrupt-on-Change
IOCC2	—	7	E4	I	ST	
IOCC3	—	8	E2	I	ST	
IOCC4	—	9	E1	I	ST	
IOCC12	39	63	F9	I	ST	
IOCC13	47	73	C10	I	ST	
IOCC14	48	74	B11	I	ST	
IOCC15	40	64	F11	I	ST	

Legend: TTL = TTL input buffer
ANA = Analog-level input/output
DIG = Digital input/output
SMB = SMBus
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated transceiver

TABLE 4-12: SFR BLOCK 700h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
I/O (Continued)			AD1CON1	746	0000000000000000	RPINR13	7AA	0011111100111111
PORTJ	700	0000000000000000	AD1CON2	748	0000000000000000	RPINR14	7AC	0011111100111111
LATJ	702	0000000000000000	AD1CON3	74A	0000000000000000	RPINR15	7AE	0011111100111111
ODCJ	704	0000000000000000	AD1CHS	74C	0000000000000000	RPINR16	7B0	0011111100111111
IOCPJ	708	0000000000000000	AD1CSSL	74E	0000000000000000	RPINR17	7B2	0011111100111111
IOCNJ	70A	0000000000000000	AD1CSSH	750	0000000000000000	RPINR18	7B4	0011111100111111
IOCFJ	70C	0000000000000000	AD1CON4	752	0000000000000000	RPINR19	7B6	0011111100111111
IOCPUJ	70E	0000000000000000	AD1CON5	754	0000000000000000	RPINR20	7B8	0011111100111111
IOCPDJ	710	0000000000000000	AD1CHITL	756	0000000000000000	RPINR21	7BA	0011111100111111
A/D			AD1CHITH	758	0000000000000000	RPINR22	7BC	0011111100111111
AD1BUF0	712	xxxxxxxxxxxxxxxx	ADC1CTMENL	75A	0000000000000000	RPINR23	7BE	0011111100111111
AD1BUF1	714	xxxxxxxxxxxxxxxx	ADC1CTMENH	75C	0000000000000000	RPINR24	7C0	0011111100111111
AD1BUF2	716	xxxxxxxxxxxxxxxx	ADC1RESDMA	75E	0000000000000000	RPINR25	7C2	0011111100111111
AD1BUF3	718	xxxxxxxxxxxxxxxx	**NVM Controller**			RPINR26	7C4	0011111100111111
AD1BUF4	71A	xxxxxxxxxxxxxxxx	NVMCON	760	0000000000000000(1)	RPINR27	7C6	0011111100111111
AD1BUF5	71C	xxxxxxxxxxxxxxxx	NVMADRL	762	0000000000000000	RPINR28	7C8	0011111100111111
AD1BUF6	71E	xxxxxxxxxxxxxxxx	NVMADRH	764	0000000000000000	RPINR29	7CA	0011111100111111
AD1BUF7	720	xxxxxxxxxxxxxxxx	NVMKEY	766	0000000000000000	RPINR30	7CC	0011111100111111
AD1BUF8	722	xxxxxxxxxxxxxxxx	NVMSRCADRL	768	0000000000000000	RPINR31	7CE	0011111100111111
AD1BUF9	724	xxxxxxxxxxxxxxxx	NVMSRCADRH	76A	0000000000000000	RPOR0	7D4	0000000000000000
AD1BUF10	726	xxxxxxxxxxxxxxxx	JDATAL	77C	xxxxxxxxxxxxxxxx	RPOR1	7D6	0000000000000000
AD1BUF11	728	xxxxxxxxxxxxxxxx	JDATAH	77E	xxxxxxxxxxxxxxxx	RPOR2	7D8	0000000000000000
AD1BUF12	72A	xxxxxxxxxxxxxxxx	**Peripheral Pin Select**			RPOR3	7DA	0000000000000000
AD1BUF13	72C	xxxxxxxxxxxxxxxx	RPINR0	790	0011111100111111	RPOR4	7DC	0000000000000000
AD1BUF14	72E	xxxxxxxxxxxxxxxx	RPINR1	792	0011111100111111	RPOR5	7DE	0000000000000000
AD1BUF15	730	xxxxxxxxxxxxxxxx	RPINR2	794	0011111100111111	RPOR6	7E0	0000000000000000
AD1BUF16	732	xxxxxxxxxxxxxxxx	RPINR3	796	0011111100111111	RPOR7	7E2	0000000000000000
AD1BUF17	734	xxxxxxxxxxxxxxxx	RPINR4	798	0011111100111111	RPOR8	7E4	0000000000000000
AD1BUF18	736	xxxxxxxxxxxxxxxx	RPINR5	79A	0011111100111111	RPOR9	7E6	0000000000000000
AD1BUF19	738	xxxxxxxxxxxxxxxx	RPINR6	79C	0011111100111111	RPOR10	7E8	0000000000000000
AD1BUF20	73A	xxxxxxxxxxxxxxxx	RPINR7	7A2	0011111100111111	RPOR11	7EA	0000000000000000
AD1BUF21	73C	xxxxxxxxxxxxxxxx	RPINR8	7A0	0011111100111111	RPOR12	7EC	0000000000000000
AD1BUF22	73E	xxxxxxxxxxxxxxxx	RPINR9	7A2	0011111100111111	RPOR13	7EE	0000000000000000
AD1BUF23	740	xxxxxxxxxxxxxxxx	RPINR10	7A4	0011111100111111	RPOR14	7F0	0000000000000000
AD1BUF24	742	xxxxxxxxxxxxxxxx	RPINR11	7A6	0011111100111111	RPOR15	7F2	0000000000000000
AD1BUF25	744	xxxxxxxxxxxxxxxx	RPINR12	7A8	0011111100111111			

Legend: x = unknown or indeterminate value. Reset and address values are in hexadecimal.

Note 1: The Reset value shown is for POR only. The value on other Reset states is dependent on the state of memory write/erase operations or partition swap at the time of Reset.

REGISTER 7-2: RCON2: RESET AND SYSTEM CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	r-0	R/CO-1	R/CO-1	R/CO-1	R/CO-0
—	—	—	—	VDDBOR(1)	VDDPOR(1,2)	VBPOR(1,3)	VBAT(1)
bit 7							bit 0

Legend:	CO = Clearable Only bit	r = Reserved bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4 **Reserved:** Maintain as '0'

bit 3 **VDDBOR:** VDD Brown-out Reset Flag bit(1)
1 = A VDD Brown-out Reset has occurred (set by hardware)
0 = A VDD Brown-out Reset has not occurred

bit 2 **VDDPOR:** VDD Power-on Reset Flag bit(1,2)
1 = A VDD Power-on Reset has occurred (set by hardware)
0 = A VDD Power-on Reset has not occurred

bit 1 **VBPOR:** VBPOR Flag bit(1,3)
1 = A VBAT POR has occurred (no battery connected to VBAT pin or VBAT power below Deep Sleep Semaphore register retention level is set by hardware)
0 = A VBAT POR has not occurred

bit 0 **VBAT:** VBAT Flag bit(1)
1 = A POR exit has occurred while power was applied to VBAT pin (set by hardware)
0 = A POR exit from VBAT has not occurred

Note 1: This bit is set in hardware only; it can only be cleared in software.
2: This bit indicates a VDD Power-on Reset. Setting the POR bit (RCON<0>) indicates a VCORE Power-on Reset.
3: This bit is set when the device is originally powered up, even if power is present on VBAT.

TABLE 7-1: RESET FLAG BIT OPERATION

Flag Bit	Setting Event	Clearing Event
TRAPR (RCON<15>)	Trap Conflict Event	POR
IOPUWR (RCON<14>)	Illegal Opcode or Uninitialized W Register Access	POR
CM (RCON<9>)	Configuration Mismatch Reset	POR
EXTR (RCON<7>)	$\overline{MCLR}$ Reset	POR
SWR (RCON<6>)	RESET Instruction	POR
WDTO (RCON<4>)	WDT Time-out	CLRWDT, PWRSAV Instruction, POR
SLEEP (RCON<3>)	PWRSAV #0 Instruction	POR
DPSLP (RCON<10>)	PWRSAV #0 Instruction while DSEN bit is set	POR
IDLE (RCON<2>)	PWRSAV #1 Instruction	POR
BOR (RCON<1>)	POR, BOR	—
POR (RCON<0>)	POR	—

Note: All Reset flag bits may be set or cleared by the user software.

REGISTER 8-21: IEC7: INTERRUPT ENABLE CONTROL REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	JTAGIE	U6ERIE	U6TXIE	U6RXIE	U5ERIE	U5TXIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5 **JTAGIE:** JATG Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 4 **U6ERIE:** UART6 Error Interrupt Enable bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **U6TXIE:** UART6 Transmitter Interrupt Enable bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **U6RXIE:** UART6 Receiver Interrupt Enable bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **U5ERIE:** UART5 Error Interrupt Enable bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **U5TXIE:** UART5 Transmitter Interrupt Enable bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 8-25: IPC3: INTERRUPT PRIORITY CONTROL REGISTER 3

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	NVMIP2	NVMIP1	NVMIP0	—	DMA1IP2	DMA1IP1	DMA1IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	AD1IP2	AD1IP1	AD1IP0	—	U1TXIP2	U1TXIP1	U1TXIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-11 **NVMIP<2:0>:** Flash Memory Write/Program Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 10-8 **DMA1IP<2:0>:** DMA Channel 1 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **AD1IP<2:0>:** 12-Bit Pipeline A/D Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **U1TXIP<2:0>:** UART1 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-36: IPC14: INTERRUPT PRIORITY CONTROL REGISTER 14

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPI2RXIP2	SPI2RXIP1	SPI2RXIP0	—	SPI1RXIP2	SPI1RXIP1	SPI1RXIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPI4RXIP2	SPI4RXIP1	SPI4RXIP0	—	KEYSTRIP2	KEYSTRIP1	KEYSTRIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **SPI2RXIP<2:0>:** SPI2 Receive Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **SPI1RXIP<2:0>:** SPI1 Receive Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SPI4RXIP<2:0>:** SPI4 Receive Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **KEYSTRIP<2:0>:** Cryptographic Key Store Program Done Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-42: IPC20: INTERRUPT PRIORITY CONTROL REGISTER 20

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U3TXIP2	U3TXIP1	U3TXIP0	—	U3RXIP2	U3RXIP1	U3RXIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	U3ERIP2	U3ERIP1	U3ERIP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **U3TXIP<2:0>:** UART3 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **U3RXIP<2:0>:** UART3 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **U3ERIP<2:0>:** UART3 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

REGISTER 8-43: IPC21: INTERRUPT PRIORITY CONTROL REGISTER 21

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U4ERIP2	U4ERIP1	U4ERIP0	—	USB1IP2	USB1IP1	USB1IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	I2C2BCIP2	I2C2BCIP1	I2C2BCIP0	—	I2C1BCIP2	I2C1BCIP1	I2C1BCIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **U4ERIP<2:0>:** UART4 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **USB1IP<2:0>:** USB1 (USB OTG) Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **I2C2BCIP<2:0>:** I2C2 Bus Collision Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **I2C1BCIP<2:0>:** I2C1 Bus Collision Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

9.8 Reference Clock

In addition to the CLKO output (FOSC/2), available in certain oscillator modes, the device clock in the PIC24FJ256GA412/GB412 family devices can also be configured to provide a reference clock output signal to a port pin. This feature is available in all oscillator configurations and allows the user to select a greater range of clock submultiples to drive external devices in the application.

This reference clock output is controlled by the REFOCONL register (Register 9-4). Setting the ROEN bit (REFOCON<15>) makes the clock signal available on the REFO pin. The ROSEL<3:0> bits (REFOCONL<3:0>) determine which clock source is used for the reference clock output.

The REFOCONH and REFOTRIML registers (Register 9-5 and Register 9-6) select the divider from the selected clock input source from a wide range of options. The RODIV<14:0> bits (REFOCONH<14:0>) enable the selection of integer clock divider options, from 1:1 to 1:65,534. The ROTRIM<8:0> bits (REFOTRIML<15:7>) allow the user to add a fractional submultiple of the clock input to the RODIVx value.

The ROSWEN bit (REFOCONL<9>) indicates that the clock divider is currently being switched. In order to change the values of the RODIVx or ROTRIMx bits:

1. Verify that ROSWEN is clear
2. Write the updated values to the ROTRIMx and RODIVx bits.
3. Set the ROSWEN bit, then wait until it is clear before assuming that the REFO clock is valid.

The ROSLP bit (REFOCONL<11>) determines if the reference source is available on REFO when the device is in Sleep mode.To use the reference clock output in Sleep mode, the ROSLP bit must be set and the clock selected by the ROSELx bits must be enabled for operation during Sleep mode, if possible. Clearing the ROSELx bits allows the reference output frequency to change as the system clock changes during any clock switches. The ROOUT bit enables/disables the reference clock output on the REFO pin.

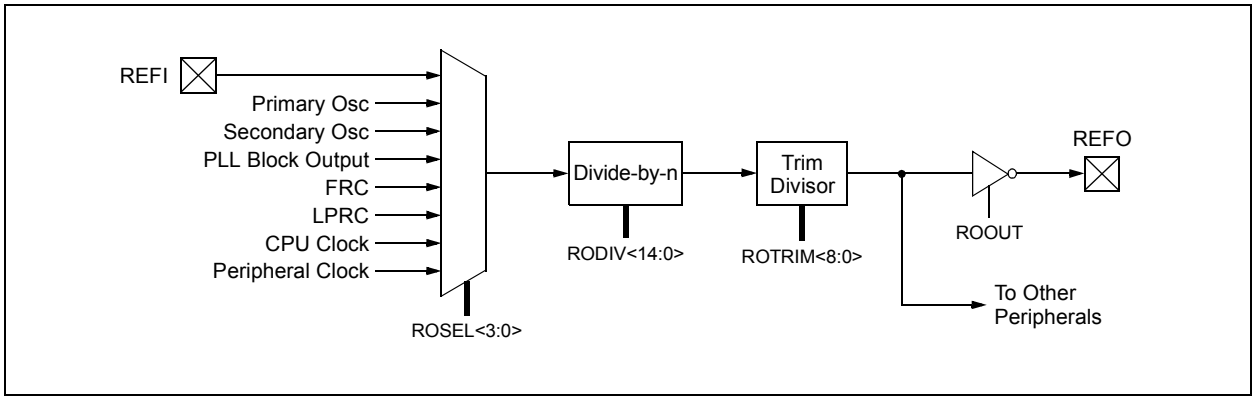
The ROACTIV bit (REFOCONL<8>) indicates that the module is active; it can be cleared by disabling the module (ROEN = 0). The user must not change the reference clock source, or adjust the trim or divider when the ROACTIV bit indicates that the module is active. To avoid glitches, the user should not disable the module until the ROACTIV bit is '1'.

9.8.1 REMAPPABLE OUTPUT

For PIC24FJ256GA412/GB412 family devices, the reference clock output is not available as a dedicated pin function. Instead, it is made available as an optional remappable digital output. If the reference clock output is required for an external consumer, it must be mapped to an available output pin. See **Section 11.5.3.2 "Output Mapping"** for more information.

When REFO is mapped to RP29 (RB15 pin), a reference clock frequency of up to 32 MHz may be used. The drive strength on this pin is also compatible with the fixed REFO pin on previous PIC24F devices. If REFO is mapped to any other output pin, the maximum reference clock frequency is limited to 16 MHz, with a lower drive strength.

FIGURE 9-3: SIMPLIFIED REFERENCE CLOCK BLOCK DIAGRAM



REGISTER 11-9: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	IC3R5	IC3R4	IC3R3	IC3R2	IC3R1	IC3R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **IC3R<5:0>:** Assign Input Capture 3 (IC3) to Corresponding RPn or RPIn Pin bits

REGISTER 11-10: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	OCFBR5	OCFBR4	OCFBR3	OCFBR2	OCFBR1	OCFBR0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	OCFAR5	OCFAR4	OCFAR3	OCFAR2	OCFAR1	OCFAR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **OCFBR<5:0>:** Assign Output Compare Fault B (OCFB) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **OCFAR<5:0>:** Assign Output Compare Fault A (OCFA) to Corresponding RPn or RPIn Pin bits

REGISTER 11-33: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP21R5	RP21R4	RP21R3	RP21R2	RP21R1	RP21R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP20R5	RP20R4	RP20R3	RP20R2	RP20R1	RP20R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP21R<5:0>:** RP21 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP21 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP20R<5:0>:** RP20 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP20 (see Table 11-12 for peripheral function numbers).

REGISTER 11-34: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP23R5	RP23R4	RP23R3	RP23R2	RP23R1	RP23R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP22R5	RP22R4	RP22R3	RP22R2	RP22R1	RP22R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP23R<5:0>:** RP23 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP23 (see Table 11-12 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP22R<5:0>:** RP22 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP22 (see Table 11-12 for peripheral function numbers).

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
TON	—	TSIDL	—	—	—	TECS1	TECS0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timer1 On bit
1 = Starts 16-bit Timer1
0 = Stops 16-bit Timer1

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9-8 **TECS<1:0>:** Timer1 Extended Clock Source Select bits (selected when TCS = 1)
When TCS = 1:
11 = Generic Timer (TMRCK) external input(2)
10 = LPRC Oscillator
01 = T1CK external clock input
00 = SOSC
When TCS = 0:
These bits are ignored; the timer is clocked from the internal system clock (FOSC/2).

bit 7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **Unimplemented:** Read as '0'

Note 1: Changing the value of T1CON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

2: The TMRCK input must also be assigned to an available RPn or RPIn pin. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

REGISTER 14-3: CCPxCON2L: CCPx CONTROL 2 LOW REGISTERS

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0
PWMRSEN	ASDGM	—	SSDG	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ASDG7	ASDG6	ASDG5	ASDG4	ASDG3	ASDG2	ASDG1	ASDG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PWMRSEN:** CCPx PWM Restart Enable bit
- 1 = ASEVT bit clears automatically at the beginning of the next PWM period, after the shutdown input has ended
- 0 = ASEVT bit must be cleared in software to resume PWM activity on output pins

bit 14 **ASDGM:** CCPx Auto-Shutdown Gate Mode Enable bit
- 1 = Waits until the next Time Base Reset or rollover for shutdown to occur
- 0 = Shutdown event occurs immediately

bit 13 **Unimplemented:** Read as '0'

bit 12 **SSDG:** CCPx Software Shutdown/Gate Control bit
- 1 = Manually forces auto-shutdown, timer clock gate or input capture signal gate event (setting of ASDGM bit still applies)
- 0 = Normal module operation

bit 11-8 **Unimplemented:** Read as '0'

bit 7-0 **ASDG<7:0>:** CCPx Auto-Shutdown/Gating Source Enable bits
- 1 = ASDGx Source n is enabled (see Table 14-7 for auto-shutdown/gating sources)
- 0 = ASDGx Source n is disabled

TABLE 14-7: AUTO-SHUTDOWN AND GATING SOURCES

ASDG<x> Bit	Auto-Shutdown/Gating Source						
	MCCP1	SCCP2	SCCP3	SCCP4	SCCP5	SCCP6	SCCP7
0	Comparator 1 Output						
1	Comparator 2 Output						
2	Comparator 3 Output						
3	SCCP4 Output Compare			MCCP1 Output Compare			
4	SCCP5 Output Compare			SCCP2 Output Compare			
5	CLC1 Output	CLC2 Output	CLC3 Output	CLC1 Output	CLC2 Output	CLC3 Output	CLC4 Output
6	OCFA Fault Input						
7	OCFB Fault Input						

REGISTER 22-2: LCDREG: LCD CHARGE PUMP CONTROL REGISTER

RW-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
CPEN	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	RW-0	RW-0
—	—	—	—	—	—	CKSEL1	CKSEL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **CPEN:** 3.6V Charge Pump Enable bit
1 = The regulator generates the highest (3.6V) voltage
0 = Highest voltage in the system is supplied externally (AVDD)

bit 14-2 **Unimplemented:** Read as ‘0’

bit 1-0 **CLKSEL<1:0>:** Regulator Clock Select Control bits
11 = SOSC
10 = 8 MHz FRC
01 = 31 kHz LPRC
00 = Disables regulator and floats regulator voltage output

REGISTER 25-5: CFGPAGE: SECURE ARRAY CONFIGURATION BITS (OTP PAGE 0) REGISTER

r-x	R/PO-x	R/P-x	R/P-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x
—	TSTPGM(1)	KEYSZRAM1	KEYSZRAM0	KEY4TYPE1	KEY4TYPE0	KEY3TYPE1	KEY3TYPE0
bit 31							bit 24

R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x
KEY2TYPE1	KEY2TYPE0	KEY1TYPE1	KEY1TYPE0	SKEYEN	LKYSRC7	LKYSRC6	LKYSRC5
bit 23							bit 16

R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x
LKYSRC4	LKYSRC3	LKYSRC2	LKYSRC1	LKYSRC0	SRCLCK	WRLOCK8	WRLOCK7
bit 15							bit 8

R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x
WRLOCK6	WRLOCK5	WRLOCK74	WRLOCK3	WRLOCK2	WRLOCK1	WRLOCK0	SWKYDIS
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	PO = Program Once bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** Do not modify

bit 30 **TSTPGM:** Customer Program Test bit(1)
1 = CFGPAGE has been programmed
0 = CFGPAGE has not been programmed

bit 29-28 **KEYSZRAM<1:0>:** Key Type Selection bits (Key RAM Pages)
11 = Keys in these pages are 192/256-bit AES operations only
10 = Keys in these pages are 128-bit AES operations only
01 = Keys in these pages are DES3 operations only
00 = Keys in these pages are DES/DES2 operations only

bit 27-26 **KEY4TYPE<1:0>:** Key Type for OTP Pages 7 and 8 bits
11 = Keys in these pages are for 192-bit/256-bit AES operations only
10 = Keys in these pages are for 128-bit AES operations only
01 = Keys in these pages are for 3DES operations only
00 = Keys in these pages are for DES/2DES operations only

bit 25-24 **KEY3TYPE<1:0>:** Key Type for OTP Pages 5 and 6 bits
11 = Keys in these pages are for 192-bit/256-bit AES operations only
10 = Keys in these pages are for 128-bit AES operations only
01 = Keys in these pages are for 3DES operations only
00 = Keys in these pages are for DES/2DES operations only

bit 23-22 **KEY2TYPE<1:0>:** Key Type for OTP Pages 3 and 4 bits
11 = Keys in these pages are for 192-bit/256-bit AES operations only
10 = Keys in these pages are for 128-bit AES operations only
01 = Keys in these pages are for 3DES operations only
00 = Keys in these pages are for DES/2DES operations only

Note 1: This bit’s state is mirrored by the PGMTST bit (CRYOTP<7>).

REGISTER 33-12: FBOOT: BOOT MODE CONFIGURATION WORD

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 15							bit 8

U-1	U-1	U-1	U-1	U-1	U-1	R/PO-1	R/PO-1
—	—	—	—	—	—	BTMOD<1:0>	
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-2 **Unimplemented:** Read as ‘1’

bit 1-0 **BTMOD<1:0>:** Boot Mode Select bits
11 = Standard (Single Partition Flash) mode
10 = Dual Partition Flash mode
01 = Protected Dual Partition Flash mode
00 = Reserved, do not use