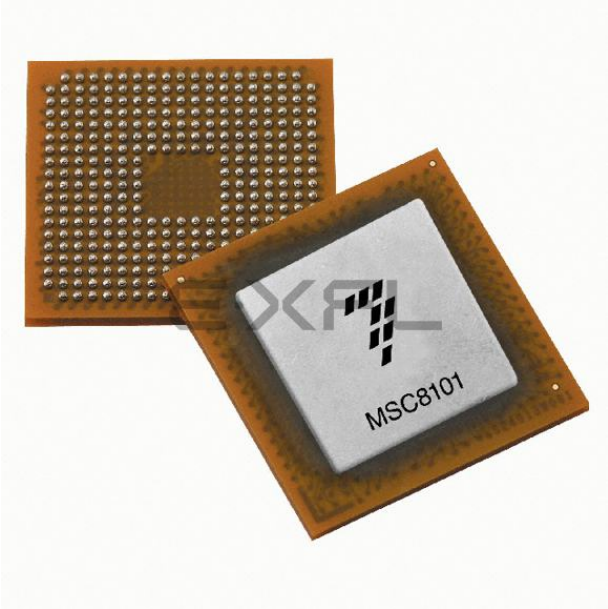


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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Obsolete |
| Type | SC140 Core |
| Interface | Communications Processor Module (CPM) |
| Clock Rate | 275MHz |
| Non-Volatile Memory | External |
| On-Chip RAM | 512kB |
| Voltage - I/O | 3.30V |
| Voltage - Core | 1.60V |
| Operating Temperature | -40°C ~ 105°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 332-BFBGA, FCBGA |
| Supplier Device Package | 332-FCBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8103vt1100f |

# Target Applications

The MSC8103 targets applications requiring very high performance, very large amounts of internal memory, and such networking capabilities as:

- Third-generation wideband wireless infrastructure systems
- Packet Telephony systems
- Multi-channel modem banks
- Multi-channel xDSL

# Product Documentation

The documents listed in **Table 1** are required for a complete description of the MSC8103 and are necessary to design properly with the part. Documentation is available from the following sources (see back cover for details):

- A local Freescale distributor
- A Freescale Semiconductor sales office
- A Freescale Semiconductor Literature Distribution Center
- The world wide web (WWW)

**Table 1.** MSC8103 Documentation

| Name | Description | Order Number |
|---|---|---|
| *MSC8103 Technical Data* | MSC8103 features list and physical, electrical, timing, and package specifications | MSC8103/D |
| *MSC8101 User's Guide* | Detailed functional description of the MSC8101 memory configuration, operation, and register programming. All details apply to the MSC8103. | MSC8101UG/D |
| *MSC8103 Reference Manual* | Detailed description of the MSC8103 processor core and instruction set | MSC8103RM/D |
| *SC140 DSP Core Reference Manual* | Detailed description of the SC140 family processor core and instruction set | MNSC140CORE/D |
| *Application Notes* | Documents describing specific applications or optimized device operation including code examples | See the MSC8103 product website |

Although there are eight interrupt request ($\overline{\text{IRQ}}$) connections to the core processor, there are multiple external lines that can connect to these internal signal lines. After reset, the default configuration includes two $\overline{\text{IRQ1}}$ and two $\overline{\text{IRQ7}}$ input lines. The designer must select one line for each required interrupt and reconfigure the other external signal line or lines for alternate functions.

**Table 1-5.** System Bus, HDI16, and Interrupt Signals

| Signal | Data Flow | Description |
|---|---|---|
| A[0–31] | Input/Output | **Address Bus**<br>When the MSC8103 is in external master bus mode, these pins function as the address bus. The MSC8103 drives the address of its internal bus masters and responds to addresses generated by external bus masters. When the MSC8103 is in Internal Master Bus mode, these pins are used as address lines connected to memory devices and are controlled by the MSC8103 memory controller. |
| TT[0–4] | Input/Output | **Bus Transfer Type**<br>The bus master drives these pins during the address tenure to specify the type of transaction. |
| TSIZ[0–3] | Input/Output | **Transfer Size**<br>The bus master drives these pins with a value indicating the number of bytes transferred in the current transaction. |
| $\overline{\text{TBST}}$ | Input/Output | **Bus Transfer Burst**<br>The bus master asserts this pin to indicate that the current transaction is a burst transaction (transfers four quad words). |
| $\overline{\text{IRQ1}}$ | Input | **Interrupt Request 1**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| $\overline{\text{GBL}}$ | Input/Output | **Global**[1]<br>When a master within the chip initiates a bus transaction, it drives this pin. When an external master initiates a bus transaction, it should drive this pin. Assertion of this pin indicates that the transfer is global and it should be snooped by caches in the system. |
| Reserved | Output | The primary configuration is reserved. |
| BADDR29 | Output | **Burst Address 29**[1]<br>One of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8103 memory controller. |
| $\overline{\text{IRQ2}}$ | Input | **Interrupt Request 2**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| Reserved | Output | The primary configuration is reserved. |
| BADDR30 | Output | **Burst Address 30**[1]<br>One of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8103 memory controller. |
| $\overline{\text{IRQ3}}$ | Input | **Interrupt Request 3**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| Reserved | Output | The primary configuration is reserved. |
| BADDR31 | Output | **Burst Address 31**[1]<br>One of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8103 memory controller. |
| $\overline{\text{IRQ5}}$ | Input | **Interrupt Request 5**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |

**Table 1-5.** System Bus, HDI16, and Interrupt Signals (Continued)

| Signal | Data Flow | Description |
|---|---|---|
| D[32–47] | Input/Output | **Data Bus Bits 32–47**<br>In write transactions the bus master drives the valid data on this bus. In read transactions the slave drives the valid data on this bus. |
| HD[0–15] | Input/Output | **Host Data**[2]<br>When the HDI16 interface is enabled, these signals are lines 0-15 of the bidirectional tri-state data bus. |
| D[48–51] | Input/Output | **Data Bus Bits 48–51**<br>In write transactions the bus master drives the valid data on these pins. In read transactions the slave drives the valid data on these pins. |
| HA[0–3] | Input | **Host Address Line 0–3**[3]<br>When the HDI16 interface bus is enabled, these lines address internal host registers. |
| D52 | Input/Output | **Data Bus Bit 52**<br>In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin. |
| $\overline{\text{HCS1}}$ | Input | **Host Chip Select**[3]<br>When the HDI16 interface is enabled, this is one of the two chip-select pins. The HDI16 chip select is a logical OR of $\overline{\text{HCS1}}$ and $\overline{\text{HCS2}}$. |
| D53 | Input/Output | **Data Bus Bit 53**<br>In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin. |
| HRW | Input | **Host Read Write Select**[3]<br>When the HDI16 interface is enabled in Single Strobe mode, this is the read/write input (HRW). |
| $\overline{\text{HRD}}$/HRD | Input | **Host Read Strobe**[3]<br>When the HDI16 is programmed to interface with a double data strobe host bus, this pin is the read data strobe Schmitt trigger input ($\overline{\text{HRD}}$/HRD). The polarity of the data strobe is programmable. |
| D54 | Input/Output | **Data Bus Bit 54**<br>In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin. |
| $\overline{\text{HDS}}$/HDS | Input | **Host Data Strobe**[3]<br>When the HDI16 is programmed to interface with a single data strobe host bus, this pin is the data strobe Schmitt trigger input ($\overline{\text{HDS}}$/HDS). The polarity of the data strobe is programmable. |
| $\overline{\text{HWR}}$/HWR | Input | **Host Write Data Strobe**[3]<br>When the HDI16 is programmed to interface with a double data strobe host bus, this pin is the write data strobe Schmitt trigger input ($\overline{\text{HWR}}$/HWR). The polarity of the data strobe is programmable. |
| D55 | Input/Output | **Data Bus Bit 55**<br>In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin. |
| $\overline{\text{HREQ}}$/HREQ | Output | **Host Request**[3]<br>When the HDI16 is programmed to interface with a single host request host bus, this pin is the host request output ($\overline{\text{HREQ}}$/HREQ). The polarity of the host request is programmable. The host request may be programmed as a driven or open-drain output. |
| $\overline{\text{HTRQ}}$/HTRQ | Output | **Transmit Host Request**[3]<br>When the HDI16 is programmed to interface with a double host request host bus, this pin is the transmit host request output ($\overline{\text{HTRQ}}$/HTRQ). The signal can be programmed as driven or open drain. The polarity of the host request is programmable. |

**Table 1-5.** System Bus, HDI16, and Interrupt Signals (Continued)

| Signal | Data Flow | Description |
|---|---|---|
| IRQ5 | Input | **Interrupt Request 5**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| DP5 | Input/Output | **Data Parity 5**[1]<br>The agent that drives the data bus also drives the data parity signals. The value driven on the data parity five pin should give odd parity (odd number of ones) on the group of signals that includes data parity 5 and D[40–47]. |
| DREQ4 | Input | **DMA Request 4**[1]<br>An external peripheral uses this pin to request DMA service. |
| EXT_DBG3 | Output | **External Data Bus Grant 3**[1,2]<br>The MSC8103 asserts this pin to grant data bus ownership to an external bus master. |
| IRQ6 | Input | **Interrupt Request 6**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| DP6 | Input/Output | **Data Parity 6**[1]<br>The agent that drives the data bus also drives the data parity signals. The value driven on the data parity six pin should give odd parity (odd number of ones) on the group of signals that includes data parity 6 and D[48–55]. |
| DACK3 | Output | **DMA Acknowledge 3**[1]<br>The DMA controller drives this output to acknowledge the DMA transaction on the bus. |
| IRQ7 | Input | **Interrupt Request 7**[1]<br>One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. |
| DP7 | Input/Output | **Data Parity 7**[1]<br>The master or slave that drives the data bus also drives the data parity signals. The value driven on the data parity seven pin should give odd parity (odd number of ones) on the group of signals that includes data parity 7 and D[56–63]. |
| DACK4 | Output | **DMA Acknowledge**[1]<br>The DMA controller drives this output to acknowledge the DMA transaction on the bus. |
| TA | Input/Output | **Transfer Acknowledge**<br>Indicates that a data beat is valid on the data bus. For single beat transfers, assertion of TA indicates the termination of the transfer. For burst transfers, TA is asserted four times to indicate the transfer of four data beats with the last assertion indicating the termination of the burst transfer. |
| TEA | Input/Output | **Transfer Error Acknowledge**<br>Indicates a bus error. masters within the MSC8103 monitor the state of this pin. The MSC8103 internal bus monitor can assert this pin if it identifies a bus transfer that is hung. |
| NMI | Input | **Non-Maskable Interrupt**<br>When an external device asserts this line, the MSC8103 NMI input is asserted. |
| NMI_OUT | Output | **Non-Maskable Interrupt**<br>Driven from the MSC8103 internal interrupt controller. Assertion of this output indicates that a non-maskable interrupt, pending in the MSC8103 internal interrupt controller, is waiting to be handled by an external host. |
| PSDVAL | Input/Output | **Data Valid**<br>Indicates that a data beat is valid on the data bus. The difference between the TA pin and PSDVAL is that the TA pin is asserted to indicate data transfer terminations while the PSDVAL signal is asserted with each data beat movement. Thus, when TA is asserted, PSDVAL is asserted, but when PSDVAL is asserted, TA is not necessarily asserted. For example when the SDMA initiates a double word (2x64 bits) transfer to a memory device that has a 32-bit port size, PSDVAL is asserted three times without TA, and finally both pins are asserted to terminate the transfer. |

**Table 1-7.** Port A Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| General-Purpose I/O | Peripheral Controller: Dedicated Signal *Protocol* | | |
| PA17 | FCC1: RXD7<br>*UTOPIA* | Input | **FCC1: UTOPIA Receive Data Bit 7.**<br>The MSC8103 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted. |
| | FCC1: RXD0<br>*MII* and *HDLC nibble* | Input | **FCC1: MII and HDLC Nibble Receive Data Bit 0**<br>RXD[3–0] is supported by MII and HDLC nibble mode in FCC1. RXD0 is the least significant bit. |
| | FCC1: RXD<br>*HDLC serial* and *transparent* | Input | **FCC1: HDLC Serial and Transparent Receive Data Bit**<br>This is the single receive data bit supported by HDLC and transparent modes. |
| PA16 | FCC1: RXD6<br>*UTOPIA* | Input | **FCC1: UTOPIA Receive Data Bit 6.**<br>The MSC8103 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. This is bit 6 of the receive data. RXD7 is the most significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted. |
| | FCC1: RXD1<br>*MII* and *HDLC nibble* | Input | **FCC1: MII and HDLC Nibble Receive Data Bit 1**<br>This is bit 1 of the receive nibble data. RXD3 is the most significant bit. |
| PA15 | FCC1: RXD5<br>*UTOPIA* | Input | **FCC1: UTOPIA Receive Data Bit 5**<br>The MSC8103 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. This is bit 5 of the receive data. RXD7 is the most significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted. |
| | RXD2<br>*MII* and *HDLC nibble* | Input | **FCC1: MII and HDLC Nibble Receive Data Bit 2**<br>This is bit 2 of the receive nibble data. RXD3 is the most significant bit. |
| PA14 | FCC1: RXD4<br>*UTOPIA* | Input | **FCC1: UTOPIA Receive Data Bit 4.**<br>The MSC8103 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted. |
| | FCC1: RXD3<br>*MII* and *HDLC nibble* | Input | **FCC1: MII and HDLC Nibble Receive Data Bit 3**<br>RXD3 is the most significant bit of the receive nibble bit. |
| PA13 | FCC1: RXD3<br>*UTOPIA* | Input | **FCC1: UTOPIA Receive Data Bit 3**<br>The MSC8103 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted. |
| | SDMA: MSNUM2 | Output | **Module Serial Number Bit 2**<br>The MSNUM has 6 bits that identify devices using the serial DMA (SDMA) modules. MSNUM[0–4] is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates the section, transmit (0) or receive (1), that is active during the transfer. The information is recorded in the SDMA transfer error registers. |

**Table 1-8.** Port B Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| **General-Purpose I/O** | **Peripheral Controller: Dedicated I/O *Protocol*** | | |
| PB28 | FCC2: RTS<br>*HDLC serial*, *HDLC nibble*, and *transparent* | Output | **FCC2: Request to Send**<br>One of the standard modem interface signals supported by FCC2 (RTS, CTS, and CD). RTS is asynchronous with the data. RTS is typically used in conjunction with CD. The MSC8103 FCC2 transmitter requests the receiver to send data by asserting RTS low. The request is accepted when CTS is returned low. |
| | FCC2: RX_ER<br>*MII* | Input | **FCC2: Media Independent Interface Receive Error**<br>Asserted by an external fast Ethernet PHY to indicate a receive error, which often indicates bad wiring. |
| | SCC2: RTS, TENA | Output | **SCC2: Request to Send, Transmit Enable**<br>Typically used in conjunction with CD supported by SCC2. The MSC8103 SCC2 transmitter requests the receiver to send data by asserting RTS low. The request is accepted when CTS is returned low. TENA is the signal used in Ethernet mode. |
| | SI2 TDMB2: L1TSYNC<br>*TDM serial* | Input | **Time-Division Multiplexing B2: Layer 1 Transmit Synchronization**<br>The synchronizing signal for the transmit channel. See the serial interface with time-slot assigner chapter in the *MSC8103 Reference Manual*. |
| PB27 | FCC2: COL<br>*MII* | Input | **FCC2: Media Independent Interface Collision Detect**<br>Asserted by an external fast Ethernet PHY when a collision is detected. |
| | SI2 TDMC2: L1TXD<br>*TDM serial* | Output | **Time-Division Multiplexing C2: Layer 1 Transmit Data**<br>TDMC2 transmits serial data out of L1TXD. |
| PB26 | FCC2: CRS<br>*MII* | Input | **FCC2: Media Independent Interface Carrier Sense Input**<br>Asserted by an external fast Ethernet PHY to indicate activity on the cable. |
| | SI2 TDMC2: L1RXD<br>*TDM serial* | Input | **Time-Division Multiplexing C2: Layer 1 Receive Data**<br>TDMC2 receives serial data from L1RXD. |
| PB25 | FCC2: TXD3<br>*MII* and *HDLC nibble* | Output | **FCC2: MII and HDLC Nibble Transmit Data Bit 3**<br>TXD3 is bit 3 and the most significant bit of the transmit data nibble. |
| | SI1 TDMA1: L1TXD3<br>*TDM nibble* | Output | **Time-Division Multiplexing A1: Nibble Layer 1 Transmit Data Bit 3**<br>L1TXD3 is bit 3 and the most significant bit of the transmit data nibble. |
| | SI2 TDMC2: L1TSYNC<br>*TDM serial* | Input | **Time-Division Multiplexing C2: Layer 1 Transmit Synchronization**<br>The synchronizing signal for the transmit channel. See the *Serial Interface with Time-Slot Assigner* chapter in the *MSC8103 Reference Manual*. |
| PB24 | FCC2: TXD2<br>*MII* and *HDLC nibble* | Output | **FCC2: MII and HDLC Nibble: Transmit Data Bit 2**<br>TXD2 is bit 2 of the transmit data nibble. |
| | SI1 TDMA1: L1RXD3<br>*nibble* | Input | **Time-Division Multiplexing A1: Nibble Layer 1 Receive Data Bit 3**<br>L1RXD3 is bit 3 and the most significant bit of the receive data nibble. |
| | SI2 TDMC2: L1RSYNC<br>*serial* | Input | **Time-Division Multiplexing C2: Layer 1 Receive Synchronization**<br>The synchronizing signal for the receive channel. |

**Table 1-9.** Port C Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| **General-Purpose I/O** | **Peripheral Controller: Dedicated I/O *Protocol*** | | |
| PC22 | SI1: L1ST1 | Output | **Serial Interface 1: Layer 1 Strobe 1**<br>The MSC8103 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control. |
| | CLK10 | Input | **Clock 10**<br>The CPM supports up to 10 clock input pins sent to the bank-of-clocks selection logic, where they can be routed to the controllers. |
| | DMA: DREQ1 | Input/ Output | **DMA: Request 1**<br>DACK1, DREQ1, DRACK1, and DONE1 belong to the SIU DMA controller. DONE1 and DRACK1 are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports. |
| PC15 | SMC2: SMTXD | Output | **SMC2: Serial Management Transmit Data**<br>The SMC interface consists of SMTXD, SMRXD, SMSYN, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that support three protocols or modes: UART, transparent, or general-circuit interface (GCI). See also PA9. |
| | SCC1: CTS/CLSN | Input | **SCC1: Clear To Send, Collision**<br>Typically used in conjunction with RTS. The MSC8103 SCC1 transmitter sends out a request to send data signal (RTS). The request is accepted when CTS is returned low. CLSN is the signal used in Ethernet mode. See also PC29. |
| | FCC1: TXADDR0<br>*UTOPIA master* | Output | **FCC1: UTOPIA Master Transmit Address Bit 0**<br>This is master transmit address bit 0. |
| | FCC1: TXADDR0<br>*UTOPIA slave* | Input | **FCC1: UTOPIA Slave Transmit Address Bit 0**<br>This is slave transmit address bit 0. |
| PC14 | SI1: L1ST2 | Output | **Serial Interface 1: Layer 1 Strobe 2**<br>The MSC8103 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also be generate output wave forms for such applications as stepper-motor control. |
| | SCC1: CD, RENA | Input | **SCC1: Carrier Detect, Receive Enable**<br>Typically used in conjunction with RTS supported by SCC1. The MSC8103MSC8103 SCC1 transmitter requests the receiver to send data by asserting RTS low. The request is accepted when CTS is returned low. |
| | FCC1: RXADDR0<br>*UTOPIA master* | Output | **FCC1: UTOPIA Multi-PHY Master Receive Address Bit 0**<br>This is master receive address bit 0. |
| | FCC1: RXADDR0<br>*UTOPIA slave* | Input | **FCC1: UTOPIA Multi-PHY Slave Receive Address Bit 0**<br>This is slave receive address bit 0. |

**Table 1-10.** Port D Signals (Continued)

| Name | | Dedicated I/O Data Direction | Description |
|---|---|---|---|
| General-Purpose I/O | Peripheral Controller: Dedicated I/O *Protocol* | | |
| PD19 | FCC1: TXADDR4<br>*UTOPIA master* | Output | **FCC1: Multi-PHY Master Transmit Address Bit 4 Multiplexed Polling**<br>This is master transmit address bit 4. |
| | FCC1: TXADDR4<br>*UTOPIA slave* | Input | **FCC1: UTOPIA Slave Transmit Address Bit 4**<br>This is slave transmit address bit 4. |
| | FCC1: TXCLAV3<br>*UTOPIA multi-PHY master, direct polling* | Input | **FCC1: UTOPIA Multi-PHY master Transmit Cell Available 3 Direct Polling**<br>Asserted by an external UTOPIA slave PHY to indicate that it can accept one complete ATM cell. |
| | BRG1O | Output | **Baud Rate Generator 1 Output**<br>The CPM supports up to 8 BRGs for use internally by the bank-of-clocks selection logic and/or to provide an output to one of the 8 BRG pins. BRG1O can be the internal input to the SIU timers. When CLK5 is selected (see PC27 above), it is the source for BRG1O which is the default input for the SIU timers. See the system interface unit (SIU) chapter in the *MSC8103 Reference Manual* for additional information. If CLK5 is not enabled, BRG1O uses an internal input. If TMCLK is enabled (see PC26 above), the BRG1O input to the SIU timers is disabled. |
| | SPI: $\overline{\text{SPISEL}}$ | Input | **SPI: Select**<br>The SPI interface comprises four signals: master out slave in ($\overline{\text{SPIMOSI}}$), master in slave out (SPIMISO), clock (SPICLK) and select ($\overline{\text{SPISEL}}$). The SPI can be configured as a slave or master in single- or multiple-master environments. $\overline{\text{SPISEL}}$ is the enable input to the SPI slave. In a multimaster environment, $\overline{\text{SPISEL}}$ (always an input) detects an error when more than one master is operating. SPI masters must output a slave select signal to enable SPI slave devices by using a separate general-purpose I/O signal. Assertion of an SPI $\overline{\text{SPISEL}}$ while it is master causes an error. |
| PD18 | FCC1: RXADDR4<br>*UTOPIA master* | Output | **FCC1: UTOPIA Master Receive Address Bit 4**<br>This is master receive address bit 4. |
| | FCC1: RXADDR4<br>*UTOPIA slave* | Input | **FCC1: UTOPIA Slave Receive Address Bit 4**<br>This is slave receive address bit 4. |
| | FCC1: RXCLAV3<br>*UTOPIA multi-PHY master, direct polling* | Input | **FCC1: UTOPIA Multi-PHY Master Receive Cell Available 3 Direct Polling**<br>Asserted by an external PHY when one complete ATM cell is available for transfer. |
| | SPI: SPICLK | Input/ Output | **SPI: Clock**<br>The SPI interface comprises four signals: master out slave in (SPIMOSI), master in slave out (SPIMISO), clock (SPICLK) and select (SPISEL). The SPI can be configured as a slave or master in single- or multiple-master environments. SPICLK is a gated clock, active only during data transfers. Four combinations of SPICLK phase and polarity can be configured. When the SPI is a master, SPICLK is the clock output signal that shifts received data in from SPIMISO and transmitted data out to SPIMOSI. |

# Physical and Electrical Specifications 2

This document contains detailed information on environmental limits, power considerations, DC/AC electrical characteristics, and AC timing specifications for the MSC8103 communications processor, mask set 2K87M. For additional information, see the *MSC8103 Reference Manual*.

## 2.1 Absolute Maximum Ratings

**CAUTION**

**This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or $V_{CC}$).**

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist. **Table 2-1** describes the maximum electrical ratings for the MSC8103.

**Table 2-1.** Absolute Maximum Ratings[2]

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Core supply voltage[3] | $V_{DD}$ | –0.2 to 1.7 | V |
| PLL supply voltage[3] | $V_{CCSYN}$ | –0.2 to 1.7 | V |
| I/O supply voltage[3] | $V_{DDH}$ | –0.2 to 3.6 | V |
| Input voltage[3] | $V_{IN}$ | (GND – 0.2) to 3.6 | V |
| Maximum operating temperature range[4] | $T_J$ | –40 to 120 | °C |
| Storage temperature range | $T_{STG}$ | –55 to +150 | °C |

**Notes:**
1. Functional operating conditions are given in **Table 2-2.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. The input voltage must not exceed the I/O supply $V_{DDH}$ by more than 2.5 V at any time, including during power-on reset. In turn, $V_{DDH}$ can exceed $V_{DD}/V_{CCSYN}$ by more than 3.3 V during power-on reset, but for no more than 100 ms. $V_{DDH}$ should not exceed $V_{DD}/V_{CCSYN}$ by more than 2.1 V during normal operation. $V_{DD}/V_{CCSYN}$ must not exceed $V_{DDH}$ by more than 0.4 V at any time, including during power-on reset. See **Section 4.2**, *Electrical Design Considerations*, on page **4-1** for more information.
4. **Section 4.1**, *Thermal Design Considerations*, on page **4-1** includes a formula for computing the chip junction temperature ($T_J$).

**Table 2-11.** Clock Ranges

| Clock | Symbol | Maximum Rated Core Frequency | | |
|---|---|---|---|---|
| | | All | Max. Values for SC140 Clock Rating of: | |
| | | Min | 275 MHz | 300 MHz |
| Input Clock | CLKIN | 18 MHz | 91.67 MHz | 100 MHz |
| SPLL MF Clock | SPLLMFCLK | 18 MHz | 34.38 MHz | 37.5 MHz |
| Bus/Output | BCLK<br>CLKOUT | 18 MHz | 91.67 MHz | 100 MHz |
| Serial Communications Controller | SCLK | 35 MHz | 91.67 MHz | 100 MHz |
| Communications Processor Module | CPMCLK | 70 MHz | 183.3 MHz | 200 MHz |
| SC140 Core | DSPCLK | 72 MHz | 275 MHz | 300 MHz |
| Baud Rate Generator<br>• For BRG DF = 4<br>• For BRG DF = 16 (default)<br>• For BRG DF = 64<br>• For BRG DF = 256 | BRGCLK | <br>36 MHz<br>9 MHz<br>2.25 MHz<br>562.5 KHz | <br>91.67 MHz<br>22.91 MHz<br>5.73 MHz<br>1.43 MHz | <br>100 MHz<br>25 MHz<br>6.25 MHz<br>1.56 MHz |

## 2.6.4 Reset Timing

The MSC8103 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)

Asserting an external $\overline{\text{PORESET}}$ causes concurrent assertion of an internal $\overline{\text{PORESET}}$ signal, $\overline{\text{HRESET}}$, and $\overline{\text{SRESET}}$. When the external $\overline{\text{PORESET}}$ signal is deasserted, the MSC8103 samples several configuration pins:

- $\overline{\text{RSTCONF}}$—determines whether the MSC8103 is a master (0) or slave (1) device
- DBREQ—determines whether to operate in normal mode (0) or invoke the SC140 debug mode (1)
- HPE—disable (0) or enable (1) the host port (HDI16)
- BTM[0–1]—boot from external memory (00) or the HDI16 (01)

All these reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the last sources to cause a reset. **Table 2-12** describes reset causes.

**Table 2-12.** Reset Causes

| Name | Direction | Description |
|---|---|---|
| Power-on reset ($\overline{\text{PORESET}}$) | Input | $\overline{\text{PORESET}}$ initiates the power-on reset flow that resets all the MSC8103s and configures various attributes of the MSC8103, including its clock mode. |
| Hard reset ($\overline{\text{HRESET}}$) | Input/Output | The MSC8103 can detect an external assertion of $\overline{\text{HRESET}}$ only if it occurs while the MSC8103 is not asserting reset. During $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$ is asserted. $\overline{\text{HRESET}}$ is an open-drain pin. |
| Soft reset ($\overline{\text{SRESET}}$) | Input/Output | The MSC8103 can detect an external assertion of $\overline{\text{SRESET}}$ only if it occurs while the MSC8103 is not asserting reset. $\overline{\text{SRESET}}$ is an open-drain pin. |

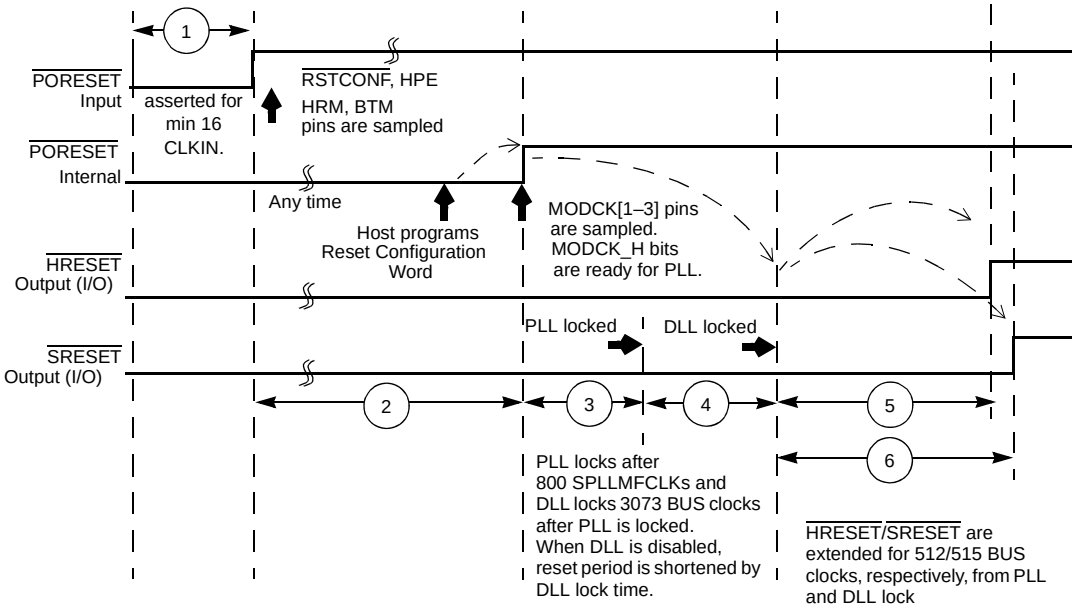


**Figure 2-7.** Host Reset Configuration Timing

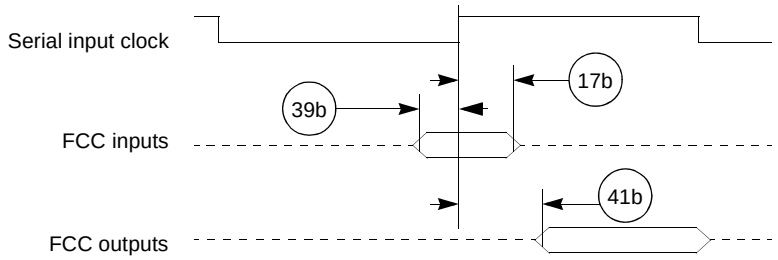


**Figure 2-19.** FCC External Clock Diagram

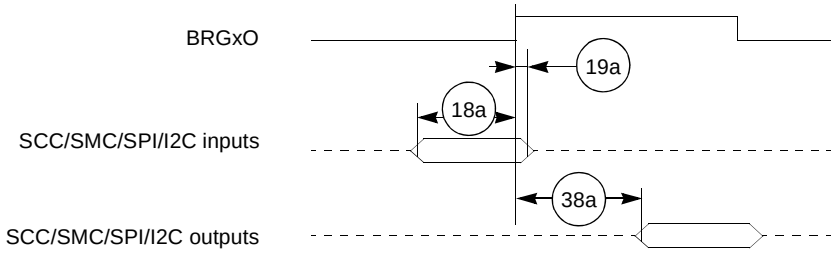


**Figure 2-20.** SCC/SMC/SPI/I$^2$C Internal Clock Diagram

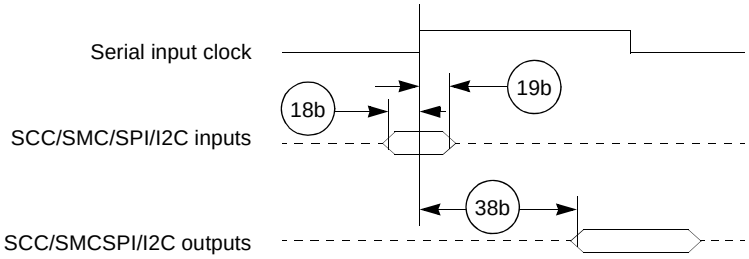


**Figure 2-21.** SCC/SMC/SPI/I$^2$C External Clock Diagram

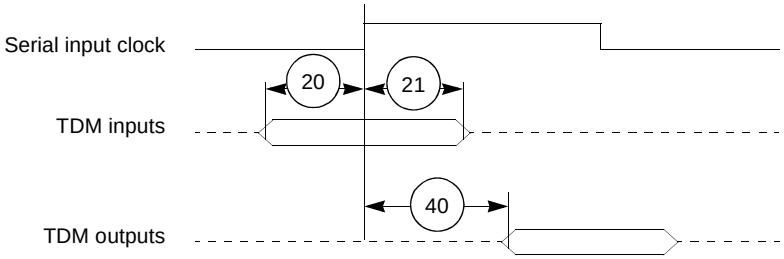


**Figure 2-22.** TDM Signal Diagram

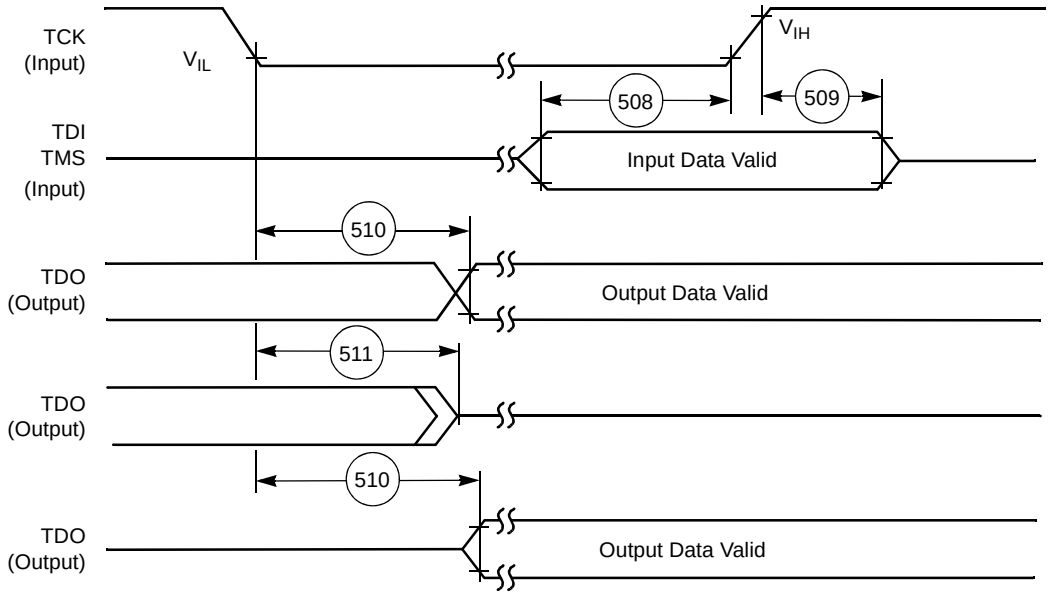


**Figure 2-25.** Test Access Port Timing Diagram

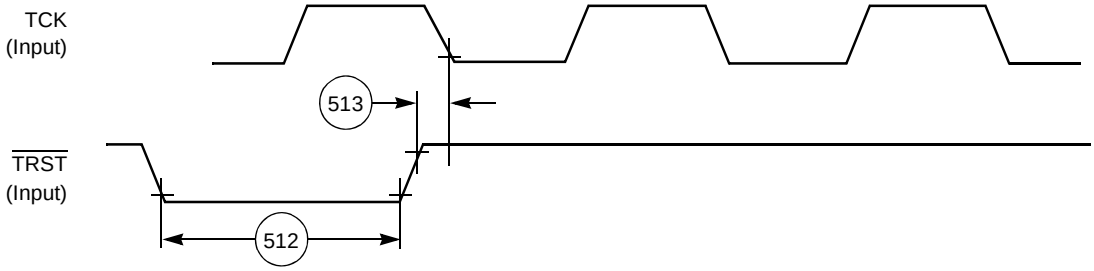


**Figure 2-26.** $\overline{\text{TRST}}$ Timing Diagram

**Table 3-1.** MSC8103 Signal Listing By Name (Continued)

| Signal Name | Number |
|---|---|
| D42 | A12 |
| D43 | D13 |
| D44 | C13 |
| D45 | B13 |
| D46 | A13 |
| D47 | E14 |
| D48 | D14 |
| D49 | C14 |
| D50 | B14 |
| D51 | A14 |
| D52 | D15 |
| D53 | C15 |
| D54 | B15 |
| D55 | A15 |
| D56 | E16 |
| D57 | D16 |
| D58 | C16 |
| D59 | B16 |
| D60 | A16 |
| D61 | C17 |
| D62 | A17 |
| D63 | A18 |
| $\overline{\text{DACK1}}$ | N5 |
| $\overline{\text{DACK2}}$ | N1 |
| $\overline{\text{DACK3}}$ | D5 |
| $\overline{\text{DACK4}}$ | F6 |
| $\overline{\text{DBB}}$ | C18 |
| $\overline{\text{DBG}}$ | B18 |
| DBREQ | D2 |
| DLLIN | P8 |
| DP0 | C2 |
| DP1 | B1 |
| DP2 | D4 |
| DP3 | B2 |

**Table 3-1.** MSC8103 Signal Listing By Name (Continued)

| Signal Name | Number |
|---|---|
| PA18 | W2 |
| PA19 | R5 |
| PA20 | T3 |
| PA21 | U1 |
| PA22 | R3 |
| PA23 | P4 |
| PA24 | P2 |
| PA25 | N2 |
| PA26 | M6 |
| PA27 | L1 |
| PA28 | K1 |
| PA29 | J1 |
| PA30 | J7 |
| PA31 | G1 |
| PB18 | R4 |
| PB19 | U2 |
| PB20 | P5 |
| PB21 | T1 |
| PB22 | T2 |
| PB23 | V1 |
| PB24 | P3 |
| PB25 | N3 |
| PB26 | M3 |
| PB27 | M1 |
| PB28 | L2 |
| PB29 | K4 |
| PB30 | H1 |
| PB31 | H4 |
| $\overline{\text{PBS0}}$ | K18 |
| $\overline{\text{PBS1}}$ | K17 |
| $\overline{\text{PBS2}}$ | K14 |
| $\overline{\text{PBS3}}$ | J19 |
| $\overline{\text{PBS4}}$ | H19 |
| $\overline{\text{PBS5}}$ | D17 |

**Table 3-2.** MSC8103 Signal Listing by Pin Designator (Continued)

| Number | Signal Name |
|---|---|
| C4 | D2 |
| C5 | D5 |
| C6 | D9 |
| C7 | D15 |
| C8 | D20 |
| C9 | D25 |
| C10 | D30 |
| C11 | D35 / HD3 |
| C12 | D40 / HD8 |
| C13 | D44 / HD12 |
| C14 | D49 / HA1 |
| C15 | D53 / HRW / $\overline{\text{HRD}}$ |
| C16 | D58 / HDDS |
| C17 | D61 |
| C18 | $\overline{\text{DBB}}$ / $\overline{\text{IRQ3}}$ |
| C19 | BADDR29 / $\overline{\text{IRQ2}}$ |
| D1 | HPE / EE1 |
| D2 | DBREQ / EE0 |
| D3 | THERM2 |
| D4 | $\overline{\text{IRQ2}}$ / DP2 / $\overline{\text{EXT\_DBG2}}$ |
| D5 | $\overline{\text{IRQ6}}$ / DP6 / $\overline{\text{DACK3}}$ |
| D6 | D8 |
| D7 | D14 |
| D8 | D19 |
| D9 | D24 |
| D10 | D29 |
| D11 | D34 / HD2 |
| D12 | D39 / HD7 |
| D13 | D43 / HD11 |
| D14 | D48 / HA0 |
| D15 | D52 / $\overline{\text{HCS1}}$ |
| D16 | D57 / HDSP |
| D17 | $\overline{\text{PWE5}}$ / $\overline{\text{PSDDQM5}}$ / $\overline{\text{PBS5}}$ |
| D18 | $\overline{\text{IRQ1}}$ / $\overline{\text{GBL}}$ |
| D19 | BADDR27 |
| E1 | BTM0 / EE4 |
| E2 | EE3 |
| E3 | EE2 |
| E4 | $V_{DDH}$ |

**Table 3-2.** MSC8103 Signal Listing by Pin Designator (Continued)

| Number | Signal Name |
|---|---|
| G6 | GND |
| G7 | D12 |
| G8 | GND |
| G9 | D23 |
| G10 | GND |
| G11 | D33 / HD1 |
| G12 | GND |
| G13 | $\overline{\text{PSDVAL}}$ |
| G14 | GND |
| G15 | $V_{DDH}$ |
| G16 | $V_{DDH}$ |
| G17 | $\overline{\text{TEA}}$ |
| G18 | MODCK3 / TC2 / BNKSEL2 |
| G19 | $\overline{\text{POE}}$ / $\overline{\text{PSDRAS}}$ / PGPL2 |
| H1 | PB30 / FCC2:MII:RX_DV / SCC2:TXD / TDBM2:L1RXD |
| H2 | PD31 / SCC1:RXD / $\overline{\text{DRACK1}}$ / $\overline{\text{DONE1}}$ |
| H3 | PC31 / BRG1O / CLK1 / $\overline{\text{TGATE1}}$ |
| H4 | PB31 / FCC2:MII:TX_ER / SCC2:RXD / TDMB2:L1TXD |
| H5 | GND |
| H6 | TDI |
| H7 | GND |
| H13 | Reserved / BADDR31 / $\overline{\text{IRQ5}}$ |
| H14 | Reserved / BADDR30 / $\overline{\text{IRQ3}}$ |
| H15 | GND |
| H16 | $V_{DD}$ |
| H17 | $\overline{\text{BR}}$ |
| H18 | ALE |
| H19 | $\overline{\text{PWE4}}$ / $\overline{\text{PSDDQM4}}$ / $\overline{\text{PBS4}}$ |
| J1 | PA29 / FCC1:UTOPIA8:TXSOC / FCC1:MII:TX_ER |
| J2 | PD30 / SCC1:TXD / DMA:$\overline{\text{DRACK2}}$/$\overline{\text{DONE2}}$ |
| J3 | PC30 / EXT1 / BRG2O / CLK2 / $\overline{\text{TOUT1}}$ |
| J4 | $V_{DD}$ |
| J5 | GND |
| J6 | GND |
| J7 | PA30 / FCC1:UTOPIA8:TXCLAV / FCC1:UTOPIA8:$\overline{\text{TXCLAV0}}$ / FCC1:MII:CRS / FCC1:HDLC and transparent:RTS |
| J13 | $\overline{\text{TA}}$ |
| J14 | GND |
| J15 | $V_{DDH}$ |

**Table 3-2.** MSC8103 Signal Listing by Pin Designator (Continued)

| Number | Signal Name |
|---|---|
| J16 | $V_{DDH}$ |
| J17 | PSDAMUX / PGPL5 |
| J18 | $\overline{\text{PGTA}}$ / PUPMWAIT / $\overline{\text{PPBS}}$ / PGPL4 |
| J19 | $\overline{\text{PWE3}}$ / $\overline{\text{PSDDQM3}}$ / $\overline{\text{PBS3}}$ |
| K1 | PA28 / FCC1:UTOPIA8:$\overline{\text{RXENB}}$ / FCC1:MII:TX_EN |
| K2 | PD29 / FCC1:UTOPIA8:RXADDR3 / FCC1:UTOPIA8:RXCLAV2 / SCC1:$\overline{\text{RTS}}$/TENA |
| K3 | PC29 / SCC1:$\overline{\text{CTS}}$ / SCC1:CLSN / BRG3O / CLK3 / TIN2 |
| K4 | PB29 / FCC2:MII:TX_EN / TDMB2:L1RSYNC |
| K5 | $V_{DDH}$ |
| K6 | GND |
| K7 | GND |
| K13 | GND |
| K14 | $\overline{\text{PWE2}}$ / $\overline{\text{PSDDQM2}}$ / $\overline{\text{PBS2}}$ |
| K15 | GND |
| K16 | $V_{DDH}$ |
| K17 | $\overline{\text{PWE1}}$ / $\overline{\text{PSDDQM1}}$ / $\overline{\text{PBS1}}$ |
| K18 | $\overline{\text{PWE0}}$ / $\overline{\text{PSDDQM0}}$ / $\overline{\text{PBS0}}$ |
| K19 | $\overline{\text{CS2}}$ |
| L1 | PA27 / FCC1:UTOPIA8:RXSOC / FCC1:MII:RX_DV |
| L2 | PB28 / FCC2:RX_ER / FCC2:HDLC:$\overline{\text{RTS}}$ / SCC2:$\overline{\text{RTS}}$/TENA / TDMB2:L1TSYNC |
| L3 | PC28 / SCC2:$\overline{\text{CTS}}$/CLSN / BRG4O / CLK4 / TIN1/$\overline{\text{TOUT2}}$ |
| L4 | $V_{DD}$ |
| L5 | GND |
| L6 | GND |
| L7 | PC27 / CLK5 / BRG5O / $\overline{\text{TGATE2}}$ |
| L13 | $\overline{\text{CS6}}$ |
| L14 | GND |
| L15 | GND |
| L16 | $V_{DD}$ |
| L17 | $\overline{\text{CS1}}$ |
| L18 | $\overline{\text{CS3}}$ |
| L19 | $\overline{\text{BCTL1}}$ |
| M1 | PB27 / FCC2:MII:COL / TDMC2:L1TXD |
| M2 | PC26 / TMCLK / BRG6O / CLK6 / $\overline{\text{TOUT3}}$ |
| M3 | PB26 / FCC2:MII:CRS / TDMC2:L1RXD |
| M4 | $V_{DDH}$ |
| M5 | GND |
| M6 | PA26 / FCC1:UTOPIA8:RXCLAV / FCC1:UTOPIA8:RXCLAV0 / FCC1:MII:RX_ER |

$GND_{SYN}$ and $GND_{SYN1}$ should be provided with an extremely low impedance path to ground and should be bypassed to $V_{CCSYN}$ and $V_{CCSYN1}$, respectively, by a 0.01-µF capacitor located as close as possible to the chip package. The user should also bypass $GND_{SYN}$ and $GND_{SYN1}$ to $V_{CCSYN}$ and $V_{CCSYN1}$ with a 0.01-µF capacitor as closely as possible to the chip package

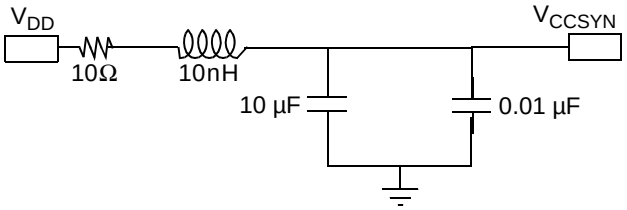


**Figure 4-2.** VCCSYN and VCCSYN1 Bypass