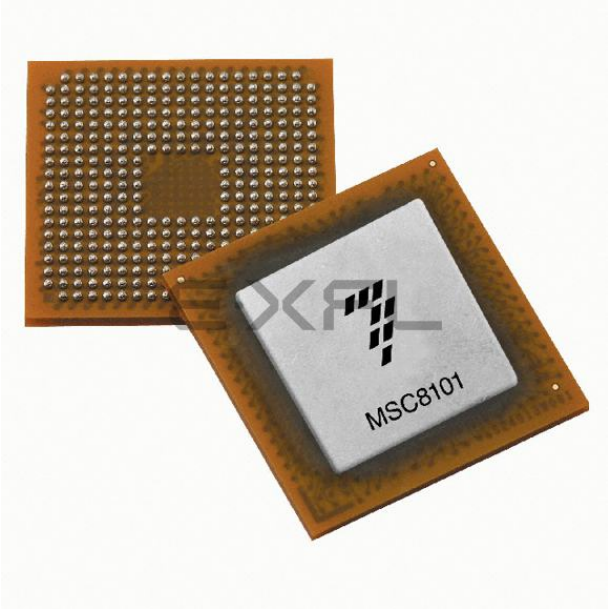

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC140 Core
Interface	Communications Processor Module (CPM)
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	512kB
Voltage - I/O	3.30V
Voltage - Core	1.60V
Operating Temperature	-40°C ~ 75°C (TJ)
Mounting Type	Surface Mount
Package / Case	332-BFBGA, FCBGA
Supplier Device Package	332-FCBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8103vt1200f

MSC8103 Features

- SC140 core
  - Architecture optimized for efficient C/C++ code compilation
  - Four 16-bit ALUs and two 32-bit AGUs
  - 1200 DSP MMACS running at 300 MHz
  - Very low power dissipation
  - Variable-length execution set (VLES) execution model
  - JTAG/Enhanced OnCE debug port
- Communications processor module (CPM)
  - Programmable protocol machine using a 32-bit RISC engine
  - 155 Mbps ATM interface (including AAL 0/1/2/5)
  - 10/100 Mbit Ethernet interface
  - Up to four E1/T1 interfaces or one E3/T3 interface and one E1/T1 interface
  - HDLC support up to T3 rates, or 256 channels
- 64- or 32-bit wide bus interface
  - Support for bursts for high efficiency
  - Glueless interface to 60x-compatible bus systems
  - Multi-master support
- Programmable memory controller
  - Control for up to eight banks of external memory
  - User-programmable machines (UPM) allowing glueless interface to various memory types (SRAM, DRAM, EPROM, and Flash memory) and other user-definable peripherals
  - Dedicated pipelined SDRAM memory interface
- Large internal SRAM
  - 256K 16-bit words (512 KB)
  - Unified program and data space configurable by the application
  - Word and byte addressable
- DMA controller
  - 16 DMA channels, FIFO based, with burst capabilities
  - Sophisticated addressing capabilities
- Small foot print package
  - 17 mm × 17 mm lidded FC-PBGA package with lead-bearing or lead-free spheres
- Very low power consumption
  - Separate power supply for internal logic (1.6 V) and for I/O (3.3 V)
- Enhanced 16-bit parallel host interface (HDI16)
  - Supports a variety of microcontroller, microprocessor, and DSP bus interfaces
- Phase-lock loops (PLLs)
  - System PLL
  - CPM DPLLs (SCC and SCM)
- Process technology
  - 0.13 micron copper interconnect process technology

Signals/Connections 1

The MSC8103 external signals are organized into functional groups, as shown in **Table 1-1**, **Figure 1-1**, and **Figure 1-2**. **Table 1-1** lists the functional groups, states the number of signal connections in each group, and references the table that gives details on multiplexed signals within each group. **Figure 1-1** shows MSC8103 external signals organized by function. **Figure 1-2** indicates how the parallel input/output (I/O) ports signals are multiplexed. Because the parallel I/O design supported by the MSC8103 communications processor module (CPM) is a subset of the parallel I/O signals supported by the MPC8260 device, port pins are not numbered sequentially.

Table 1-1. MSC8103 Functional Signal Groupings

Functional Group		Number of Signal Connections	Detailed Description
Power (V_{CC}, V_{DD}, and GND)		80	**Table 1-2** on page 1-4
Clock		6	**Table 1-3** on page 1-4
Reset, configuration, and EOnCE		11	**Table 1-4** on page 1-5
System bus, HDI16, and interrupts		133	**Table 1-5** on page 1-7
Memory controller		27	**Table 1-6** on page 1-13
CPM input/output parallel ports	Port A	26	**Table 1-7** on page 1-16
	Port B	14	**Table 1-8** on page 1-21
	Port C	18	**Table 1-9** on page 1-24
	Port D	8	**Table 1-10** on page 1-33
JTAG test access port (TAP)		5	**Table 1-11** on page 1-36
Reserved (denotes connections that are always reserved)		5	**Table 1-12** on page 1-36

1.1 Power Signals

Table 1-2. Power and Ground Signal Inputs

Power Name	Description
V_{DD}	**Internal Logic Power** V_{DD} dedicated for use with the device core. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{DD} power rail.
V_{DDH}	**Input/Output Power** This source supplies power for the I/O buffers. The user must provide adequate external decoupling capacitors.
V_{CCSYN}	**System PLL Power** V_{CC} dedicated for use with the system Phase Lock Loop (PLL). The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail.
V_{CCSYN1}	**SC140 PLL Power** V_{CC} dedicated for use with the SC140 core PLL. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail.
GND	**System Ground** An isolated ground for the internal processing logic. This connection must be tied externally to all chip ground connections, except GND_{SYN} and GND_{SYN1}. The user must provide adequate external decoupling capacitors.
GND_{SYN}	**System PLL Ground** Ground dedicated for system PLL use. The connection should be provided with an extremely low-impedance path to ground.
GND_{SYN1}	**SC140 PLL Ground 1** Ground dedicated for SC140 core PLL use. The connection should be provided with an extremely low-impedance path to ground.

1.2 Clock Signals

Table 1-3. Clock Signals

Signal Name	Type	Signal Description
CLKIN	Input	**Clock In** Primary clock input to the MSC8103 PLL.
$\overline{\text{MODCK1}}$	Input	**Clock Mode Input 1** Defines the operating mode of internal clock circuits.
TC0	Output	**Transfer Code 0** Supplies information that can be useful for debugging bus transactions initiated by the MSC8103.
BNKSEL0	Output	**Bank Select 0** Selects the SDRAM bank when the MSC8103 is in 60x-compatible bus mode.
$\overline{\text{MODCK2}}$	Input	**Clock Mode Input 2** Defines the operating mode of internal clock circuits.
TC1	Output	**Transfer Code 1** Supplies information that can be useful for debugging bus transactions initiated by the MSC8103.
BNKSEL1	Output	**Bank Select 1** Selects the SDRAM bank when the MSC8103 is in 60x-compatible bus mode.
$\overline{\text{MODCK3}}$	Input	**Clock Mode Input 3** Defines the operating mode of internal clock circuits.
TC2	Output	**Transfer Code 2** Supplies information that can be useful for debugging bus transactions initiated by the MSC8103.
BNKSEL2	Output	**Bank Select 2** Selects the SDRAM bank when the MSC8103 is in 60x-compatible bus mode.

Table 1-4. Reset, Configuration, and EOnCE Event Signals (Continued)

Signal Name	Type	Signal Description
BTM[0–1]	Input	**Boot Mode 0–1** Determines the MSC8103 boot mode when PORESET is deasserted. See the emulation and debug chapter in the *SC140 DSP Core Reference Manual* for details on how to set these pins.
EE4[1]		**EOnCE Event 4** After PORESET is deasserted, you can configure EE4 as an input (default) or an output. See the emulation and debug chapter in the *SC140 DSP Core Reference Manual* for details on the ETRSMT Register.
	Input	Enable Address Event Detection Channel 4 or generate an EOnCE event.
	Output	The DSP wrote the EOnCE Transmit Register (ETRSMT). Triggers external debugging equipment.
EE5[1]		**EOnCE Event 5** After PORESET is deasserted, you can configure EE5 as an input (default) or an output.
	Input	Enable Address Event Detection Channel 5.
	Output	Detection by Address Event Detection Channel 5. Triggers external debugging equipment.
EED[1]		**Enhanced OnCE (EOnCE) Event Detection** After PORESET is deasserted, you can configure EED as an input (default) or output:
	Input	Enable the Data Event Detection Channel.
	Output	Detection by the Data Event Detection Channel. Triggers external debugging equipment.
PORESET	Input	**Power-On Reset** When asserted, this line causes the MSC8103 to enter power-on reset state.
RSTCONF	Input	**Reset Configuration** Used during reset configuration sequence of the chip. A detailed explanation of its function is provided in the “Power-On Reset Flow” and “Hardware Reset Configuration” sections of the *MSC8103 Reference Manual*.
HRESET	Input	**Hard Reset** When asserted, this open-drain line causes the MSC8103 to enter the hard reset state.
SRESET	Input	**Soft Reset** When asserted, this open-drain line causes the MSC8103 to enter the soft reset state.
Note: See the emulation and debug chapter in the *SC140 DSP Core Reference Manual* for details on how to configure these pins.		

1.4 System Bus, HDI16, and Interrupt Signals

The system bus, HDI16, and interrupt signals are grouped together because they use a common set of signal lines. Individual assignment of a signal to a specific signal line is configured through registers in the System Interface Unit (SIU) and the Host Interface (HDI16). 1-5 describes the signals in this group.

Note: To boot from the host interface, the HDI16 must be enabled by pulling up the HPE signal line during PORESET. The configuration word must then be loaded from the host. The configuration word must set the Internal Space Port Size bit in the Bus Control Register (BCR[ISPS]) to change the system data bus width from 64 bits to 32 bits and reassign the upper 32 bits to their HDI16 functions. Never set the Host Port Enable (HEN) bit in the Host Port Control Register (HPCR) to enable the HDI16, unless the bus size is first changed from 64 bits to 32 bits. Otherwise, unpredictable operation may occur.

Table 1-7. Port A Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	Peripheral Controller: Dedicated Signal *Protocol*		
PA27	FCC1: RXSOC *UTOPIA slave*	Output	**FCC1: UTOPIA Receive Start of Cell** Asserted by the MSC8103 (UTOPIA slave) for an external PHY when RXD[0–7] contains the first valid byte of the cell.
	FCC1: RX_DV *MII*	Input	**FCC1: Media Independent Interface Receive Data Valid** Asserted by an external fast Ethernet PHY to indicate that valid data is being sent. The presence of carrier sense but not RX_DV indicates reception of broken packet headers, probably due to bad wiring or a bad circuit.
PA26	FCC1: RXCLAV *UTOPIA slave*	Output	**FCC1: UTOPIA Slave Receive Cell Available** Asserted by the MSC8103 (UTOPIA slave PHY) when one complete ATM cell is available for transfer.
	FCC1: RXCLAV *UTOPIA master, or*	Input	**FCC1: UTOPIA Master Receive Cell Available** Asserted by an external PHY when one complete ATM cell is available for transfer.
	RXCLAV0 *UTOPIA master, Multi-PHY, direct polling*	Input	**FCC1: UTOPIA Master Receive Cell Available 0 Direct Polling** Asserted by an external PHY when one complete ATM cell is available for transfer.
	FCC1: RX_ER *MII*	Input	**FCC1: Media Independent Interface Receive Error** Asserted by an external fast Ethernet PHY to indicate a receive error, which often indicates bad wiring.
PA25	FCC1: TXD0 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 0** The MSC8103 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.
	SDMA: MSNUM0	Output	**Module Serial Number Bit 0** The MSNUM has 6 bits that identify devices using the serial DMA (SDMA) modules. MSNUM[0–4] is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates the section, transmit (0) or receive (1), that is active during the transfer. The information is recorded in the SDMA transfer error registers.
PA24	FCC1: TXD1 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 1** The MSC8103 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. This is bit 1 of the transmit data. TXD7 is the most significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.
	SDMA: MSNUM1	Output	**Module Serial Number Bit 1** The MSNUM has 6 bits that identify devices using the serial DMA (SDMA) modules. MSNUM[0–4] is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates the section, transmit (0) or receive (1), that is active during the transfer. The information is recorded in the SDMA transfer error registers.
PA23	FCC1: TXD2 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 2** The MSC8103 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. This is bit 2 of the transmit data. TXD7 is the most significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.

Table 1-9. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC5	SMC1: SMTXD	Output	**SMC1: Transmit Data** The SMC interface consists of SMTXD, SMRXD, $\overline{\text{SMSYN}}$, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI).
	SI2: L1ST3	Output	**Serial Interface 2: Layer 1 Strobe 3** The MSC8103 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control.
	FCC2: $\overline{\text{CTS}}$ *HDLC serial*, *HDLC nibble*, and *transparent*	Input	**FCC2: Clear To Send** In the standard modem interface signals supported by FCC2 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$). $\overline{\text{CTS}}$ is asynchronous with the data.
PC4	SMC1: SMRXD	Input	**SMC1: Receive Data** The SMC interface consists of SMTXD, SMRXD, $\overline{\text{SMSYN}}$, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI).
	SI2: L1ST4	Output	**Serial Interface 2: Layer 1 Strobe 4** The MSC8103 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control.
	FCC2: $\overline{\text{CD}}$ *HDLC serial*, *HDLC nibble*, and *transparent*	Input	**FCC2: Carrier Detect** In the standard modem interface signals supported by FCC2 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$ and $\overline{\text{CD}}$). $\overline{\text{CD}}$ is asynchronous with the data.

Table 1-10. Port D Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	Peripheral Controller: Dedicated I/O *Protocol*		
PD19	FCC1: TXADDR4 *UTOPIA master*	Output	**FCC1: Multi-PHY Master Transmit Address Bit 4 Multiplexed Polling** This is master transmit address bit 4.
	FCC1: TXADDR4 *UTOPIA slave*	Input	**FCC1: UTOPIA Slave Transmit Address Bit 4** This is slave transmit address bit 4.
	FCC1: TXCLAV3 *UTOPIA multi-PHY master, direct polling*	Input	**FCC1: UTOPIA Multi-PHY master Transmit Cell Available 3 Direct Polling** Asserted by an external UTOPIA slave PHY to indicate that it can accept one complete ATM cell.
	BRG1O	Output	**Baud Rate Generator 1 Output** The CPM supports up to 8 BRGs for use internally by the bank-of-clocks selection logic and/or to provide an output to one of the 8 BRG pins. BRG1O can be the internal input to the SIU timers. When CLK5 is selected (see PC27 above), it is the source for BRG1O which is the default input for the SIU timers. See the system interface unit (SIU) chapter in the *MSC8103 Reference Manual* for additional information. If CLK5 is not enabled, BRG1O uses an internal input. If TMCLK is enabled (see PC26 above), the BRG1O input to the SIU timers is disabled.
	SPI: $\overline{\text{SPISEL}}$	Input	**SPI: Select** The SPI interface comprises four signals: master out slave in ($\overline{\text{SPIMOSI}}$), master in slave out (SPIMISO), clock (SPICLK) and select ($\overline{\text{SPISEL}}$). The SPI can be configured as a slave or master in single- or multiple-master environments. $\overline{\text{SPISEL}}$ is the enable input to the SPI slave. In a multimaster environment, $\overline{\text{SPISEL}}$ (always an input) detects an error when more than one master is operating. SPI masters must output a slave select signal to enable SPI slave devices by using a separate general-purpose I/O signal. Assertion of an SPI $\overline{\text{SPISEL}}$ while it is master causes an error.
PD18	FCC1: RXADDR4 *UTOPIA master*	Output	**FCC1: UTOPIA Master Receive Address Bit 4** This is master receive address bit 4.
	FCC1: RXADDR4 *UTOPIA slave*	Input	**FCC1: UTOPIA Slave Receive Address Bit 4** This is slave receive address bit 4.
	FCC1: RXCLAV3 *UTOPIA multi-PHY master, direct polling*	Input	**FCC1: UTOPIA Multi-PHY Master Receive Cell Available 3 Direct Polling** Asserted by an external PHY when one complete ATM cell is available for transfer.
	SPI: SPICLK	Input/ Output	**SPI: Clock** The SPI interface comprises four signals: master out slave in (SPIMOSI), master in slave out (SPIMISO), clock (SPICLK) and select (SPISEL). The SPI can be configured as a slave or master in single- or multiple-master environments. SPICLK is a gated clock, active only during data transfers. Four combinations of SPICLK phase and polarity can be configured. When the SPI is a master, SPICLK is the clock output signal that shifts received data in from SPIMISO and transmitted data out to SPIMOSI.

Table 2-14. Reset Timing (Continued)

No.	Characteristics	Expression	Min	Max	Unit
4	Delay from SPLL lock to DLL lock				
	• DLL enabled	3073 / BLCK			
	— BCLK = 18 MHz		170.72		µs
	— BCLK = 75 MHz		40.97		µs
	• DLL disabled	—	0.0		ns
5	Delay from SPLL lock to $\overline{\text{HRESET}}$ deassertion				
	• DLL enabled	3585 / BLCK			
	— BCLK = 18 MHz		199.17		µs
	— BCLK = 75 MHz		47.5		µs
	• DLL disabled	512 / BLCK			
	— BCLK = 18 MHz		28.4		µs
	— BCLK = 75 MHz		6.83		µs
6	Delay from SPLL lock to $\overline{\text{SRESET}}$ deassertion				
	• DLL enabled	3588 / BLCK			
	— BCLK = 18 MHz		199.33		µs
	— BCLK = 75 MHz		47.84		µs
	• DLL disabled	515 / BLCK			
	— BCLK = 18 MHz		28.61		µs
	— BCLK = 75 MHz		6.87		µs

Note: Value given for lowest possible CLKIN frequency 18 MHz to ensure proper initialization of reset sequence.

2.6.4.3 Host Reset Configuration

Host reset configuration allows the host to program the reset configuration word via the Host port after $\overline{\text{PORESET}}$ is deasserted, as described in the *MSC8103 Reference Manual*. The MSC8103 samples the signals described in **Table 2-13** one the rising edge of $\overline{\text{PORESET}}$ when the signal is deasserted.

If HPE is sampled high, the host port is enabled. In this mode the $\overline{\text{RSTCONF}}$ pin *must* be pulled up. The device extends the internal $\overline{\text{PORESET}}$ until the host programs the reset configuration word register. The host must write four 8-bit half-words to the Host Reset Configuration Register address to program the reset configuration word, which is 32 bits wide. For more information, see the *MSC8103 Reference Manual*. The reset configuration word is programmed before the internal PLL and DLL in the MSC8103 are locked. The host must program it after the rising edge of the $\overline{\text{PORESET}}$ input. In this mode, the host must have its own clock that does not depend on the MSC8103 clock. After the PLL and DLL are locked, $\overline{\text{HRESET}}$ remains asserted for another 512 bus clocks and is then released. The $\overline{\text{SRESET}}$ is released three bus clocks later (see **Figure 2-7**).

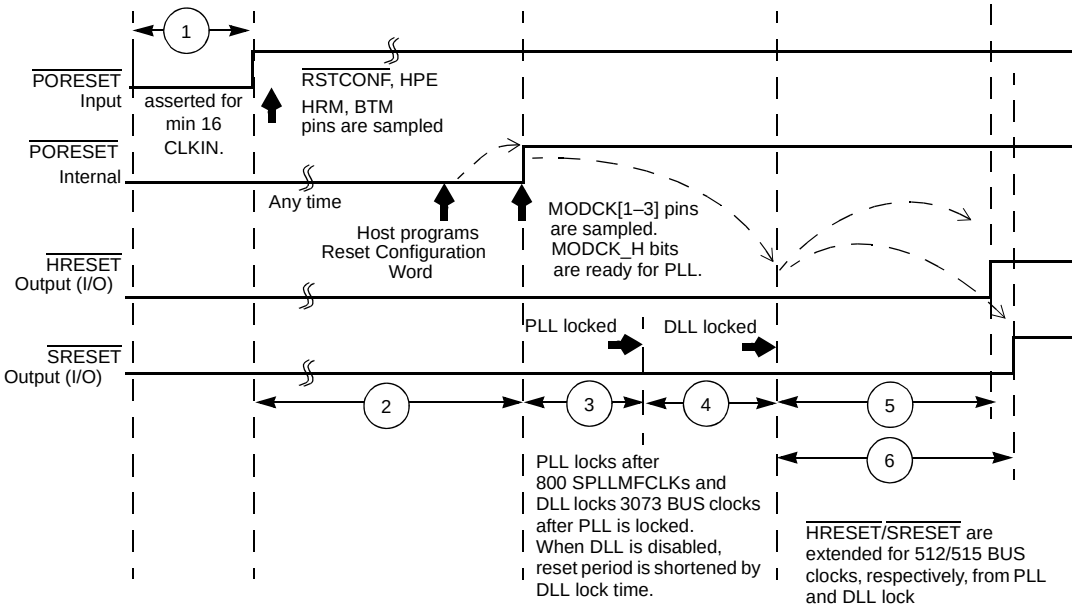

Figure 2-7. Host Reset Configuration Timing

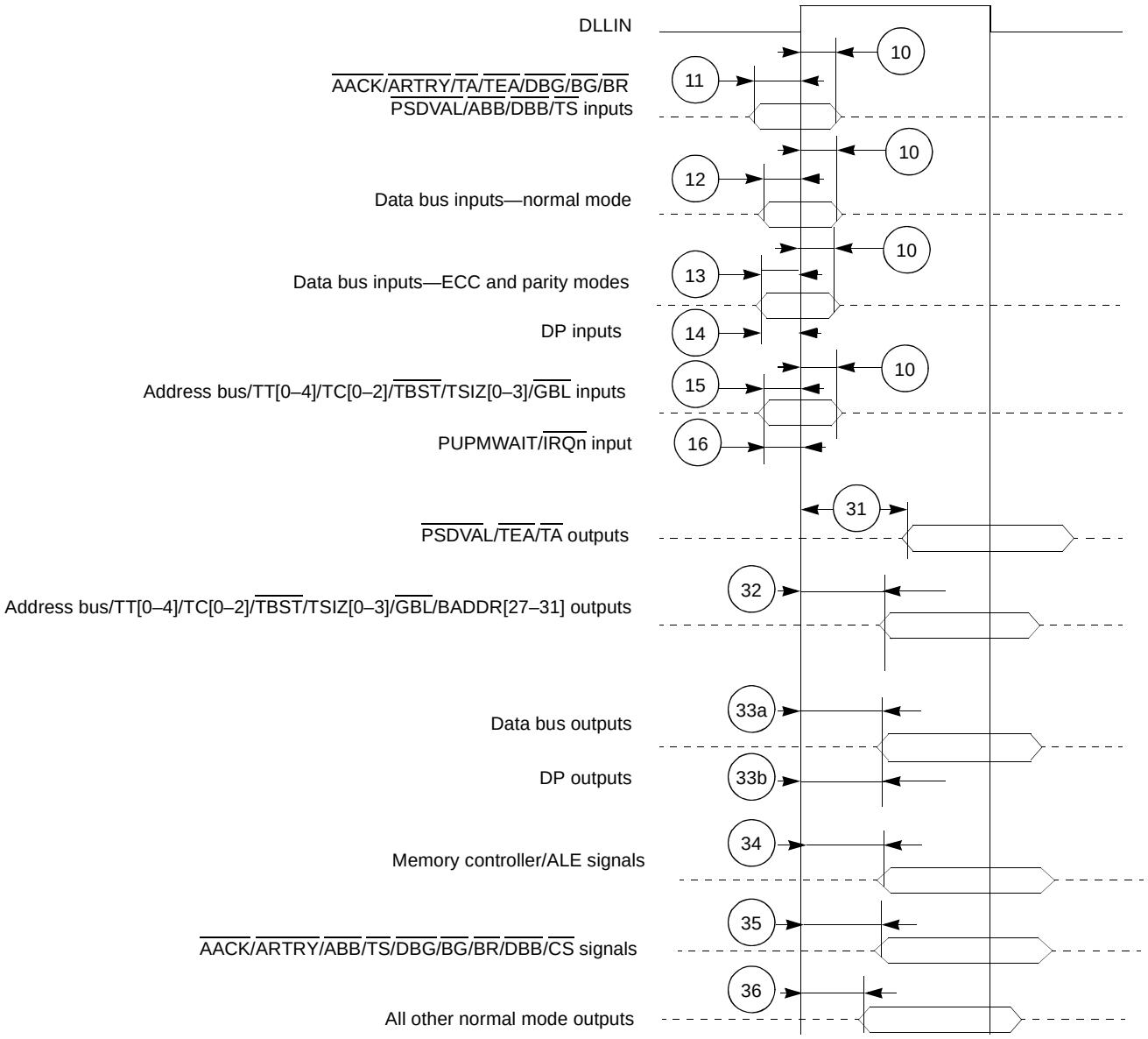

Figure 2-10. Bus Signal Timing

2.6.7 CPM Timings

Table 2-20. CPM Input Characteristics

No.	Characteristic	Typical	Unit
39	FCC input set-up time before low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial clock input)	 10 5	 ns ns
17	FCC input hold time after low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial clock input)	 0 3	 ns ns
18	SCC/SMC/SPI/I^2C input set-up time before low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial clock input)	 20 5	 ns ns
19	SCC/SMC/SPI/I^2C input hold time after low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial clock input)	 0 5	 ns ns
20	TDM input set-up time before low-to-high serial clock transition	5	ns
21	TDM input hold time after low-to-high serial transition	5	ns
22	PIO/TIMER/DMA input set-up time before low-to-high serial clock transition	10	ns
23	PIO/TIMER/DMA input hold time after low-to-high serial clock transition	3	ns
Note:	FCC, SCC, SMC, SPI, I^2C are non-multiplexed serial interface signals.		

Table 2-21. CPM Output Characteristics

No.	Characteristic	Min	Max	Unit
41	FCC output delay after low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial input clock)	 0 2	 6 18	 ns ns
38	SCC/SMC/SPI/I^2C output delay after low-to-high clock transition a. internal clock (BRGxO) b. external clock (serial input clock)	 0 0	 20 30	 ns ns
40	TDM output delay after low-to-high serial clock transition	5	15	ns
42	PIO/TIMER/DMA output delay after low-to-high serial clock transition	1	14	ns
Note:	FCC, SCC, SMC, SPI, I^2C are Non-Multiplexed Serial Interface signals.			

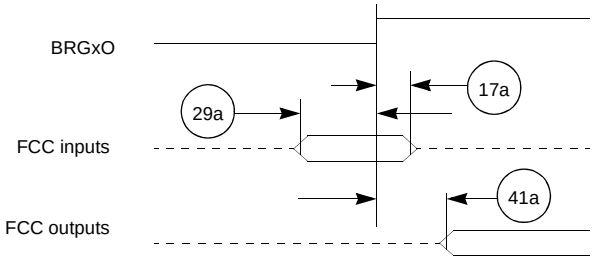

Figure 2-18. FCC Internal Clock Diagram

Packaging 3

This chapter provides information about the MSC8103 package, including diagrams of the package pinouts and tables showing how the signals discussed in **Chapter 1** are allocated. The MSC8103 is available in a 332-pin lidded flip chip-plastic ball grid array (FC-PBGA).

3.1 FC-PBGA Package Description

Figure 3-1 and **Figure 3-2** show top and bottom views of the FC-PBGA package, including pinouts. **Table 3-1** lists the MSC8103 signals alphabetically by signal name. Connections with multiple names are listed individually by each name. Signals with programmable polarity are shown both as signals which are asserted low (default) and high (that is, $\overline{\text{NAME}}$/NAME). **Table 3-2** lists the signals numerically by pin number. Each pin number is listed once with the various signals that are multiplexed to it. For simplicity, signals with programmable polarity are shown in this table only with their default name (asserted low).

Note: The package description in this chapter applies to packages with lead-bearing and lead-free spheres.

Table 3-1. MSC8103 Signal Listing By Name (Continued)

Signal Name	Number
D8	D6
D9	C6
D10	B6
D11	A6
D12	G7
D13	E7
D14	D7
D15	C7
D16	B7
D17	A7
D18	F8
D19	D8
D20	C8
D21	B8
D22	A8
D23	G9
D24	D9
D25	C9
D26	B9
D27	A9
D28	F10
D29	D10
D30	C10
D31	B10
D32	A10
D33	G11
D34	D11
D35	C11
D36	B11
D37	A11
D38	F12
D39	D12
D40	C12
D41	B12

Table 3-1. MSC8103 Signal Listing By Name (Continued)

Signal Name	Number
RXD3 for FCC2 MII/HDLC nibble	R4
RXD4 for FCC1 UTOPIA 8	W8
RXD5 for FCC1 UTOPIA 8	W3
RXD6 for FCC1 UTOPIA 8	M7
RXD7 for FCC1 UTOPIA 8	T4
$\overline{\text{RXENB}}$ for FCC1	K1
RXPRTY for FCC1 UTOPIA 8	N7
RXSOC for FCC1	L1
SCL	R4
SDA	U2
SMRXD for SMC1	P10
SMRXD for SMC2	U10
$\overline{\text{SMSYN}}$ for SMC1	V9
$\overline{\text{SMSYN}}$ for SMC2	V10
SMTXD for SMC1	W10
SMTXD for SMC2	W9
SMTXD for SMC2	V3
SPARE1	R2
SPARE5	U11
SPICLK	U3
SPIMISO	U4
SPIMOSI	N7
$\overline{\text{SPISEL}}$	V2
$\overline{\text{SRESET}}$	W4
$\overline{\text{TA}}$	J13
$\overline{\text{TBST}}$	U13
TC0	E18
TC1	F18
TC2	G18
TCK	G4
TDI	H6
TDO	F1
$\overline{\text{TEA}}$	G17
TEST	W6

Table 3-1. MSC8103 Signal Listing By Name (Continued)

Signal Name	Number
V_{DD}	H16
V_{DD}	J4
V_{DD}	L16
V_{DD}	L4
V_{DD}	N4
V_{DD}	P16
V_{DD}	R11
V_{DD}	R13
V_{DD}	R8
V_{DDH}	E10
V_{DDH}	E11
V_{DDH}	E13
V_{DDH}	E15
V_{DDH}	E4
V_{DDH}	E6
V_{DDH}	E8
V_{DDH}	G15
V_{DDH}	G16
V_{DDH}	G5
V_{DDH}	J15
V_{DDH}	J16
V_{DDH}	K16
V_{DDH}	K5
V_{DDH}	M4
V_{DDH}	N15
V_{DDH}	N16
V_{DDH}	R10
V_{DDH}	R12
V_{DDH}	R14
V_{DDH}	R15
V_{DDH}	R6
V_{DDH}	R7
V_{DDH}	R9
V_{DDH}	T15

Table 3-2. MSC8103 Signal Listing by Pin Designator (Continued)

Number	Signal Name
E5	V_{DD}
E6	V_{DDH}
E7	D13
E8	V_{DDH}
E9	V_{DD}
E10	V_{DDH}
E11	V_{DDH}
E12	V_{DD}
E13	V_{DDH}
E14	D47 / HD15
E15	V_{DDH}
E16	D56 / $\overline{\text{HACK}}$ / $\overline{\text{HRRQ}}$
E17	PSDA10 / PGPL0
E18	MODCK1 / TC0 / BNKSEL0
E19	$\overline{\text{PSDCAS}}$ / PGPL3
F1	TDO
F2	EED
F3	BTM1 / EE5
F4	V_{DD}
F5	GND
F6	$\overline{\text{IRQ7}}$ / DP7 / $\overline{\text{DACK4}}$
F7	GND
F8	D18
F9	GND
F10	D28
F11	GND
F12	D38 / HD6
F13	GND
F14	$\overline{\text{PSDWE}}$ / PGPL1
F15	GND
F16	V_{DD}
F17	$\overline{\text{PWE7}}$ / $\overline{\text{PSDDQM7}}$ / $\overline{\text{PBS7}}$
F18	MODCK2 / TC1 / BNKSEL1
F19	$\overline{\text{BCTL0}}$
G1	PA31 / FCC1:UTOPIA8:$\overline{\text{TXENB}}$ / FCC1:MII:COL
G2	TMS
G3	$\overline{\text{TRST}}$
G4	TCK
G5	V_{DDH}

Table 3-2. MSC8103 Signal Listing by Pin Designator (Continued)

Number	Signal Name
M7	PA16 / FCC1:UTOPIA8:RXD6 / FCC1:MII and HDLC nibble:RXD1
M13	A21
M14	A26
M15	GND
M16	$\overline{CS0}$
M17	$\overline{CS5}$
M18	$\overline{CS7}$
M19	$\overline{CS4}$
N1	PC25 / DMA:$\overline{DACK2}$ / BRG7O / CLK7 / TIN4
N2	PA25 / FCC1:UTOPIA8:TXD0 / SDMA:MSNUM0
N3	PB25 / FCC2:MII and HDLC nibble:TXD3 / TDMA1:nibble:L1TXD3 / TDMC2:L1TSYNC
N4	V_{DD}
N5	PC23 / EXT2 / DMA:$\overline{DACK1}$ / CLK9
N6	GND
N7	PD17 / FCC1:UTOPIA8:RXPRTY / SPI:SPIMOSI / BRG2O
N8	CLKIN
N9	GND
N10	PC6 / FCC1:UTOPIA8:RXADDR2 / FCC1:UTOPIA8:RXADDR2/RXCLAV1 / FCC1:$\overline{CD}$ / SI2:LIST2
N11	TSIZ3
N12	TT1
N13	TT0
N14	A1
N15	V_{DDH}
N16	V_{DDH}
N17	A28
N18	A30
N19	A31
P1	PC24 / DMA:DREQ2 / BRG8O / CLK8 / TIN3/$\overline{TOUT4}$
P2	PA24 / FCC1:UTOPIA8:TXD1 / SDMA:MSNUM1
P3	PB24 / FCC2:MII and HDLC nibble:TXD2 / TDMA1:nibble:L1RXD3 / TDMC2:L1RSYNC
P4	PA23 / FCC1:UTOPIA8:TXD2
P5	PB20 / FCC2:MII and HDLC nibble:RXD1 / TDMA1:nibble:L1TXD1 / TDMD2:L1RSYNC
P6	GND
P7	GND
P8	DLLIN
P9	GND

3.2 Lidded FC-PBGA Package Mechanical Drawing

.

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M–1994.
2. Dimensions in millimeters.
3. Maximum solder ball diameter measured parallel to Datum A.
4. Primary Datum A and the seating plane are defined by the spherical crowns of the solder balls.

CASE 1473-01

Figure 3-3. Case 1473-01 Mechanical Information, 332-pin Lidded FC-PBGA Package

Ordering Information

For product availability, consult a Freescale Semiconductor sales office or authorized distributor.

Part	Supply Voltage	Package Type	Pin Count	Mask Set	Sphere Type	Core Frequency (MHz)	Order Number
MSC8103	1.6 V core 3.3 V I/O	Lidded Flip Chip Plastic Ball Grid Array (FC-PBGA)	332	2K87M	Pb-bearing	275	MSC8103M1100F
					Pb-free	275	MSC8103VT1100F
					Pb-bearing	300	MSC8103M1200F
					Pb-free	300	MSC8103VT1200F

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