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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xe164gm-48f80l-aa

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



General Device Information

Table	Fable 5 Pin Definitions and Functions (cont'd)					
Pin	Symbol	Ctrl.	Туре	Function		
6	P7.0	O0 / I	St/B	Bit 0 of Port 7, General Purpose Input/Output		
	T3OUT	01	St/B	GPT12E Timer T3 Toggle Latch Output		
	T6OUT	02	St/B	GPT12E Timer T6 Toggle Latch Output		
	TDO_A	OH / IH	St/B	JTAG Test Data Output / DAP1 Input/Output If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.		
	ESR2_1	I	St/B	ESR2 Trigger Input 1		
7	P7.3	O0 / I	St/B	Bit 3 of Port 7, General Purpose Input/Output		
	EMUX1	01	St/B	External Analog MUX Control Output 1 (ADC1)		
	U0C1_DOUT	02	St/B	USIC0 Channel 1 Shift Data Output		
	U0C0_DOUT	O3	St/B	USIC0 Channel 0 Shift Data Output		
	CCU62_CCP OS1A	I	St/B	CCU62 Position Input 1		
	TMS_C	IH	St/B	JTAG Test Mode Selection Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.		
	U0C1_DX0F	I	St/B	USIC0 Channel 1 Shift Data Input		
8	P7.1	O0 / I	St/B	Bit 1 of Port 7, General Purpose Input/Output		
	EXTCLK	01	St/B	Programmable Clock Signal Output		
	CCU62_CTR APA	I	St/B	CCU62 Emergency Trap Input		
	BRKIN_C	I	St/B	OCDS Break Signal Input		



General Device Information

Tabl	Fin Definitions and Functions (cont'd)					
Pin	Symbol	Ctrl.	Туре	Function		
54	P2.7	O0 / I	St/B	Bit 7 of Port 2, General Purpose Input/Output		
	U0C1_SELO 0	01	St/B	USIC0 Channel 1 Select/Control 0 Output		
	U0C0_SELO 1	O2	St/B	USIC0 Channel 0 Select/Control 1 Output		
	CC2_CC20	O3 / I	St/B	CAPCOM2 CC20IO Capture Inp./ Compare Out.		
	A20	ОН	St/B	External Bus Interface Address Line 20		
	U0C1_DX2C	I	St/B	USIC0 Channel 1 Shift Control Input		
	RxDC1C	I	St/B	CAN Node 1 Receive Data Input		
	ESR2_7	I	St/B	ESR2 Trigger Input 7		
55	P0.1	O0 / I	St/B	Bit 1 of Port 0, General Purpose Input/Output		
-	U1C0_DOUT	01	St/B	USIC1 Channel 0 Shift Data Output		
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output		
	CCU61_CC6 1	O3	St/B	CCU61 Channel 1 Output		
	A1	OH	St/B	External Bus Interface Address Line 1		
	U1C0_DX0B	I	St/B	USIC1 Channel 0 Shift Data Input		
	CCU61_CC6 1INA	I	St/B	CCU61 Channel 1 Input		
	U1C0_DX1A	I	St/B	USIC1 Channel 0 Shift Clock Input		
56	P2.8	O0 / I	DP/B	Bit 8 of Port 2, General Purpose Input/Output		
	U0C1_SCLK OUT	01	DP/B	USIC0 Channel 1 Shift Clock Output		
	EXTCLK	O2	DP/B	Programmable Clock Signal Output		
	CC2_CC21	O3 / I	DP/B	CAPCOM2 CC21IO Capture Inp./ Compare Out.		
	A21	OH	DP/B	External Bus Interface Address Line 21		
	U0C1_DX1D	I	DP/B	USIC0 Channel 1 Shift Clock Input		



General Device Information

Table	Table 5 Pin Definitions and Functions (cont'd)					
Pin	Symbol	Ctrl.	Туре	Function		
59	P10.0	O0 / I	St/B	Bit 0 of Port 10, General Purpose Input/Output		
	U0C1_DOUT	01	St/B	USIC0 Channel 1 Shift Data Output		
	CCU60_CC6 0	O2	St/B	CCU60 Channel 0 Output		
	AD0	OH / IH	St/B	External Bus Interface Address/Data Line 0		
	CCU60_CC6 0INA	I	St/B	CCU60 Channel 0 Input		
	ESR1_2	I	St/B	ESR1 Trigger Input 2		
	U0C0_DX0A	I	St/B	USIC0 Channel 0 Shift Data Input		
	U0C1_DX0A	I	St/B	USIC0 Channel 1 Shift Data Input		
60	P10.1	O0 / I	St/B	Bit 1 of Port 10, General Purpose Input/Output		
	U0C0_DOUT	01	St/B	USIC0 Channel 0 Shift Data Output		
	CCU60_CC6 1	O2	St/B	CCU60 Channel 1 Output		
	AD1	OH / IH	St/B	External Bus Interface Address/Data Line 1		
	CCU60_CC6 1INA	I	St/B	CCU60 Channel 1 Input		
	U0C0_DX1A	I	St/B	USIC0 Channel 0 Shift Clock Input		
	U0C0_DX0B	I	St/B	USIC0 Channel 0 Shift Data Input		
61	P0.3	O0 / I	St/B	Bit 3 of Port 0, General Purpose Input/Output		
	U1C0_SELO 0	01	St/B	USIC1 Channel 0 Select/Control 0 Output		
	U1C1_SELO 1	O2	St/B	USIC1 Channel 1 Select/Control 1 Output		
	CCU61_COU T60	O3	St/B	CCU61 Channel 0 Output		
	A3	ОН	St/B	External Bus Interface Address Line 3		
	U1C0_DX2A	I	St/B	USIC1 Channel 0 Shift Control Input		
	RxDC0B	I	St/B	CAN Node 0 Receive Data Input		



General Device Information

Table	able 5 Fin Definitions and Functions (cont d)					
Pin	Symbol	Ctrl.	Туре	Function		
97	PORST	1	In/B	Power On Reset Input A low level at this pin resets the XE164xM completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pull-up device will hold this pin high when nothing is driving it.		
98	ESR1	O0 / I	St/B	External Service Request 1 After power-up, an internal weak pull-up device holds this pin high when nothing is driving it.		
	RxDC0E	I	St/B	CAN Node 0 Receive Data Input		
	U1C0_DX0F	Ι	St/B	USIC1 Channel 0 Shift Data Input		
	U1C0_DX2C	I	St/B	USIC1 Channel 0 Shift Control Input		
	U1C1_DX0C	I	St/B	USIC1 Channel 1 Shift Data Input		
-	U1C1_DX2B	Ι	St/B	USIC1 Channel 1 Shift Control Input		
	U2C1_DX2C	I	St/B	USIC2 Channel 1 Shift Control Input		
99	ESR0	O0 / I	St/B	External Service Request 0 After power-up, ESR0 operates as open-drain bidirectional reset with a weak pull-up.		
	U1C0_DX0E	I	St/B	USIC1 Channel 0 Shift Data Input		
	U1C0_DX2B	I	St/B	USIC1 Channel 0 Shift Control Input		
10	V _{DDIM}	-	PS/M	Digital Core Supply Voltage for Domain M Decouple with a ceramic capacitor, see Data Sheet for details.		
38, 64, 88	V _{DDI1}	-	PS/1	Digital Core Supply Voltage for Domain 1 Decouple with a ceramic capacitor, see Data Sheet for details. All V_{DDI1} pins must be connected to each other.		
14	V _{DDPA}	-	PS/A	Digital Pad Supply Voltage for Domain A Connect decoupling capacitors to adjacent $V_{\text{DDP}}/V_{\text{SS}}$ pin pairs as close as possible to the pins. Note: The A/D_Converters and ports P5, P6 and P15 are fed from supply voltage V_{DDPA} .		

Tabla F Din Definitions and Eurotions (cost'd)



3.4 Memory Protection Unit (MPU)

The XE164xM's Memory Protection Unit (MPU) protects user-specified memory areas from unauthorized read, write, or instruction fetch accesses. The MPU can protect the whole address space including the peripheral area. This completes establisched mechanisms such as the register security mechanism or stack overrun/underrun detection.

Four Protection Levels support flexible system programming where operating system, low level drivers, and applications run on separate levels. Each protection level permits different access restrictions for instructions and/or data.

Every access is checked (if the MPU is enabled) and an access violating the permission rules will be marked as invalid and leads to a protection trap.

A set of protection registers for each protection level specifies the address ranges and the access permissions. Applications requiring more than 4 protection levels can dynamically re-program the protection registers.

3.5 Memory Checker Module (MCHK)

The XE164xM's Memory Checker Module calculates a checksum (fractional polynomial division) on a block of data, often called Cyclic Redundancy Code (CRC). It is based on a 32-bit linear feedback shift register and may, therefore, also be used to generate pseudo-random numbers.

The Memory Checker Module is a 16-bit parallel input signature compression circuitry which enables error detection within a block of data stored in memory, registers, or communicated e.g. via serial communication lines. It reduces the probability of error masking due to repeated error patterns by calculating the signature of blocks of data.

The polynomial used for operation is configurable, so most of the commonly used polynomials may be used. Also, the block size for generating a CRC result is configurable via a local counter. An interrupt may be generated if testing the current data block reveals an error.

An autonomous CRC compare circuitry is included to enable redundant error detection, e.g. to enable higher safety integrity levels.

The Memory Checker Module provides enhanced fault detection (beyond parity or ECC) for data and instructions in volatile and non volatile memories. This is especially important for the safety and reliability of embedded systems.



3.6 Interrupt System

The architecture of the XE164xM supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Where in a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XE164xM has eight PEC channels, each whith fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of 7/11¹⁾ CPU clocks, the XE164xM can react quickly to the occurrence of non-deterministic events.

Interrupt Nodes and Source Selection

The interrupt system provides 96 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

Trap Processing

The XE164xM provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called 'Hardware Traps'. A hardware trap causes an immediate system reaction similar to a standard interrupt service (branching

¹⁾ Depending if the jump cache is used or not.



to a dedicated vector table location). The occurrence of a hardware trap is also indicated by a single bit in the trap flag register (TFR). Unless another higher-priority trap service is in progress, a hardware trap will interrupt any ongoing program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Depending on the package option up to 3 External Service Request (ESR) pins are provided. The ESR unit processes their input values and allows to implement user controlled trap functions (System Requests SR0 and SR1). In this way reset, wakeup and power control can be efficiently realized.

Software interrupts are supported by the 'TRAP' instruction in combination with an individual trap (interrupt) number. Alternatively to emulate an interrupt by software a program can trigger interrupt requests by writing the Interrupt Request (IR) bit of an interrupt control register.

3.7 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system built into the XE164xM provides a broad range of debug and emulation features. User software running on the XE164xM can be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface. This either consists of the 2-pin Device Access Port (DAP) or of the JTAG port conforming to IEEE-1149. The debug interface can be completed with an optional break interface.

The debugger controls the OCDS with a set of dedicated registers accessible via the debug interface (DAP or JTAG). In addition the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported, as is the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing data can be obtained via the debug interface, or via the external bus interface for increased performance.

Tracing of program execution is supported by the XE166 Family emulation device.

The DAP interface uses two interface signals, the JTAG interface uses four interface signals, to communicate with external circuitry. The debug interface can be amended with two optional break lines.



3.14 MultiCAN Module

The MultiCAN module contains independently operating CAN nodes with Full-CAN functionality which are able to exchange Data and Remote Frames using a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

Note: The number of CAN nodes and message objects depends on the selected device type.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to its own message object list and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.



Figure 12 Block Diagram of MultiCAN Module



MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Independent CAN nodes
- Set of independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
 - Can be assigned to one of the CAN nodes
 - Configurable as transmit or receive objects, or as message buffer FIFO
 - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
 - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

3.15 System Timer

The System Timer consists of a programmable prescaler and two concatenated timers (10 bits and 6 bits). Both timers can generate interrupt requests. The clock source can be selected and the timers can also run during power reduction modes.

Therefore, the System Timer enables the software to maintain the current time for scheduling functions or for the implementation of a clock.



4.2.1 DC Parameters

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV} .

Note: Operating Conditions apply.

 Table 13 is valid under the following conditions:

 $V_{\text{DDP}} \ge 4.5 \text{ V}; V_{\text{DDPtvp}} = 5 \text{ V}; V_{\text{DDP}} \le 5.5 \text{ V}$

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Pin capacitance (digital inputs/outputs). To be doubled for double bond pins. ¹⁾	C _{IO} CC	-	-	10	pF	not subject to production test
Input Hysteresis ²⁾	HYS CC	0.11 x V _{DDP}	-	-	V	$R_{\rm S} = 0$ Ohm
Absolute input leakage current on pins of analog ports ³⁾	I _{OZ1} CC	_	10	200	nA	$V_{\rm IN}$ > 0 V; $V_{\rm IN}$ < $V_{\rm DDP}$
Absolute input leakage current for all other pins. To be doubled for double	I _{OZ2} CC	-	0.2	5	μΑ	$\begin{array}{l} T_{\rm J} \leq 110 ~^{\circ}{\rm C}; \\ V_{\rm IN} < V_{\rm DDP}; \\ V_{\rm IN} > V_{\rm SS} \end{array}$
bond pins. ³⁾¹⁾⁴⁾		-	0.2	15	μΑ	$T_{ m J} \leq$ 150 °C; $V_{ m IN} < V_{ m DDP};$ $V_{ m IN} > V_{ m SS}$
Pull Level Force Current ⁵⁾	$ I_{PLF} $ SR	250	-	-	μA	6)
Pull Level Keep Current ⁷⁾	I _{PLK} SR	-	-	30	μA	6)
Input high voltage (all except XTAL1)	$V_{\rm IH}{ m SR}$	$0.7 ext{ x}$ $V_{ ext{DDP}}$	-	V _{DDP} + 0.3	V	
Input low voltage (all except XTAL1)	$V_{\rm IL}{\rm SR}$	-0.3	-	$0.3 ext{ x}$ $V_{ ext{DDP}}$	V	
Output High voltage ⁸⁾	V _{OH} CC	V _{DDP} - 1.0	-	-	V	$I_{\rm OH} \ge I_{\rm OHmax}$
		V _{DDP} - 0.4	_	-	V	$I_{OH} \ge I_{OHnom}^{9)}$

Table 13 DC Characteristics for Upper Voltage Range



			•	•	•	,
Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Output Low Voltage ⁸⁾	$V_{\rm OL}{\rm CC}$	-	-	1.0	V	$I_{\rm OL} \leq I_{\rm OLmax}$
		-	-	0.4	V	$I_{\rm OL} \leq I_{\rm OLnom}^{9)}$

Table 13 DC Characteristics for Upper Voltage Range (cont'd)

1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.

- Not subject to production test verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.
- 3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{\rm IN} < V_{\rm SS}$) or supply ripple ($V_{\rm IN} > V_{\rm DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current ($I_{\rm INJ}$) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor $K_{\rm CV}$.
- 4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature (*T*_J = junction temperature [°C]): *I*_{OZ} = 0.05 x e^(1.5 + 0.028 x TJ-) [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = *V*_{DDP} *V*_{PIN} [V]): *I*_{OZ} = *I*_{OZtempmax} (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.
- 5) Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: V_{PIN} ≤ V_{ILmax} for a pullup; V_{PIN} ≥ V_{ILmin} for a pulldown.
- 6) These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.
- 7) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: V_{PIN} ≥ V_{IHmin} for a pullup; V_{PIN} ≤ V_{ILmax} for a pulldown.
- 8) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
- 9) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL} -> V_{SS} , V_{OH} -> V_{DDP}). However, only the levels for nominal output currents are verified.



					`	,
Parameter	Symbol Values			lues		Note /
		Min.	Тур.	Max.		Test Condition
Output Low Voltage ⁸⁾	$V_{\rm OL}{\rm CC}$	-	-	1.0	V	$I_{\rm OL} \leq I_{\rm OLmax}$
		-	-	0.4	V	$I_{\rm OL} \leq I_{\rm OLnom}^{10}$

Table 14 DC Characteristics for Lower Voltage Range (cont'd)

1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.

- 2) Not subject to production test verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.
- 3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{\rm IN} < V_{\rm SS}$) or supply ripple ($V_{\rm IN} > V_{\rm DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current ($I_{\rm INJ}$) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor $K_{\rm CV}$.
- 4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature (*T*_J = junction temperature [°C]): *I*_{OZ} = 0.05 x e^(1.5 + 0.028 x TJ-) [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = *V*_{DDP} *V*_{PIN} [V]): *I*_{OZ} = *I*_{OZtempmax} (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.
- Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: V_{PIN} <= V_{IL} for a pullup; V_{PIN} >= V_{IH} for a pulldown.
- 6) These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.
- 7) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: V_{PIN} >= V_{IH} for a pullup; V_{PIN} <= V_{IL} for a pulldown.
- 8) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
- As a rule, with decreasing output current the output levels approach the respective supply level (VOL->VSS, VOH->VDDP). However, only the levels for nominal output currents are verified.
- 10) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL} -> V_{SS} , V_{OH} -> V_{DDP}). However, only the levels for nominal output currents are verified.



Electrical Parameters



Figure 15 Leakage Supply Current as a Function of Temperature



Sample time and conversion time of the XE164xM's A/D converters are programmable. The timing above can be calculated using **Table 18**.

The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

GLOBCTR.5-0 (DIVA)	A/D Converter Analog Clock f_{ADCI}	INPCRx.7-0 (STC)	Sample Time ¹⁾ t _s
000000 _B	f _{sys}	00 _H	$t_{ADCI} \times 2$
000001 _B	<i>f</i> _{SYS} / 2	01 _H	$t_{ADCI} \times 3$
000010 _B	<i>f</i> _{SYS} / 3	02 _H	$t_{ADCI} \times 4$
:	$f_{\rm SYS}$ / (DIVA+1)	:	$t_{ADCI} \times (STC+2)$
111110 _B	f _{SYS} / 63	FE _H	$t_{ADCI} \times 256$
111111 _B	f _{SYS} / 64	FF _H	$t_{ADCI} \times 257$

 Table 18
 A/D Converter Computation Table

1) The selected sample time is doubled if broken wire detection is active (due to the presampling phase).

Converter Timing Example A:

Assumptions:	$f_{\rm SYS}$	= 80 MHz (i.e. t_{SYS} = 12.5 ns), DIVA = 03 _H , STC = 00 _H
Analog clock	$f_{\rm ADCI}$	$= f_{SYS} / 4 = 20 \text{ MHz}$, i.e. $t_{ADCI} = 50 \text{ ns}$
Sample time	t _S	$= t_{ADCI} \times 2 = 100 \text{ ns}$
Conversion 10	-bit:	
	<i>t</i> _{C10}	= $13 \times t_{ADCI}$ + $2 \times t_{SYS}$ = 13×50 ns + 2×12.5 ns = 0.675 μ s
Conversion 8-b	oit:	
	t _{C8}	= $11 \times t_{ADCI}$ + $2 \times t_{SYS}$ = 11×50 ns + 2×12.5 ns = 0.575 µs

Converter Timing Example B:

Assumptions:	$f_{\rm SYS}$	= 40 MHz (i.e. t_{SYS} = 25 ns), DIVA = 02 _H , STC = 03 _H
Analog clock	$f_{\rm ADCI}$	$= f_{SYS} / 3 = 13.3 \text{ MHz}$, i.e. $t_{ADCI} = 75 \text{ ns}$
Sample time	t _S	$= t_{ADCI} \times 5 = 375 \text{ ns}$
Conversion 10-b	oit:	
	<i>t</i> _{C10}	= $16 \times t_{ADCI}$ + 2 × t_{SYS} = 16 × 75 ns + 2 × 25 ns = 1.25 µs
Conversion 8-bi	t:	
	t _{C8}	= $14 \times t_{ADCI}$ + $2 \times t_{SYS}$ = 14×75 ns + 2×25 ns = 1.10 μ s



- 3) $f_{\rm WU}$ in MHz
- 4) This value includes a hysteresis of approximately 50 mV for rising voltage.
- 5) $V_{\rm LV}$ = selected SWD voltage level
- 6) The limit V_{LV} 0.10 V is valid for the OK1 level. The limit for the OK2 level is V_{LV} 0.15 V.

Conditions for t_{SPO} Timing Measurement

The time required for the transition from **Power-On** to **Base** mode is called t_{SPO} . It is measured under the following conditions:

Precondition: The pad supply is valid, i.e. V_{DDPB} is above 3.0 V and remains above 3.0 V even though the XE164xM is starting up. No debugger is attached.

Start condition: Power-on reset is removed ($\overline{PORST} = 1$).

End condition: External pin toggle caused by first user instruction executed from FLASH after startup.

Conditions for t_{SSO} Timing Measurement

The time required for the transition from **Stopover** to **Stopover Waked-Up** mode is called t_{SSO} . It is measured under the following conditions:

Precondition: The **Stopover** mode has been entered using the procedure defined in the Programmer's Guide.

Start condition: Pin toggle on ESR pin triggering the startup sequence.

Coding of bit fields LEVxV in SWD and PVC Configuration Registers

End condition: External pin toggle caused by first user instruction executed from PSRAM after startup.

Table 20	County of bit netus LEVXV in Register SWDCONU							
Code	Default Voltage Level	Notes ¹⁾						
0000 _B	2.9 V							
0001 _B	3.0 V	LEV1V: reset request						
0010 _B	3.1 V							
0011 _B	3.2 V							
0100 _B	3.3 V							
0101 _B	3.4 V							
0110 _B	3.6 V							
0111 _B	4.0 V							
1000 _B	4.2 V							

Table 20 Coding of bit fields LEVxV in Register SWDCON0





Figure 20 Approximated Accumulated PLL Jitter

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L = 20 \text{ pF}$.

The maximum peak-to-peak noise on the pad supply voltage (measured between V_{DDPB} pin 100 and V_{SS} pin 1) is limited to a peak-to-peak voltage of V_{PP} = 50 mV. This can be achieved by appropriate blocking of the supply voltage as close as possible to the supply pins and using PCB supply and ground planes.



 Table 26 is valid under the following conditions:

 $V_{\text{DDP}} \ge 3.0 \text{ V}; V_{\text{DDPtyp}} = 3.3 \text{ V}; V_{\text{DDP}} \le 4.5 \text{ V}; C_{\text{L}} \ge 20 \text{ pF}; C_{\text{L}} \le 100 \text{ pF};$

Table 26	Standard Pa	ad Parameters	for Lower	Voltage Range
	otuniaurari			Tonago nango

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.	-	Test Condition
Maximum output driver current (absolute value) ¹⁾	I _{Omax} CC	-	-	10	mA	Strong driver
		-	-	2.5	mA	Medium driver
		-	-	0.5	mA	Weak driver
Nominal output driver	I _{Onom} CC	-	-	2.5	mA	Strong driver
current (absolute value)		-	-	1.0	mA	Medium driver
		-	-	0.1	mA	Weak driver
Rise and Fall times (10% - 90%)	t _{RF} CC	-	-	6.2 + 0.24 x <i>C</i> _L	ns	Strong driver; Sharp edge
		_	-	24 + 0.3 x <i>C</i> _L	ns	Strong driver; Medium edge
		-	-	34 + 0.3 x <i>C</i> _L	ns	Strong driver; Slow edge
		_	-	37 + 0.65 x <i>C</i> _L	ns	Medium driver
		-	-	500 + 2.5 x <i>C</i> L	ns	Weak driver

 The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and Σ-I_{OH}) must remain below 50 mA.



4.6.5.1 Bus Cycle Control with the READY Input

The duration of an external bus cycle can be controlled by the external circuit using the READY input signal. The polarity of this input signal can be selected.

Synchronous READY permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

An asynchronous READY signal puts no timing constraints on the input signal but incurs a minimum of one waitstate due to the additional synchronization stage. The minimum duration of an asynchronous READY signal for safe synchronization is one CLKOUT period plus the input setup time.

An active READY signal can be deactivated in response to the trailing (rising) edge of the corresponding command (\overline{RD} or \overline{WR}).

If the next bus cycle is controlled by READY, an active READY signal must be disabled before the first valid sample point in the next bus cycle. This sample point depends on the programmed phases of the next cycle.



4.6.7 Debug Interface Timing

The debugger can communicate with the XE164xM either via the 2-pin DAP interface or via the standard JTAG interface.

Debug via DAP

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply; C_L = 20 pF.

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
DAP0 clock period	<i>t</i> ₁₁ SR	25 ¹⁾	-	-	ns	
DAP0 high time	t ₁₂ SR	8	-	-	ns	
DAP0 low time	t ₁₃ SR	8	-	-	ns	
DAP0 clock rise time	<i>t</i> ₁₄ SR	-	-	4	ns	
DAP0 clock fall time	<i>t</i> ₁₅ SR	-	-	4	ns	
DAP1 setup to DAP0 rising edge	<i>t</i> ₁₆ SR	6	-	-	ns	pad_type= stan dard
DAP1 hold after DAP0 rising edge	<i>t</i> ₁₇ SR	6	-	-	ns	pad_type= stan dard
DAP1 valid per DAP0 clock period ²⁾	<i>t</i> ₁₉ CC	17	20	-	ns	pad_type= stan dard

 Table 35
 DAP Interface Timing for Upper Voltage Range

1) The debug interface cannot operate faster than the overall system, therefore $t_{11} \ge t_{SYS}$.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.



Electrical Parameters



Figure 28 DAP Timing Host to Device



Figure 29 DAP Timing Device to Host

Note: The transmission timing is determined by the receiving debugger by evaluating the sync-request synchronization pattern telegram.