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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24К х 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xe164hm-24f80l-aa

Email: info@E-XFL.COM

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16-Bit

Architecture

XE164FM, XE164GM, XE164HM, XE164KM

16-Bit Single-Chip Real Time Signal Controller XE166 Family / Base Line

Data Sheet V2.1 2011-07

Microcontrollers



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General Device Information

Table	Fable 5 Pin Definitions and Functions (cont'd)							
Pin	Symbol	Ctrl.	Туре	Function				
6	P7.0	O0 / I	St/B	Bit 0 of Port 7, General Purpose Input/Output				
	T3OUT	01	St/B	GPT12E Timer T3 Toggle Latch Output				
	T6OUT	02	St/B	GPT12E Timer T6 Toggle Latch Output				
	TDO_A	OH / IH	St/B	JTAG Test Data Output / DAP1 Input/Output If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.				
	ESR2_1	I	St/B	ESR2 Trigger Input 1				
7	P7.3	O0 / I	St/B	Bit 3 of Port 7, General Purpose Input/Output				
	EMUX1	01	St/B	External Analog MUX Control Output 1 (ADC1)				
	U0C1_DOUT	02	St/B	USIC0 Channel 1 Shift Data Output				
	U0C0_DOUT	O3	St/B	USIC0 Channel 0 Shift Data Output				
	CCU62_CCP OS1A	I	St/B	CCU62 Position Input 1				
	TMS_C	IH	St/B	JTAG Test Mode Selection Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.				
	U0C1_DX0F	I	St/B	USIC0 Channel 1 Shift Data Input				
8	P7.1	O0 / I	St/B	Bit 1 of Port 7, General Purpose Input/Output				
	EXTCLK	01	St/B	Programmable Clock Signal Output				
	CCU62_CTR APA	I	St/B	CCU62 Emergency Trap Input				
	BRKIN_C	I	St/B	OCDS Break Signal Input				



General Device Information

Table	Fin Definitions and Functions (cont'd)						
Pin	Symbol	Ctrl.	Туре	Function			
70	P10.5	O0 / I	St/B	Bit 5 of Port 10, General Purpose Input/Output			
	U0C1_SCLK OUT	O1	St/B	USIC0 Channel 1 Shift Clock Output			
	CCU60_COU T62	O2	St/B	CCU60 Channel 2 Output			
	U2C0_DOUT	O3	St/B	USIC2 Channel 0 Shift Data Output			
	AD5	OH / IH	St/B	External Bus Interface Address/Data Line 5			
	U0C1_DX1B	I	St/B	USIC0 Channel 1 Shift Clock Input			
71	P0.6	O0 / I	St/B	Bit 6 of Port 0, General Purpose Input/Output			
	U1C1_DOUT	01	St/B	USIC1 Channel 1 Shift Data Output			
	TxDC1	02	St/B	CAN Node 1 Transmit Data Output			
	CCU61_COU T63	O3	St/B	CCU61 Channel 3 Output			
	A6	ОН	St/B	External Bus Interface Address Line 6			
	U1C1_DX0A	I	St/B	USIC1 Channel 1 Shift Data Input			
	CCU61_CTR APA	I	St/B	CCU61 Emergency Trap Input			
	U1C1_DX1B	I	St/B	USIC1 Channel 1 Shift Clock Input			
72	P10.6	O0 / I	St/B	Bit 6 of Port 10, General Purpose Input/Output			
	U0C0_DOUT	01	St/B	USIC0 Channel 0 Shift Data Output			
	U1C0_SELO 0	O3	St/B	USIC1 Channel 0 Select/Control 0 Output			
	AD6	OH / IH	St/B	External Bus Interface Address/Data Line 6			
	U0C0_DX0C	I	St/B	USIC0 Channel 0 Shift Data Input			
	U1C0_DX2D	Ι	St/B	USIC1 Channel 0 Shift Control Input			
	CCU60_CTR APA	I	St/B	CCU60 Emergency Trap Input			



3.1 Memory Subsystem and Organization

The memory space of the XE164xM is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

	-			
Address Area	Start Loc.	End Loc.	Area Size ²⁾	Notes
IMB register space	FF'FF00 _H	FF'FFFF _H	256 Bytes	-
Reserved (Access trap)	F0'0000 _H	FF'FEFF _H	<1 Mbyte	Minus IMB registers
Reserved for EPSRAM	E8'8000 _H	EF'FFFF _H	480 Kbytes	Mirrors EPSRAM
Emulated PSRAM	E8'0000 _H	E8'7FFF _H	32 Kbytes	With Flash timing
Reserved for PSRAM	E0'8000 _H	E7'FFFF _H	480 Kbytes	Mirrors PSRAM
Program SRAM	E0'0000 _H	E0'7FFF _H	32 Kbytes	Maximum speed
Reserved for Flash	CD'0000 _H	DF'FFFF _H	<1.25 Mbytes	-
Program Flash 3	CC'0000 _H	CC'FFFF _H	64 Kbytes	-
Program Flash 2	C8'0000 _H	CB'FFFF _H	256 Kbytes	-
Program Flash 1	C4'0000 _H	C7'FFFF _H	256 Kbytes	-
Program Flash 0	C0'0000 _H	C3'FFFF _H	256 Kbytes	3)
External memory area	40'0000 _H	BF'FFFF _H	8 Mbytes	-
Available Ext. IO area ⁴⁾	21'0000 _H	3F'FFFF _H	< 2 Mbytes	Minus USIC/CAN
Reserved	20'BC00 _H	20'FFFF _H	17 Kbytes	-
USIC alternate regs.	20'B000 _H	20'BFFF _H	4 Kbytes	Accessed via EBC
MultiCAN alternate	20'8000 _H	20'AFFF _H	12 Kbytes	Accessed via EBC
Reserved	20'6000	20'7FFF	8 Khytes	
	20'4000	20'5EEE.	8 Khytes	Accessed via EBC
MultiCAN registers	20'0000	20'3FFF	16 Khytes	Accessed via EBC
External memory area	01'0000	1E'EEE	< 2 Mbytes	Minus segment 0
SER area	00'EE00	00'EEEE	0.5 Kbyte	
Dual-Port RAM	00'E600		2 Khytes	
Reserved for DPRAM	00'F200	00'E5EE	1 Khyte	_
	001200 _H	00'E1EE		
				-
NORK area	UU EUUU _H	UU EFFF _H	4 NDytes	-

Table 7 XE164xM Memory Map ¹⁾



3.2 External Bus Controller

All external memory access operations are performed by a special on-chip External Bus Controller (EBC). The EBC also controls access to resources connected to the on-chip LXBus (MultiCAN and the USIC modules). The LXBus is an internal representation of the external bus that allows access to integrated peripherals and modules in the same way as to external components.

The EBC can be programmed either to Single Chip Mode, when no external memory is required, or to an external bus mode with the following selections¹⁾:

- Address Bus Width with a range of 0 ... 24-bit
- Data Bus Width 8-bit or 16-bit
- Bus Operation Multiplexed or Demultiplexed

The bus interface uses Port 10 and Port 2 for addresses and data. In the demultiplexed bus modes, the lower addresses are output separately on Port 0 and Port 1. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes ... 64 Kbytes. This is required when interface lines shall be assigned to Port 2.

External CS signals (address windows plus default) can be generated and output on Port 4 in order to save external glue logic. External modules can be directly connected to the common address/data bus and their individual select lines.

Important timing characteristics of the external bus interface are programmable (with registers TCONCSx/FCONCSx) to allow the user to adapt it to a wide range of different types of memories and external peripherals.

Access to very slow memories or modules with varying access times is supported by a special 'Ready' function. The active level of the control input signal is selectable.

In addition, up to four independent address windows may be defined (using registers ADDRSELx) to control access to resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these four address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is based on the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

¹⁾ Bus modes are switched dynamically if several address windows with different mode settings are used.



3.4 Memory Protection Unit (MPU)

The XE164xM's Memory Protection Unit (MPU) protects user-specified memory areas from unauthorized read, write, or instruction fetch accesses. The MPU can protect the whole address space including the peripheral area. This completes establisched mechanisms such as the register security mechanism or stack overrun/underrun detection.

Four Protection Levels support flexible system programming where operating system, low level drivers, and applications run on separate levels. Each protection level permits different access restrictions for instructions and/or data.

Every access is checked (if the MPU is enabled) and an access violating the permission rules will be marked as invalid and leads to a protection trap.

A set of protection registers for each protection level specifies the address ranges and the access permissions. Applications requiring more than 4 protection levels can dynamically re-program the protection registers.

3.5 Memory Checker Module (MCHK)

The XE164xM's Memory Checker Module calculates a checksum (fractional polynomial division) on a block of data, often called Cyclic Redundancy Code (CRC). It is based on a 32-bit linear feedback shift register and may, therefore, also be used to generate pseudo-random numbers.

The Memory Checker Module is a 16-bit parallel input signature compression circuitry which enables error detection within a block of data stored in memory, registers, or communicated e.g. via serial communication lines. It reduces the probability of error masking due to repeated error patterns by calculating the signature of blocks of data.

The polynomial used for operation is configurable, so most of the commonly used polynomials may be used. Also, the block size for generating a CRC result is configurable via a local counter. An interrupt may be generated if testing the current data block reveals an error.

An autonomous CRC compare circuitry is included to enable redundant error detection, e.g. to enable higher safety integrity levels.

The Memory Checker Module provides enhanced fault detection (beyond parity or ECC) for data and instructions in volatile and non volatile memories. This is especially important for the safety and reliability of embedded systems.



3.8 Capture/Compare Unit (CAPCOM2)

The CAPCOM2 unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of one system clock cycle (eight cycles in staggered mode). The CAPCOM2 unit is typically used to handle high-speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), digital to analog (D/A) conversion, software timing, or time recording with respect to external events.

Two 16-bit timers (T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range or variation for the timer period and resolution and allows precise adjustments to the application-specific requirements. In addition, an external count input allows event scheduling for the capture/compare registers relative to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer and programmed for capture or compare function.

All registers have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

Compare Modes	Function
Mode 0	Interrupt-only compare mode; Several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; Several compare events per timer period are possible

Table 8 Compare Modes



With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD¹). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XE164xM to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

¹⁾ Exception: T5EUD is not connected to a pin.



Functional Description







4.1.2 Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XE164xM. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Note: Typical parameter values refer to room temperature and nominal supply voltage, minimum/maximum parameter values also include conditions of minimum/maximum temperature and minimum/maximum supply voltage. Additional details are described where applicable.

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Voltage Regulator Buffer Capacitance for DMP_M	$C_{\rm EVRM}$ SR	1.0	-	4.7	μF	1)
Voltage Regulator Buffer Capacitance for DMP_1	$C_{\rm EVR1}$ SR	0.47	-	2.2	μF	1)2)
External Load Capacitance	$C_{L} \operatorname{SR}$	-	20 ³⁾	-	pF	pin out driver= default 4)
System frequency	$f_{\rm SYS}{\rm SR}$	-	-	100	MHz	5)
Overload current for analog inputs ⁶⁾	$I_{\rm OVA}{\rm SR}$	-2	-	5	mA	not subject to production test
Overload current for digital inputs ⁶⁾	$I_{\rm OVD}{\rm SR}$	-5	-	5	mA	not subject to production test
Overload current coupling factor for analog inputs ⁷⁾	K _{OVA} CC	-	2.5 x 10⁻⁴	1.5 x 10 ⁻³	-	I _{OV} < 0 mA; not subject to production test
		_	1.0 x 10 ⁻⁶	1.0 x 10 ⁻⁴	-	I _{OV} > 0 mA; not subject to production test
Overload current coupling factor for digital I/O pins	K _{OVD} CC	_	1.0 x 10 ⁻²	3.0 x 10 ⁻²		I _{OV} < 0 mA; not subject to production test
		_	1.0 x 10 ⁻⁴	5.0 x 10 ⁻³		I _{OV} > 0 mA; not subject to production test

Table 12 Operating Conditions



2) The pad supply voltage pins (V_{DDPB}) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers input stages are switched.

In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to $3 + 0.6 \text{ x} f_{SYS}$.

3) Please consider the additional conditions described in section "Active Mode Power Supply Current".

Active Mode Power Supply Current

The actual power supply current in active mode not only depends on the system frequency but also on the configuration of the XE164xM's subsystem.

Besides the power consumed by the device logic the power supply pins also provide the current that flows through the pin output drivers.

A small current is consumed because the drivers' input stages are switched.

The IO power domains can be supplied separately. Power domain A ($V_{\rm DDPA}$) supplies the A/D converters and Port 6. Power domain B ($V_{\rm DDPB}$) supplies the on-chip EVVRs and all other ports.

During operation domain A draws a maximum current of 1.5 mA for each active A/D converter module from $V_{\rm DDPA}$.

In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to $(3 + 0.6 \times f_{SYS})$ mA.





Figure 16 Equivalent Circuitry for Analog Inputs



Table 20	Coding d	County of bit news LEVXV in Register SwDCONU (Cont a)							
Code	Defa	ult Voltage Level	Notes ¹⁾						
1001 _B	4.5 V		LEV2V: no request						
1010 _B	4.6 V								
1011 _B	4.7 V								
1100 _B	4.8 V								
1101 _B	4.9 V								
1110 _B	5.0 V								
1111 _B	5.5 V								

Table 20 Coding of bit fields LEVxV in Register SWDCON0 (cont'd)

1) The indicated default levels are selected automatically after a power reset.

Table 21 Coding of Bitfields LEVxV in Registers PVCyCONz

Code	Default Voltage Level	Notes ¹⁾
000 _B	0.95 V	
001 _B	1.05 V	
010 _B	1.15 V	
011 _B	1.25 V	
100 _B	1.35 V	LEV1V: reset request
101 _B	1.45 V	LEV2V: interrupt request ²⁾
110 _B	1.55 V	
111 _B	1.65 V	

1) The indicated default levels are selected automatically after a power reset.

2) Due to variations of the tolerance of both the Embedded Voltage Regulators (EVR) and the PVC levels, this interrupt can be triggered inadvertently, even though the core voltage is within the normal range. It is, therefore, recommended not to use the this warning level.



|--|

Parameter	Symbol		Values		Unit	Note / Test Condition
		Min.	Тур.	Max.		
Number of erase cycles	N _{Er} SR	-	-	15 000	cycle s	$t_{RET} \ge 5$ years; Valid for up to 64 user- selected sectors (data storage)
		_	_	1 000	cycle s	$t_{RET} \ge 20$ years

 All Flash module(s) can be erased/programmed while code is executed and/or data is read from only one Flash module or from PSRAM. The Flash module that delivers code/data can, of course, not be erased/programmed.

 Flash module 3 can be erased/programmed while code is executed and/or data is read from any other Flash module.

3) Value of IMB_IMBCTRL.WSFLASH.

4) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticably only at extremely low system clock frequencies.

Access to the XE164xM Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.



PLL frequency band selection

Different frequency bands can be selected for the VCO so that the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
VCO output frequency	$f_{\rm VCO}$ CC	50	-	110	MHz	$VCOSEL = 00_B$
(VCO controlled)		100	-	160	MHz	$VCOSEL = 01_B$
VCO output frequency	$f_{\rm VCO}$ CC	10	-	40	MHz	$VCOSEL = 00_B$
(VCO free-running)		20	-	80	MHz	$VCOSEL = 01_B$

Table 23 System PLL Parameters

4.6.2.2 Wakeup Clock

When wakeup operation is selected (SYSCON0.CLKSEL = 00_B), the system clock is derived from the low-frequency wakeup clock source:

 $f_{SYS} = f_{WU}$.

In this mode, a basic functionality can be maintained without requiring an external clock source and while minimizing the power consumption.

4.6.2.3 Selecting and Changing the Operating Frequency

When selecting a clock source and the clock generation method, the required parameters must be carefully written to the respective bit fields, to avoid unintended intermediate states.

Many applications change the frequency of the system clock (f_{SYS}) during operation in order to optimize system performance and power consumption. Changing the operating frequency also changes the switching currents, which influences the power supply.

To ensure proper operation of the on-chip EVRs while they generate the core voltage, the operating frequency shall only be changed in certain steps. This prevents overshoots and undershoots of the supply voltage.

To avoid the indicated problems, recommended sequences are provided which ensure the intended operation of the clock system interacting with the power system. Please refer to the Programmer's Guide.



Electrical Parameters







Table 34 USIC SSC Slave Mode Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.	1	Test Condition
Select input DX2 setup to first clock input DX1 transmit edge ¹⁾	<i>t</i> ₁₀ SR	7	-	-	ns	
Select input DX2 hold after last clock input DX1 receive edge ¹⁾	<i>t</i> ₁₁ SR	7	-	-	ns	
Receive data input setup time to shift clock receive edge ¹⁾	<i>t</i> ₁₂ SR	7	-	-	ns	
Data input DX0 hold time from clock input DX1 receive edge ¹⁾	<i>t</i> ₁₃ SR	5	-	-	ns	
Data output DOUT valid time	<i>t</i> ₁₄ CC	8	-	41	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).



4.6.7 Debug Interface Timing

The debugger can communicate with the XE164xM either via the 2-pin DAP interface or via the standard JTAG interface.

Debug via DAP

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply; C_L = 20 pF.

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
DAP0 clock period	<i>t</i> ₁₁ SR	25 ¹⁾	-	-	ns	
DAP0 high time	t ₁₂ SR	8	-	-	ns	
DAP0 low time	t ₁₃ SR	8	-	-	ns	
DAP0 clock rise time	<i>t</i> ₁₄ SR	-	-	4	ns	
DAP0 clock fall time	<i>t</i> ₁₅ SR	-	-	4	ns	
DAP1 setup to DAP0 rising edge	<i>t</i> ₁₆ SR	6	-	-	ns	pad_type= stan dard
DAP1 hold after DAP0 rising edge	<i>t</i> ₁₇ SR	6	-	-	ns	pad_type= stan dard
DAP1 valid per DAP0 clock period ²⁾	<i>t</i> ₁₉ CC	17	20	-	ns	pad_type= stan dard

 Table 35
 DAP Interface Timing for Upper Voltage Range

1) The debug interface cannot operate faster than the overall system, therefore $t_{11} \ge t_{SYS}$.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.



Electrical Parameters



Figure 28 DAP Timing Host to Device



Figure 29 DAP Timing Device to Host

Note: The transmission timing is determined by the receiving debugger by evaluating the sync-request synchronization pattern telegram.