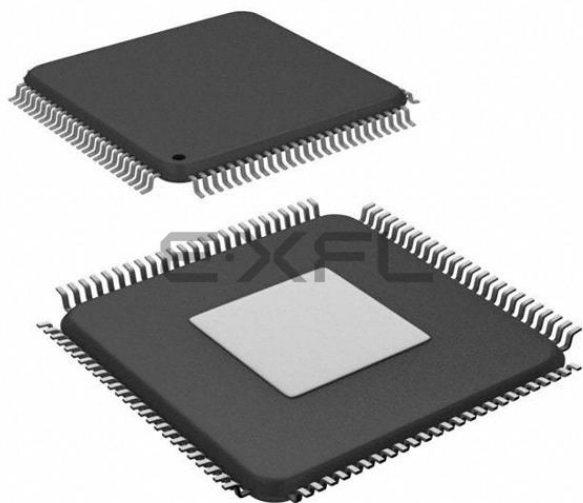




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Details

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xe164km-24f80l-aa

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XE164xM

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39	ID registers added
86	ADC capacitances corrected (typ. vs. max.)
90	Conditions relaxed for Δf_{INT} Range for f_{WU} adapted according to PCN 2010-013-A Added startup time from power-on t_{SPO}
127	Quality declarations added

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1.1 Basic Device Types

Basic device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 1 Synopsis of XE164xM Basic Device Types

Derivative¹⁾	Flash Memory²⁾	PSRAM DSRAM³⁾	Capt./Comp. Modules	ADC⁴⁾ Chan.	Interfaces⁴⁾
XE164FM-72FxxL	576 Kbytes	32 Kbytes 16 Kbytes	CC2 CCU60/1/2	11 + 5	4 CAN Nodes, 6 Serial Chan.
XE164FM-48FxxL	384 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1/2	11 + 5	4 CAN Nodes, 6 Serial Chan.
XE164FM-24FxxL	192 Kbytes	8 Kbytes 16 Kbytes	CC2 CCU60/1/2	11 + 5	4 CAN Nodes, 6 Serial Chan.
XE164GM-72FxxL	576 Kbytes	32 Kbytes 16 Kbytes	CC2 CCU60/1	6 + 5	2 CAN Nodes, 4 Serial Chan.
XE164GM-48FxxL	384 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1	6 + 5	2 CAN Nodes, 4 Serial Chan.
XE164GM-24FxxL	192 Kbytes	8 Kbytes 16 Kbytes	CC2 CCU60/1	6 + 5	2 CAN Nodes, 4 Serial Chan.
XE164HM-72FxxL	576 Kbytes	32 Kbytes 16 Kbytes	CC2 CCU60/1/2	11 + 5	No CAN Nodes, 6 Serial Chan.
XE164HM-48FxxL	384 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1/2	11 + 5	No CAN Nodes, 6 Serial Chan.
XE164HM-24FxxL	192 Kbytes	8 Kbytes 16 Kbytes	CC2 CCU60/1/2	11 + 5	No CAN Nodes, 6 Serial Chan.
XE164KM-72FxxL	576 Kbytes	32 Kbytes 16 Kbytes	CC2 CCU60/1	6 + 5	No CAN Nodes, 6 Serial Chan.
XE164KM-48FxxL	384 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1	6 + 5	No CAN Nodes, 6 Serial Chan.
XE164KM-24FxxL	192 Kbytes	8 Kbytes 16 Kbytes	CC2 CCU60/1	6 + 5	No CAN Nodes, 6 Serial Chan.

1) xx is a placeholder for the available speed grade (in MHz).

2) Specific information about the on-chip Flash memory in [Table 2](#).

3) All derivatives additionally provide 8 Kbytes SBRAM and 2 Kbytes DPRAM.

4) Specific information about the available channels in [Table 4](#).

Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

Summary of Features

The XE164xM types are offered with several SRAM memory sizes. **Figure 1** shows the allocation rules for PSRAM and DSRAM. Note that the rules differ:

- PSRAM allocation starts from the **lower** address
- DSRAM allocation starts from the **higher** address

For example 8 Kbytes of PSRAM will be allocated at E0'0000h-E0'1FFFh and 8 Kbytes of DSRAM will be at 00'C000h-00'DFFFh.

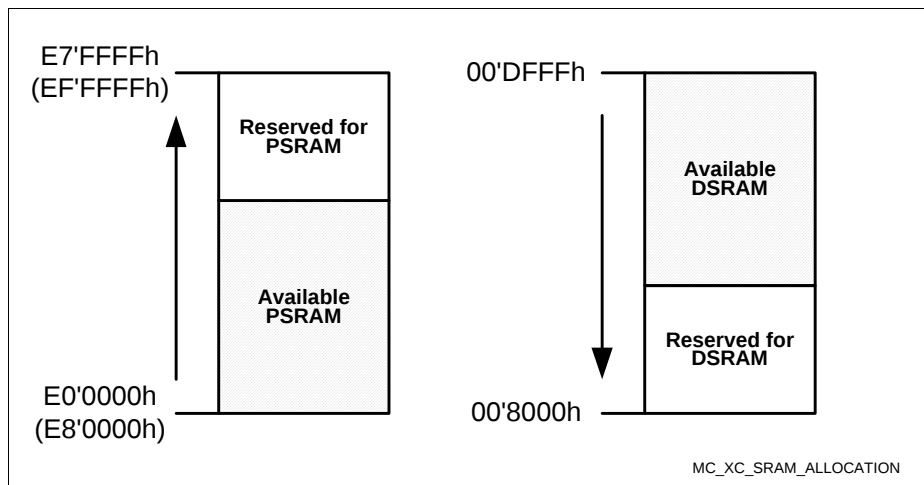


Figure 1 **SRAM Allocation**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
48	P2.6	O0 / I	St/B	Bit 6 of Port 2, General Purpose Input/Output
	U0C0_SELO0	O1	St/B	USIC0 Channel 0 Select/Control 0 Output
	U0C1_SELO1	O2	St/B	USIC0 Channel 1 Select/Control 1 Output
	CC2_CC19	O3 / I	St/B	CAPCOM2 CC19IO Capture Inp./ Compare Out.
	A19	OH	St/B	External Bus Interface Address Line 19
	U0C0_DX2D	I	St/B	USIC0 Channel 0 Shift Control Input
	RxDC0D	I	St/B	CAN Node 0 Receive Data Input
	ESR2_6	I	St/B	ESR2 Trigger Input 6
49	P4.3	O0 / I	St/B	Bit 3 of Port 4, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	CC2_CC27	O3 / I	St/B	CAPCOM2 CC27IO Capture Inp./ Compare Out.
	CS3	OH	St/B	External Bus Interface Chip Select 3 Output
	RxDC2A	I	St/B	CAN Node 2 Receive Data Input
	T2EUDA	I	St/B	GPT12E Timer T2 External Up/Down Control Input
	CCU62_CCP0S2B	I	St/B	CCU62 Position Input 2
53	P0.0	O0 / I	St/B	Bit 0 of Port 0, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	CCU61_CC60	O3	St/B	CCU61 Channel 0 IOutput
	A0	OH	St/B	External Bus Interface Address Line 0
	U1C0_DX0A	I	St/B	USIC1 Channel 0 Shift Data Input
	CCU61_CC60INA	I	St/B	CCU61 Channel 0 Input
	ESR1_11	I	St/B	ESR1 Trigger Input 11

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
54	P2.7	O0 / I	St/B	Bit 7 of Port 2, General Purpose Input/Output
	U0C1_SELO0	O1	St/B	USIC0 Channel 1 Select/Control 0 Output
	U0C0_SELO1	O2	St/B	USIC0 Channel 0 Select/Control 1 Output
	CC2_CC20	O3 / I	St/B	CAPCOM2 CC20IO Capture Inp./ Compare Out.
	A20	OH	St/B	External Bus Interface Address Line 20
	U0C1_DX2C	I	St/B	USIC0 Channel 1 Shift Control Input
	RxDC1C	I	St/B	CAN Node 1 Receive Data Input
	ESR2_7	I	St/B	ESR2 Trigger Input 7
55	P0.1	O0 / I	St/B	Bit 1 of Port 0, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CCU61_CC61	O3	St/B	CCU61 Channel 1 Output
	A1	OH	St/B	External Bus Interface Address Line 1
	U1C0_DX0B	I	St/B	USIC1 Channel 0 Shift Data Input
	CCU61_CC61INA	I	St/B	CCU61 Channel 1 Input
	U1C0_DX1A	I	St/B	USIC1 Channel 0 Shift Clock Input
56	P2.8	O0 / I	DP/B	Bit 8 of Port 2, General Purpose Input/Output
	U0C1_SCLKOUT	O1	DP/B	USIC0 Channel 1 Shift Clock Output
	EXTCLK	O2	DP/B	Programmable Clock Signal Output¹⁾
	CC2_CC21	O3 / I	DP/B	CAPCOM2 CC21IO Capture Inp./ Compare Out.
	A21	OH	DP/B	External Bus Interface Address Line 21
	U0C1_DX1D	I	DP/B	USIC0 Channel 1 Shift Clock Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
57	P2.9	O0 / I	St/B	Bit 9 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	CC2_CC22	O3 / I	St/B	CAPCOM2 CC22IO Capture Inp./ Compare Out.
	A22	OH	St/B	External Bus Interface Address Line 22
	CLKIN1	I	St/B	Clock Signal Input 1
	TCK_A	IH	St/B	DAP0/JTAG Clock Input If JTAG pos. A is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 0 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
58	P0.2	O0 / I	St/B	Bit 2 of Port 0, General Purpose Input/Output
	U1C0_SCLK OUT	O1	St/B	USIC1 Channel 0 Shift Clock Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CCU61_CC6 2	O3	St/B	CCU61 Channel 2 Output
	A2	OH	St/B	External Bus Interface Address Line 2
	U1C0_DX1B	I	St/B	USIC1 Channel 0 Shift Clock Input
	CCU61_CC6 2INA	I	St/B	CCU61 Channel 2 Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
70	P10.5	O0 / I	St/B	Bit 5 of Port 10, General Purpose Input/Output
	U0C1_SCLK OUT	O1	St/B	USIC0 Channel 1 Shift Clock Output
	CCU60_COU T62	O2	St/B	CCU60 Channel 2 Output
	U2C0_DOUT	O3	St/B	USIC2 Channel 0 Shift Data Output
	AD5	OH / IH	St/B	External Bus Interface Address/Data Line 5
	U0C1_DX1B	I	St/B	USIC0 Channel 1 Shift Clock Input
71	P0.6	O0 / I	St/B	Bit 6 of Port 0, General Purpose Input/Output
	U1C1_DOUT	O1	St/B	USIC1 Channel 1 Shift Data Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	CCU61_COU T63	O3	St/B	CCU61 Channel 3 Output
	A6	OH	St/B	External Bus Interface Address Line 6
	U1C1_DX0A	I	St/B	USIC1 Channel 1 Shift Data Input
	CCU61_CTR APA	I	St/B	CCU61 Emergency Trap Input
	U1C1_DX1B	I	St/B	USIC1 Channel 1 Shift Clock Input
72	P10.6	O0 / I	St/B	Bit 6 of Port 10, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	U1C0_SELO 0	O3	St/B	USIC1 Channel 0 Select/Control 0 Output
	AD6	OH / IH	St/B	External Bus Interface Address/Data Line 6
	U0C0_DX0C	I	St/B	USIC0 Channel 0 Shift Data Input
	U1C0_DX2D	I	St/B	USIC1 Channel 0 Shift Control Input
	CCU60_CTR APA	I	St/B	CCU60 Emergency Trap Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
84	P1.2	O0 / I	St/B	Bit 2 of Port 1, General Purpose Input/Output
	CCU62_CC62	O1	St/B	CCU62 Channel 2 Output
	U1C0_SELO6	O2	St/B	USIC1 Channel 0 Select/Control 6 Output
	U2C1_SCLKOUT	O3	St/B	USIC2 Channel 1 Shift Clock Output
	A10	OH	St/B	External Bus Interface Address Line 10
	ESR1_4	I	St/B	ESR1 Trigger Input 4
	CCU61_T12HRB	I	St/B	External Run Control Input for T12 of CCU61
	CCU62_CC62INA	I	St/B	CCU62 Channel 2 Input
	U2C1_DX0D	I	St/B	USIC2 Channel 1 Shift Data Input
	U2C1_DX1C	I	St/B	USIC2 Channel 1 Shift Clock Input
85	P10.12	O0 / I	St/B	Bit 12 of Port 10, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	TxDC2	O2	St/B	CAN Node 2 Transmit Data Output
	TDO_B	OH / IH	St/B	JTAG Test Data Output / DAP1 Input/Output If DAP pos. 1 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	AD12	OH / IH	St/B	External Bus Interface Address/Data Line 12
	U1C0_DX0C	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX1E	I	St/B	USIC1 Channel 0 Shift Clock Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
97	PORST	I	In/B	Power On Reset Input A low level at this pin resets the XE164xM completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pull-up device will hold this pin high when nothing is driving it.
98	ESR1	O0 / I	St/B	External Service Request 1 After power-up, an internal weak pull-up device holds this pin high when nothing is driving it.
	RxDC0E	I	St/B	CAN Node 0 Receive Data Input
	U1C0_DX0F	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX2C	I	St/B	USIC1 Channel 0 Shift Control Input
	U1C1_DX0C	I	St/B	USIC1 Channel 1 Shift Data Input
	U1C1_DX2B	I	St/B	USIC1 Channel 1 Shift Control Input
	U2C1_DX2C	I	St/B	USIC2 Channel 1 Shift Control Input
99	ESR0	O0 / I	St/B	External Service Request 0 After power-up, ESR0 operates as open-drain bidirectional reset with a weak pull-up.
	U1C0_DX0E	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX2B	I	St/B	USIC1 Channel 0 Shift Control Input
10	V _{DDIM}	-	PS/M	Digital Core Supply Voltage for Domain M Decouple with a ceramic capacitor, see Data Sheet for details.
38, 64, 88	V _{DDI1}	-	PS/1	Digital Core Supply Voltage for Domain 1 Decouple with a ceramic capacitor, see Data Sheet for details. All V _{DDI1} pins must be connected to each other.
14	V _{DDPA}	-	PS/A	Digital Pad Supply Voltage for Domain A Connect decoupling capacitors to adjacent V _{DDP} /V _{SS} pin pairs as close as possible to the pins. <i>Note: The A/D Converters and ports P5, P6 and P15 are fed from supply voltage V_{DDPA}.</i>

Functional Description

Table 8 Compare Modes (cont'd)

Compare Modes	Function
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode

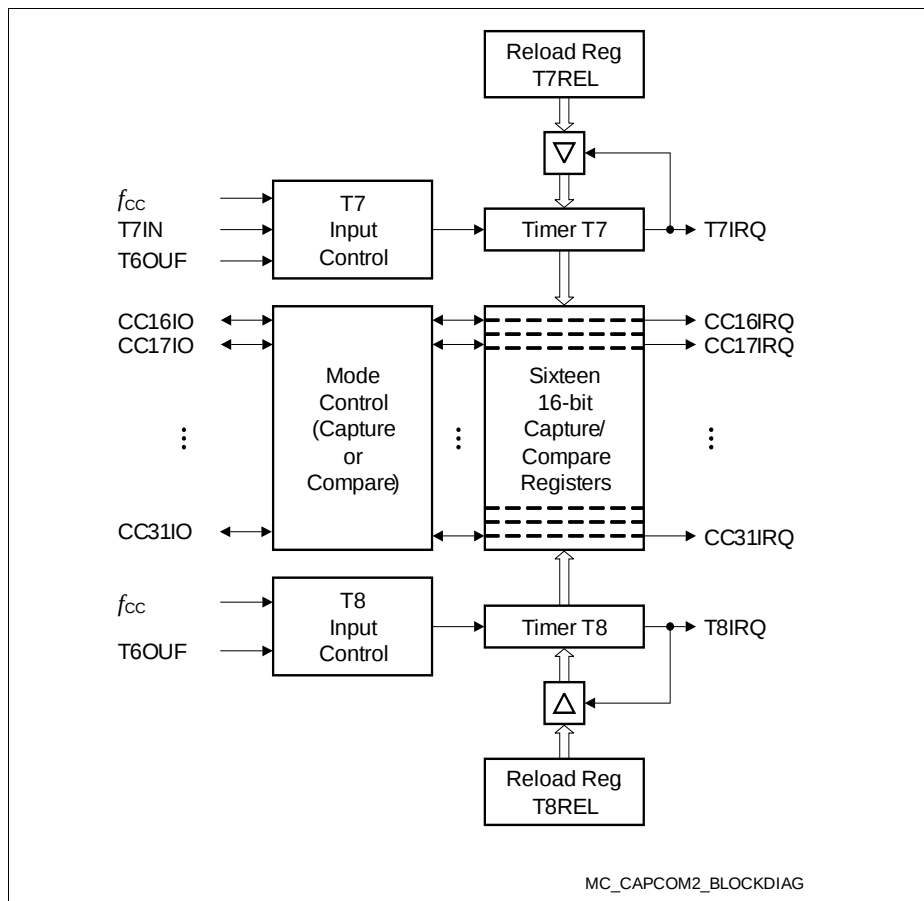


Figure 6 CAPCOM2 Unit Block Diagram

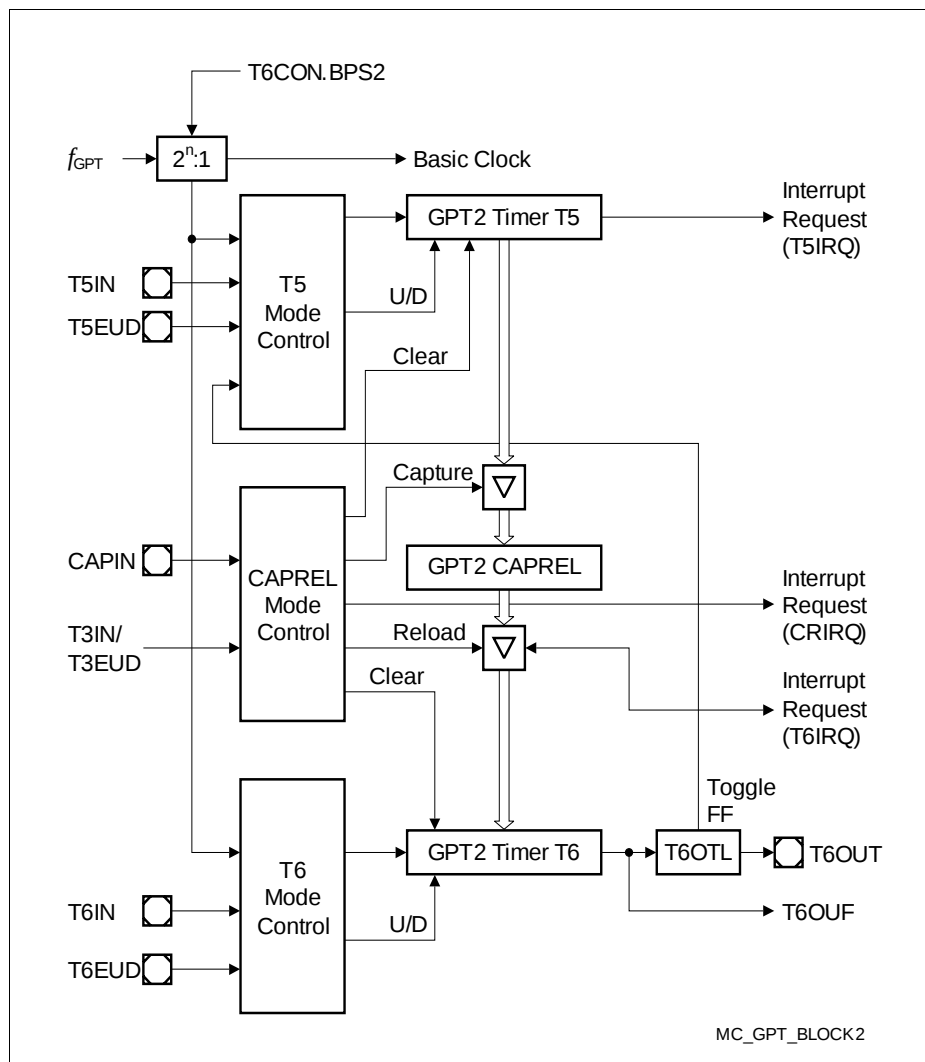


Figure 9 Block Diagram of GPT2

Functional Description

Table 10 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

- 1) The Enter Power Down Mode instruction is not used in the XE164xM, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

4 Electrical Parameters

The operating range for the XE164xM is defined by its electrical parameters. For proper operation the specified limits must be respected when integrating the device in its target environment.

4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

4.1.1 Absolut Maximum Rating Conditions

Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability.

During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 11 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output current on a pin when high value is driven	I_{OH} SR	-30	—	—	mA	
Output current on a pin when low value is driven	I_{OL} SR	—	—	30	mA	
Overload current	I_{OV} SR	-10	—	10	mA	¹⁾
Absolute sum of overload currents	$\Sigma I_{OV} $ SR	—	—	100	mA	¹⁾
Junction Temperature	T_J SR	-40	—	150	°C	
Storage Temperature	T_{ST} SR	-65	—	150	°C	
Digital supply voltage for IO pads and voltage regulators	V_{DDPA} , V_{DDPB} SR	-0.5	—	6.0	V	
Voltage on any pin with respect to ground (V_{SS})	V_{IN} SR	-0.5	—	$V_{DDP} + 0.5$	V	$V_{IN} \leq V_{DDP(max)}$

1) Overload condition occurs if the input voltage V_{IN} is out of the absolute maximum rating range. In this case the current must be limited to the listed values by design measures.

Electrical Parameters

Table 12 Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Absolute sum of overload currents	$\Sigma I_{OV} $ SR	–	–	50	mA	not subject to production test
Digital core supply voltage for domain M ⁸⁾	V_{DDIM} CC	–	1.5	–		
Digital core supply voltage for domain 1 ⁸⁾	V_{DDI1} CC	–	1.5	–		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	4.5	–	5.5	V	
Digital ground voltage	V_{SS} SR	–	0	–	V	

- 1) To ensure the stability of the voltage regulators the EVRs must be buffered with ceramic capacitors. Separate buffer capacitors with the recommended values shall be connected as close as possible to each V_{DDIM} and V_{DDI1} pin to keep the resistance of the board tracks below 2 Ohm. Connect all V_{DDI1} pins together. The minimum capacitance value is required for proper operation under all conditions (e.g. temperature). Higher values slightly increase the startup time.
- 2) Use one Capacitor for each pin.
- 3) This is the reference load. For bigger capacitive loads, use the derating factors listed in the PAD properties section.
- 4) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).
- 5) The operating frequency range may be reduced for specific device types. This is indicated in the device designation (...FxxL). 80 MHz devices are marked ...F80L.
- 6) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{IHmax}$ ($I_{OV} > 0$) or $V_{OV} < V_{ILmin}$ ($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed 50 mA. The supply voltages must remain within the specified limits. Proper operation under overload conditions depends on the application. Overload conditions must not occur on pin XTAL1 (powered by V_{DDIM}).
- 7) An overload current (I_{OV}) through a pin injects a certain error current (I_{INj}) into the adjacent pins. This error current adds to the respective pins leakage current (I_{OZ}). The amount of error current depends on the overload current and is defined by the overload coupling factor K_{OV} . The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it. The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \cdot K_{OV})$. The additional error current may distort the input voltage on analog inputs.
- 8) Value is controlled by on-chip regulator

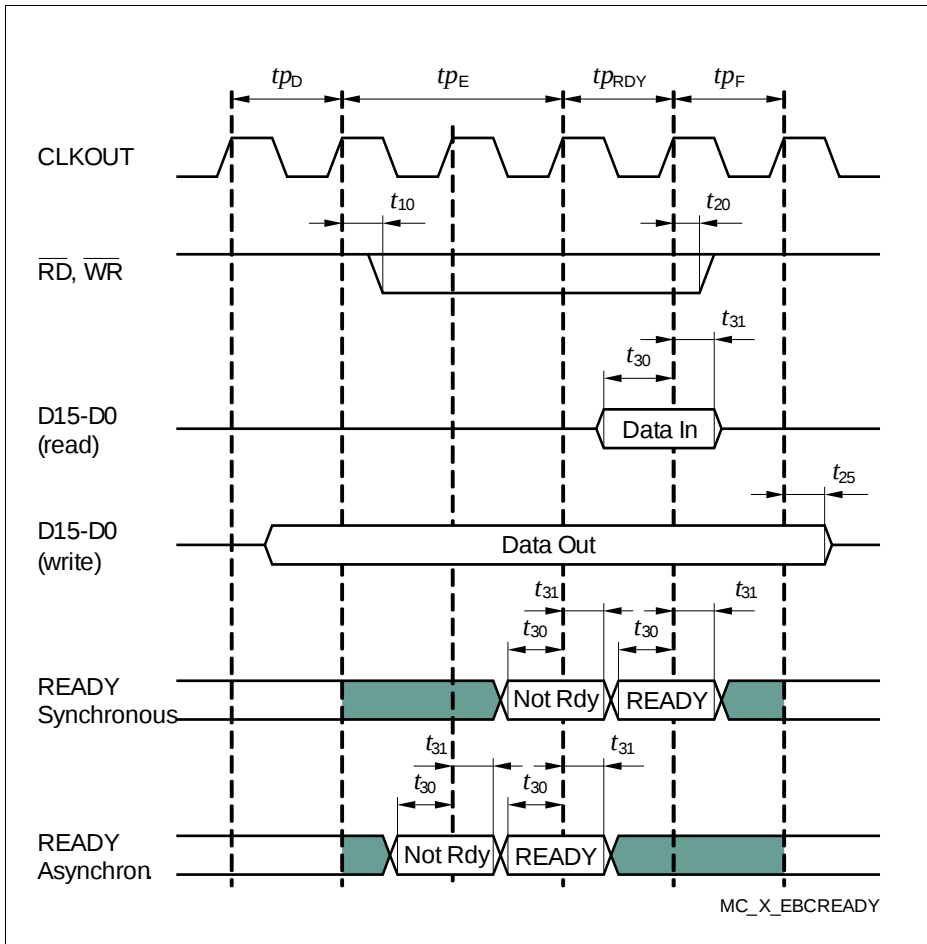


Figure 25 READY Timing

Note: If the READY input is sampled inactive at the indicated sampling point ("Not Rdy") a READY-controlled waitstate is inserted (tp_{RDY}), sampling the READY input active at the indicated sampling point ("Ready") terminates the currently running bus cycle. Note the different sampling points for synchronous and asynchronous READY. This example uses one mandatory waitstate (see tp_E) before the READY input value is used.

5 Package and Reliability

The XE166 Family devices use the package type PG-LQFP (Plastic Green - Low Profile Quad Flat Package). The following specifications must be regarded to ensure proper integration of the XE164xM in its target environment.

5.1 Packaging

These parameters specify the packaging rather than the silicon.

Table 39 Package Parameters (PG-LQFP-100-8)

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Exposed Pad Dimension	$E_x \times E_y$	–	6.2×6.2	mm	–
Power Dissipation	P_{DISS}	–	1.0	W	–
Thermal resistance Junction-Ambient	$R_{\Theta JA}$	–	47	K/W	No thermal via ¹⁾
			29	K/W	4-layer, no pad ²⁾
			23	K/W	4-layer, pad ³⁾

1) Device mounted on a 2-layer JEDEC board (according to JESD 51-3) or a 4-layer board without thermal vias; exposed pad not soldered.

2) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad not soldered.

3) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad soldered to the board.

Note: To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground, independent of the thermal requirements.

Board layout examples are given in an application note.

Package Compatibility Considerations

The XE164xM is a member of the XE166 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Pad (if present) may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.