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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe164fm72f80lrabkxuma1

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16-Bit Single-Chip
Real Time Signal Controller
XE164xM (XE166 Family)

1 Summary of Features

For a quick overview and easy reference, the features of the XE164xM are summarized here.

- High-performance CPU with five-stage pipeline and MPU
 - 12.5 ns instruction cycle at 80 MHz CPU clock (single-cycle execution)
 - One-cycle 32-bit addition and subtraction with 40-bit result
 - One-cycle multiplication (16×16 bit)
 - Background division ($32 / 16$ bit) in 21 cycles
 - One-cycle multiply-and-accumulate (MAC) instructions
 - Enhanced Boolean bit manipulation facilities
 - Zero-cycle jump execution
 - Additional instructions to support HLL and operating systems
 - Register-based design with multiple variable register banks
 - Fast context switching support with two additional local register banks
 - 16 Mbytes total linear address space for code and data
 - 1024 Bytes on-chip special function register area (C166 Family compatible)
 - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels for up to 96 sources
 - Selectable external inputs for interrupt generation and wake-up
 - Fastest sample-rate 12.5 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
 - 8 Kbytes on-chip stand-by RAM (SBRAM)
 - 2 Kbytes on-chip dual-port RAM (DPRAM)
 - Up to 16 Kbytes on-chip data SRAM (DSRAM)
 - Up to 32 Kbytes on-chip program/data SRAM (PSRAM)
 - Up to 576 Kbytes on-chip program memory (Flash memory)
 - Memory content protection through Error Correction Code (ECC)
- On-Chip Peripheral Modules
 - Multi-functional general purpose timer unit with 5 timers
 - 16-channel general purpose capture/compare unit (CAPCOM2)

Summary of Features

- Up to 3 capture/compare units for flexible PWM signal generation (CCU6x)
- Two Synchronizable A/D Converters with a total of up to 16 channels, 10-bit resolution, conversion time below 1 μ s, optional data preprocessing (data reduction, range check), broken wire detection
- Up to 6 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
- On-chip MultiCAN interface (Rev. 2.0B active) with up to 128 message objects (Full CAN/Basic CAN) on up to 4 CAN nodes and gateway functionality
- On-chip system timer and on-chip real time clock
- Up to 12 Mbytes external address space for code and data
 - Programmable external bus characteristics for different address ranges
 - Multiplexed or demultiplexed external address/data buses
 - Selectable address bus width
 - 16-bit or 8-bit data bus width
 - Four programmable chip-select signals
- Single power supply from 3.0 V to 5.5 V
- Programmable watchdog timer and oscillator watchdog
- Up to 76 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via Device Access Port (DAP) or JTAG interface
- 100-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the function set of the corresponding product type
- the temperature range:
 - SAF-...: -40°C to 85°C
 - SAK-...: -40°C to 125°C
- the package and the type of delivery.

For ordering codes for the XE164xM please contact your sales representative or local distributor.

This document describes several derivatives of the XE164xM group:

Table 1 lists these derivatives and summarizes the differences.

As this document refers to all of these derivatives, some descriptions may not apply to a specific product, in particular to the special device types.

For simplicity the term **XE164xM** is used for all derivatives throughout this document.

XE164xM device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
6	P7.0	O0 / I	St/B	Bit 0 of Port 7, General Purpose Input/Output
	T3OUT	O1	St/B	GPT12E Timer T3 Toggle Latch Output
	T6OUT	O2	St/B	GPT12E Timer T6 Toggle Latch Output
	TDO_A	OH / IH	St/B	JTAG Test Data Output / DAP1 Input/Output If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	ESR2_1	I	St/B	ESR2 Trigger Input 1
7	P7.3	O0 / I	St/B	Bit 3 of Port 7, General Purpose Input/Output
	EMUX1	O1	St/B	External Analog MUX Control Output 1 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_DOUT	O3	St/B	USIC0 Channel 0 Shift Data Output
	CCU62_CCP OS1A	I	St/B	CCU62 Position Input 1
	TMS_C	I/H	St/B	JTAG Test Mode Selection Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	U0C1_DX0F	I	St/B	USIC0 Channel 1 Shift Data Input
8	P7.1	O0 / I	St/B	Bit 1 of Port 7, General Purpose Input/Output
	EXTCLK	O1	St/B	Programmable Clock Signal Output
	CCU62_CTR APA	I	St/B	CCU62 Emergency Trap Input
	BRKIN_C	I	St/B	OCDS Break Signal Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
9	P7.4	O0 / I	St/B	Bit 4 of Port 7, General Purpose Input/Output
	EMUX2	O1	St/B	External Analog MUX Control Output 2 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C1_SCLK OUT	O3	St/B	USIC0 Channel 1 Shift Clock Output
	CCU62_CCP OS2A	I	St/B	CCU62 Position Input 2
	TCK_C	IH	St/B	DAP0/JTAG Clock Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	U0C0_DX0D	I	St/B	USIC0 Channel 0 Shift Data Input
11	U0C1_DX1E	I	St/B	USIC0 Channel 1 Shift Clock Input
	P6.0	O0 / I	DA/A	Bit 0 of Port 6, General Purpose Input/Output
	EMUX0	O1	DA/A	External Analog MUX Control Output 0 (ADC0)
	TxDC2	O2	DA/A	CAN Node 2 Transmit Data Output
	BRKOUT	O3	DA/A	OCDS Break Signal Output
	ADCx_REQG TyG	I	DA/A	External Request Gate Input for ADC0/1
	U1C1_DX0E	I	DA/A	USIC1 Channel 1 Shift Data Input
12	P6.1	O0 / I	DA/A	Bit 1 of Port 6, General Purpose Input/Output
	EMUX1	O1	DA/A	External Analog MUX Control Output 1 (ADC0)
	T3OUT	O2	DA/A	GPT12E Timer T3 Toggle Latch Output
	U1C1_DOUT	O3	DA/A	USIC1 Channel 1 Shift Data Output
	ADCx_REQT RyE	I	DA/A	External Request Trigger Input for ADC0/1
	RxDC2E	I	DA/A	CAN Node 2 Receive Data Input
	ESR1_6	I	DA/A	ESR1 Trigger Input 6

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
24	P5.3	I	In/A	Bit 3 of Port 5, General Purpose Input
	ADC0_CH3	I	In/A	Analog Input Channel 3 for ADC0
	T3INA	I	In/A	GPT12E Timer T3 Count/Gate Input
28	P5.4	I	In/A	Bit 4 of Port 5, General Purpose Input
	ADC0_CH4	I	In/A	Analog Input Channel 4 for ADC0
	T3EUDA	I	In/A	GPT12E Timer T3 External Up/Down Control Input
	TMS_A	I	In/A	JTAG Test Mode Selection Input
29	P5.5	I	In/A	Bit 5 of Port 5, General Purpose Input
	ADC0_CH5	I	In/A	Analog Input Channel 5 for ADC0
	CCU60_T12 HRB	I	In/A	External Run Control Input for T12 of CCU60
30	P5.8	I	In/A	Bit 8 of Port 5, General Purpose Input
	ADC0_CH8	I	In/A	Analog Input Channel 8 for ADC0
	ADC1_CH8	I	In/A	Analog Input Channel 8 for ADC1
	CCU6x_T12H RC	I	In/A	External Run Control Input for T12 of CCU60/1/2
	CCU6x_T13H RC	I	In/A	External Run Control Input for T13 of CCU60/1/2
	U2C0_DX0F	I	In/A	USIC2 Channel 0 Shift Data Input
31	P5.9	I	In/A	Bit 9 of Port 5, General Purpose Input
	ADC0_CH9	I	In/A	Analog Input Channel 9 for ADC0
	ADC1_CH9	I	In/A	Analog Input Channel 9 for ADC1
	CC2_T7IN	I	In/A	CAPCOM2 Timer T7 Count Input
32	P5.10	I	In/A	Bit 10 of Port 5, General Purpose Input
	ADC0_CH10	I	In/A	Analog Input Channel 10 for ADC0
	ADC1_CH10	I	In/A	Analog Input Channel 10 for ADC1
	BRKIN_A	I	In/A	OCDS Break Signal Input
	U2C1_DX0F	I	In/A	USIC2 Channel 1 Shift Data Input
	CCU61_T13 HRA	I	In/A	External Run Control Input for T13 of CCU61

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
67	P10.3	O0 / I	St/B	Bit 3 of Port 10, General Purpose Input/Output
	CCU60_COUT60	O2	St/B	CCU60 Channel 0 Output
	AD3	OH / IH	St/B	External Bus Interface Address/Data Line 3
	U0C0_DX2A	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX2A	I	St/B	USIC0 Channel 1 Shift Control Input
68	P0.5	O0 / I	St/B	Bit 5 of Port 0, General Purpose Input/Output
	U1C1_SCLKOUT	O1	St/B	USIC1 Channel 1 Shift Clock Output
	U1C0_SELO2	O2	St/B	USIC1 Channel 0 Select/Control 2 Output
	CCU61_COUT62	O3	St/B	CCU61 Channel 2 Output
	A5	OH	St/B	External Bus Interface Address Line 5
	U1C1_DX1A	I	St/B	USIC1 Channel 1 Shift Clock Input
	U1C0_DX1C	I	St/B	USIC1 Channel 0 Shift Clock Input
	RXDC3E	I	St/B	CAN Node 3 Receive Data Input
69	P10.4	O0 / I	St/B	Bit 4 of Port 10, General Purpose Input/Output
	U0C0_SELO3	O1	St/B	USIC0 Channel 0 Select/Control 3 Output
	CCU60_COUT61	O2	St/B	CCU60 Channel 1 Output
	AD4	OH / IH	St/B	External Bus Interface Address/Data Line 4
	U0C0_DX2B	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX2B	I	St/B	USIC0 Channel 1 Shift Control Input
	ESR1_9	I	St/B	ESR1 Trigger Input 9

3.4 Memory Protection Unit (MPU)

The XE164xM's Memory Protection Unit (MPU) protects user-specified memory areas from unauthorized read, write, or instruction fetch accesses. The MPU can protect the whole address space including the peripheral area. This completes established mechanisms such as the register security mechanism or stack overrun/underrun detection.

Four Protection Levels support flexible system programming where operating system, low level drivers, and applications run on separate levels. Each protection level permits different access restrictions for instructions and/or data.

Every access is checked (if the MPU is enabled) and an access violating the permission rules will be marked as invalid and leads to a protection trap.

A set of protection registers for each protection level specifies the address ranges and the access permissions. Applications requiring more than 4 protection levels can dynamically re-program the protection registers.

3.5 Memory Checker Module (MCHK)

The XE164xM's Memory Checker Module calculates a checksum (fractional polynomial division) on a block of data, often called Cyclic Redundancy Code (CRC). It is based on a 32-bit linear feedback shift register and may, therefore, also be used to generate pseudo-random numbers.

The Memory Checker Module is a 16-bit parallel input signature compression circuitry which enables error detection within a block of data stored in memory, registers, or communicated e.g. via serial communication lines. It reduces the probability of error masking due to repeated error patterns by calculating the signature of blocks of data.

The polynomial used for operation is configurable, so most of the commonly used polynomials may be used. Also, the block size for generating a CRC result is configurable via a local counter. An interrupt may be generated if testing the current data block reveals an error.

An autonomous CRC compare circuitry is included to enable redundant error detection, e.g. to enable higher safety integrity levels.

The Memory Checker Module provides enhanced fault detection (beyond parity or ECC) for data and instructions in volatile and non volatile memories. This is especially important for the safety and reliability of embedded systems.

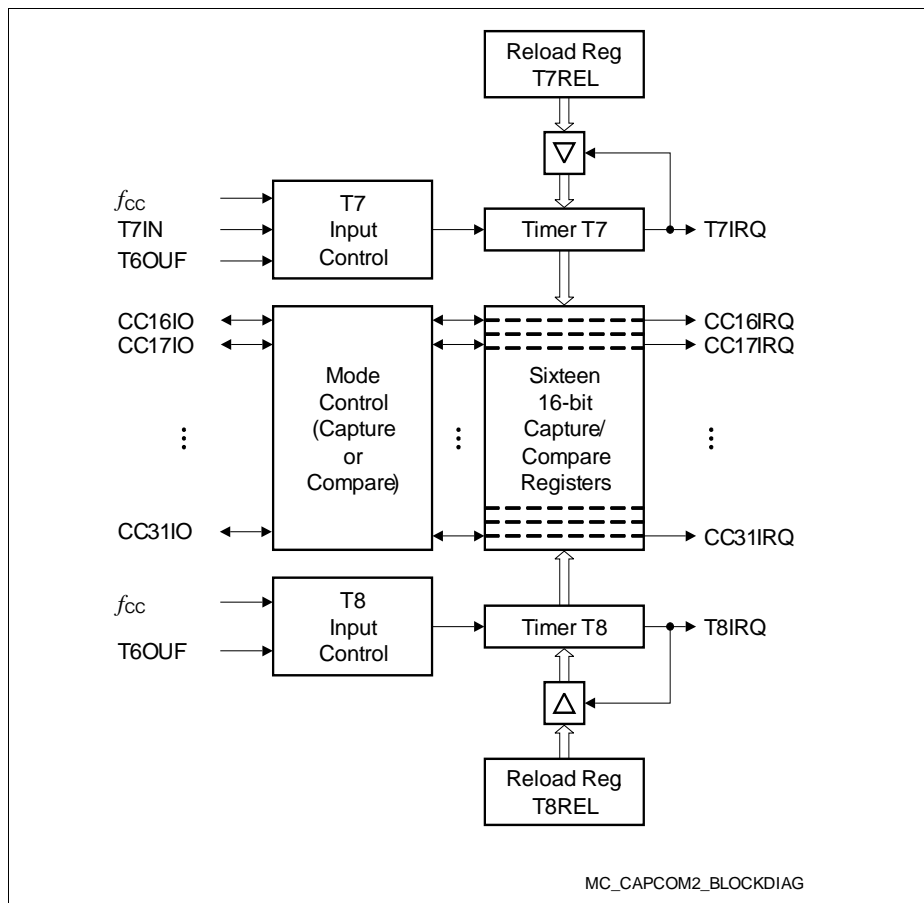


Figure 6 CAPCOM2 Unit Block Diagram

3.10 General Purpose Timer (GPT12E) Unit

The GPT12E unit is a very flexible multifunctional timer/counter structure which can be used for many different timing tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers organized in two separate modules, GPT1 and GPT2. Each timer in each module may either operate independently in a number of different modes or be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation: Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock and divided by a programmable prescaler. Counter Mode allows timer clocking in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes each timer has one associated port pin (TxIN) which serves as a gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The counting direction (up/down) for each timer can be programmed by software or altered dynamically by an external signal on a port pin (TxEUD), e.g. to facilitate position tracking.

In Incremental Interface Mode the GPT1 timers can be directly connected to the incremental position sensor signals A and B through their respective inputs TxIN and TxEUD. Direction and counting signals are internally derived from these two input signals, so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to the basic operating modes, T2 and T4 may be configured as reload or capture register for timer T3. A timer used as capture or reload register is stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at the associated input pin (TxIN). Timer T3 is reloaded with the contents of T2 or T4, triggered either by an external signal or a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be continuously generated without software intervention.

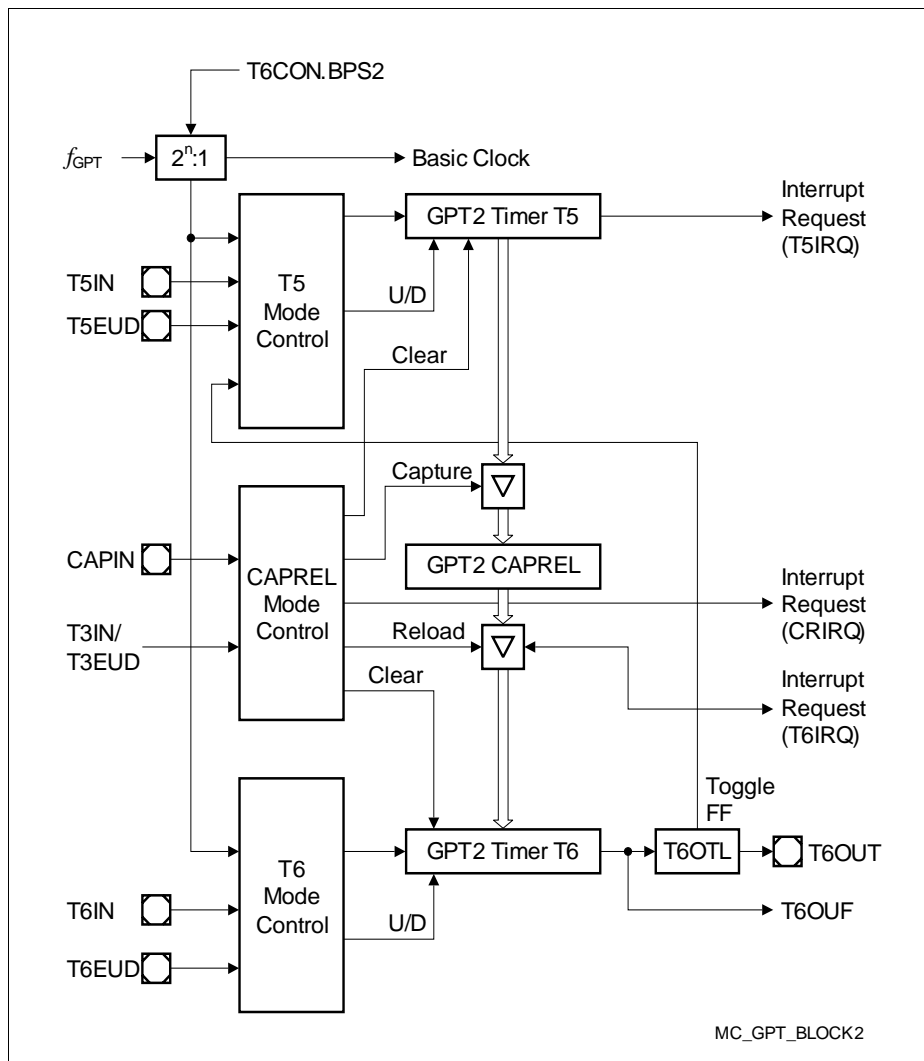


Figure 9 Block Diagram of GPT2

Functional Description

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time-based interrupt, to provide a system time tick independent of CPU frequency and other resources
- 48-bit timer for long-term measurements
- Alarm interrupt at a defined time

Electrical Parameters

Table 12 Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Absolute sum of overload currents	$\Sigma I_{OV} $ SR	—	—	50	mA	not subject to production test
Digital core supply voltage for domain M ⁸⁾	V_{DDIM} CC	—	1.5	—		
Digital core supply voltage for domain 1 ⁸⁾	V_{DDI1} CC	—	1.5	—		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	4.5	—	5.5	V	
Digital ground voltage	V_{SS} SR	—	0	—	V	

- 1) To ensure the stability of the voltage regulators the EVRs must be buffered with ceramic capacitors. Separate buffer capacitors with the recommended values shall be connected as close as possible to each V_{DDIM} and V_{DDI1} pin to keep the resistance of the board tracks below 2 Ohm. Connect all V_{DDI1} pins together. The minimum capacitance value is required for proper operation under all conditions (e.g. temperature). Higher values slightly increase the startup time.
- 2) Use one Capacitor for each pin.
- 3) This is the reference load. For bigger capacitive loads, use the derating factors listed in the PAD properties section.
- 4) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).
- 5) The operating frequency range may be reduced for specific device types. This is indicated in the device designation (...FxxL). 80 MHz devices are marked ...F80L.
- 6) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{IHmax}$ ($I_{OV} > 0$) or $V_{OV} < V_{ILmin}$ ($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed 50 mA. The supply voltages must remain within the specified limits. Proper operation under overload conditions depends on the application. Overload conditions must not occur on pin XTAL1 (powered by V_{DDIM}).
- 7) An overload current (I_{OV}) through a pin injects a certain error current (I_{INj}) into the adjacent pins. This error current adds to the respective pins leakage current (I_{OZ}). The amount of error current depends on the overload current and is defined by the overload coupling factor K_{OV} . The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it. The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \cdot K_{OV})$. The additional error current may distort the input voltage on analog inputs.
- 8) Value is controlled by on-chip regulator

4.1.3 Pad Timing Definition

If not otherwise noted, all timing parameters are tested and are valid for the corresponding output pins operating in strong driver, fast edge mode.

See also [“Pad Properties” on Page 103](#).

4.1.4 Parameter Interpretation

The parameters listed in the following include both the characteristics of the XE164xM and its demands on the system. To aid in correctly interpreting the parameters when evaluating them for a design, they are marked accordingly in the column “Symbol”:

CC (Controller Characteristics):

The logic of the XE164xM provides signals with the specified characteristics.

SR (System Requirement):

The external system must provide signals with the specified characteristics to the XE164xM.

Electrical Parameters

Table 14 DC Characteristics for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output Low Voltage ⁸⁾	$V_{OL\ CC}$	—	—	1.0	V	$I_{OL} \leq I_{OLmax}$
		—	—	0.4	V	$I_{OL} \leq I_{OLnom}$ ¹⁰⁾

- 1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.
- 2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.
- 3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{IN} < V_{SS}$) or supply ripple ($V_{IN} > V_{DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV} .
- 4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature (T_J = junction temperature [°C]): $I_{OZ} = 0.05 \times e^{(1.5 + 0.028 \times T_J)}$ [μA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 μA. Leakage derating depending on voltage level ($DV = V_{DDP} - V_{PIN}$ [V]): $I_{OZ} = I_{OZtempmax} - (1.6 \times DV)$ (μA). This voltage derating formula is an approximation which applies for maximum temperature.
- 5) Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pullup; $V_{PIN} \geq V_{IH}$ for a pulldown.
- 6) These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.
- 7) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pullup; $V_{PIN} \leq V_{IL}$ for a pulldown.
- 8) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
- 9) As a rule, with decreasing output current the output levels approach the respective supply level (VOL->VSS, VOH->VDDP). However, only the levels for nominal output currents are verified.
- 10) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are verified.

4.5 Flash Memory Parameters

The XE164xM is delivered with all Flash sectors erased and with no protection installed. The data retention time of the XE164xM's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 22 Flash Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Parallel Flash module program/erase limit depending on Flash read activity	N_{PP} SR	–	–	4 ¹⁾		$N_{FL_RD} \leq 1$, $f_{SYS} \leq 80$ MHz
		–	–	1 ²⁾		$N_{FL_RD} > 1$
Flash erase endurance for security pages	N_{SEC} SR	10	–	–	cycle s	$t_{RET} \geq 20$ years
Flash wait states ³⁾	N_{WSFLAS} H SR	1	–	–		$f_{SYS} \leq 8$ MHz
		2	–	–		$f_{SYS} \leq 13$ MHz
		3	–	–		$f_{SYS} \leq 17$ MHz
		4	–	–		$f_{SYS} > 17$ MHz
Erase time per sector/page	t_{ER} CC	–	7 ⁴⁾	8.0	ms	
Programming time per page	t_{PR} CC	–	3 ⁴⁾	3.5	ms	
Data retention time	t_{RET} CC	20	–	–	year s	$N_{Er} \leq 1\,000$ cycles
Drain disturb limit	N_{DD} SR	32	–	–	cycle s	

Table 25 is valid under the following conditions:

$V_{DDP} \geq 4.5 \text{ V}$; $V_{DDPtyp} = 5 \text{ V}$; $V_{DDP} \leq 5.5 \text{ V}$; $C_L \geq 20 \text{ pF}$; $C_L \leq 100 \text{ pF}$;

Table 25 Standard Pad Parameters for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output driver current (absolute value) ¹⁾	I_{Omax} CC	—	—	10	mA	Strong driver
		—	—	4.0	mA	Medium driver
		—	—	0.5	mA	Weak driver
Nominal output driver current (absolute value)	I_{Onom} CC	—	—	2.5	mA	Strong driver
		—	—	1.0	mA	Medium driver
		—	—	0.1	mA	Weak driver
Rise and Fall times (10% - 90%)	t_{RF} CC	—	—	$4.2 + 0.14 \times C_L$	ns	Strong driver; Sharp edge
		—	—	$11.6 + 0.22 \times C_L$	ns	Strong driver; Medium edge
		—	—	$20.6 + 0.22 \times C_L$	ns	Strong driver; Slow edge
		—	—	$23 + 0.6 \times C_L$	ns	Medium driver
		—	—	$212 + 1.9 \times C_L$	ns	Weak driver

1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and ΣI_{OH}) must remain below 50 mA.

Table 29 EBC External Bus Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output valid delay for \overline{RD} , $\overline{WR}(L/H)$	t_{10} CC	–	7	13	ns	
Output valid delay for BHE, ALE	t_{11} CC	–	7	14	ns	
Address output valid delay for A23 ... A0	t_{12} CC	–	8	14	ns	
Address output valid delay for AD15 ... AD0 (MUX mode)	t_{13} CC	–	8	15	ns	
Output valid delay for \overline{CS}	t_{14} CC	–	7	13	ns	
Data output valid delay for AD15 ... AD0 (write data, MUX mode)	t_{15} CC	–	8	15	ns	
Data output valid delay for D15 ... D0 (write data, DEMUX mode)	t_{16} CC	–	8	15	ns	
Output hold time for \overline{RD} , $\overline{WR}(L/H)$	t_{20} CC	-2	6	8	ns	
Output hold time for \overline{BHE} , ALE	t_{21} CC	-2	6	10	ns	
Address output hold time for AD15 ... AD0	t_{23} CC	-3	6	8	ns	
Output hold time for \overline{CS}	t_{24} CC	-3	6	11	ns	
Data output hold time for D15 ... D0 and AD15 ... AD0	t_{25} CC	-3	6	8	ns	
Input setup time for READY, D15 ... D0, AD15 ... AD0	t_{30} SR	25	15	–	ns	
Input hold time READY, D15 ... D0, AD15 ... AD0 ¹⁾	t_{31} SR	0	-7	–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.

Table 36 DAP Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} SR	25 ¹⁾	—	—	ns	
DAP0 high time	t_{12} SR	8	—	—	ns	
DAP0 low time	t_{13} SR	8	—	—	ns	
DAP0 clock rise time	t_{14} SR	—	—	4	ns	
DAP0 clock fall time	t_{15} SR	—	—	4	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6	—	—	ns	pad_type= standard
DAP1 hold after DAP0 rising edge	t_{17} SR	6	—	—	ns	pad_type= standard
DAP1 valid per DAP0 clock period ²⁾	t_{19} CC	12	17	—	ns	pad_type= standard

1) The debug interface cannot operate faster than the overall system, therefore $t_{11} \geq t_{SYS}$.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

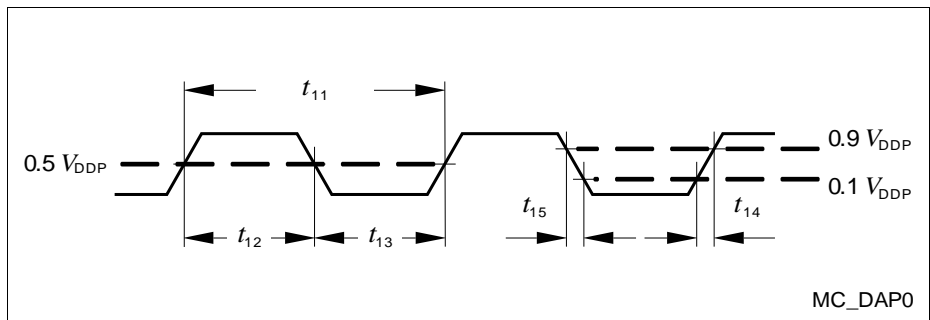


Figure 27 Test Clock Timing (DAP0)