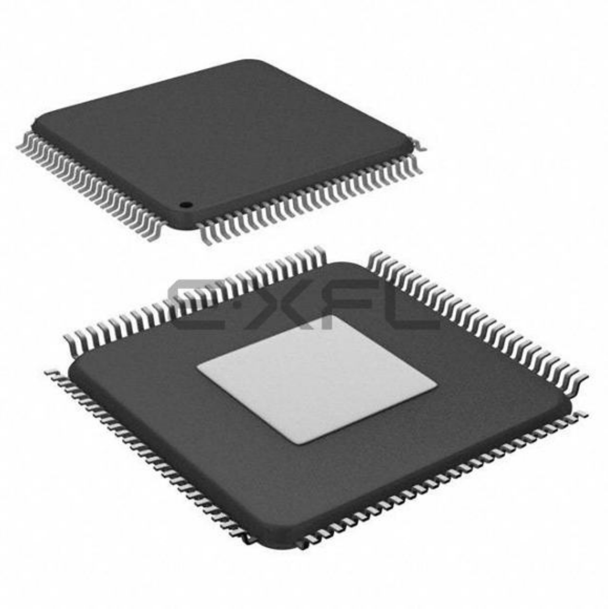

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe164gm72f80laakxuma1

1.1 Basic Device Types

Basic device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 1 Synopsis of XE164xM Basic Device Types

Derivative[1]	Flash Memory[2]	PSRAM DSRAM[3]	Capt./Comp. Modules	ADC[4] Chan.	Interfaces[4]
XE164FM-72FxxL	576 Kbytes	32 Kbytes 16 Kbytes	CC2 CCU60/1/2	11 + 5	4 CAN Nodes, 6 Serial Chan.
XE164FM-48FxxL	384 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1/2	11 + 5	4 CAN Nodes, 6 Serial Chan.
XE164FM-24FxxL	192 Kbytes	8 Kbytes 16 Kbytes	CC2 CCU60/1/2	11 + 5	4 CAN Nodes, 6 Serial Chan.
XE164GM-72FxxL	576 Kbytes	32 Kbytes 16 Kbytes	CC2 CCU60/1	6 + 5	2 CAN Nodes, 4 Serial Chan.
XE164GM-48FxxL	384 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1	6 + 5	2 CAN Nodes, 4 Serial Chan.
XE164GM-24FxxL	192 Kbytes	8 Kbytes 16 Kbytes	CC2 CCU60/1	6 + 5	2 CAN Nodes, 4 Serial Chan.
XE164HM-72FxxL	576 Kbytes	32 Kbytes 16 Kbytes	CC2 CCU60/1/2	11 + 5	No CAN Nodes, 6 Serial Chan.
XE164HM-48FxxL	384 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1/2	11 + 5	No CAN Nodes, 6 Serial Chan.
XE164HM-24FxxL	192 Kbytes	8 Kbytes 16 Kbytes	CC2 CCU60/1/2	11 + 5	No CAN Nodes, 6 Serial Chan.
XE164KM-72FxxL	576 Kbytes	32 Kbytes 16 Kbytes	CC2 CCU60/1	6 + 5	No CAN Nodes, 6 Serial Chan.
XE164KM-48FxxL	384 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1	6 + 5	No CAN Nodes, 6 Serial Chan.
XE164KM-24FxxL	192 Kbytes	8 Kbytes 16 Kbytes	CC2 CCU60/1	6 + 5	No CAN Nodes, 6 Serial Chan.

1) xx is a placeholder for the available speed grade (in MHz).

2) Specific information about the on-chip Flash memory in **Table 2**.

3) All derivatives additionally provide 8 Kbytes SBRAM and 2 Kbytes DPRAM.

4) Specific information about the available channels in **Table 4**.
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
6	P7.0	O0 / I	St/B	**Bit 0 of Port 7, General Purpose Input/Output**
	T3OUT	O1	St/B	**GPT12E Timer T3 Toggle Latch Output**
	T6OUT	O2	St/B	**GPT12E Timer T6 Toggle Latch Output**
	TDO_A	OH / IH	St/B	**JTAG Test Data Output / DAP1 Input/Output** If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	ESR2_1	I	St/B	**ESR2 Trigger Input 1**
7	P7.3	O0 / I	St/B	**Bit 3 of Port 7, General Purpose Input/Output**
	EMUX1	O1	St/B	**External Analog MUX Control Output 1 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_DOUT	O3	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU62_CCPOS1A	I	St/B	**CCU62 Position Input 1**
	TMS_C	IH	St/B	**JTAG Test Mode Selection Input** If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	U0C1_DX0F	I	St/B	**USIC0 Channel 1 Shift Data Input**
8	P7.1	O0 / I	St/B	**Bit 1 of Port 7, General Purpose Input/Output**
	EXTCLK	O1	St/B	**Programmable Clock Signal Output**
	CCU62_CTRAPA	I	St/B	**CCU62 Emergency Trap Input**
	$\overline{\text{BRKIN\_C}}$	I	St/B	**OCDS Break Signal Input**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
13	P6.2	O0 / I	DA/A	**Bit 2 of Port 6, General Purpose Input/Output**
	EMUX2	O1	DA/A	**External Analog MUX Control Output 2 (ADC0)**
	T6OUT	O2	DA/A	**GPT12E Timer T6 Toggle Latch Output**
	U1C1_SCLKOUT	O3	DA/A	**USIC1 Channel 1 Shift Clock Output**
	U1C1_DX1C	I	DA/A	**USIC1 Channel 1 Shift Clock Input**
15	P15.0	I	In/A	**Bit 0 of Port 15, General Purpose Input**
	ADC1_CH0	I	In/A	**Analog Input Channel 0 for ADC1**
16	P15.2	I	In/A	**Bit 2 of Port 15, General Purpose Input**
	ADC1_CH2	I	In/A	**Analog Input Channel 2 for ADC1**
	T5INA	I	In/A	**GPT12E Timer T5 Count/Gate Input**
17	P15.4	I	In/A	**Bit 4 of Port 15, General Purpose Input**
	ADC1_CH4	I	In/A	**Analog Input Channel 4 for ADC1**
	T6INA	I	In/A	**GPT12E Timer T6 Count/Gate Input**
18	P15.5	I	In/A	**Bit 5 of Port 15, General Purpose Input**
	ADC1_CH5	I	In/A	**Analog Input Channel 5 for ADC1**
	T6EUDA	I	In/A	**GPT12E Timer T6 External Up/Down Control Input**
19	P15.6	I	In/A	**Bit 6 of Port 15, General Purpose Input**
	ADC1_CH6	I	In/A	**Analog Input Channel 6 for ADC1**
20	V_{AREF}	-	PS/A	**Reference Voltage for A/D Converters ADC0/1**
21	V_{AGND}	-	PS/A	**Reference Ground for A/D Converters ADC0/1**
22	P5.0	I	In/A	**Bit 0 of Port 5, General Purpose Input**
	ADC0_CH0	I	In/A	**Analog Input Channel 0 for ADC0**
23	P5.2	I	In/A	**Bit 2 of Port 5, General Purpose Input**
	ADC0_CH2	I	In/A	**Analog Input Channel 2 for ADC0**
	TDI_A	I	In/A	**JTAG Test Data Input**

Table 5 **Pin Definitions and Functions** (cont'd)

Pin	Symbol	Ctrl.	Type	Function
79	P10.8	O0 / I	St/B	**Bit 8 of Port 10, General Purpose Input/Output**
	U0C0_MCLKOUT	O1	St/B	**USIC0 Channel 0 Master Clock Output**
	U0C1_SELO0	O2	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	U2C1_DOUT	O3	St/B	**USIC2 Channel 1 Shift Data Output**
	AD8	OH / IH	St/B	**External Bus Interface Address/Data Line 8**
	CCU60_CCPOS1A	I	St/B	**CCU60 Position Input 1**
	U0C0_DX1C	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	$\overline{\text{BRKIN\_B}}$	I	St/B	**OCDS Break Signal Input**
	T3EUDB	I	St/B	**GPT12E Timer T3 External Up/Down Control Input**
80	P10.9	O0 / I	St/B	**Bit 9 of Port 10, General Purpose Input/Output**
	U0C0_SELO4	O1	St/B	**USIC0 Channel 0 Select/Control 4 Output**
	U0C1_MCLKOUT	O2	St/B	**USIC0 Channel 1 Master Clock Output**
	AD9	OH / IH	St/B	**External Bus Interface Address/Data Line 9**
	CCU60_CCPOS2A	I	St/B	**CCU60 Position Input 2**
	TCK_B	IH	St/B	**DAP0/JTAG Clock Input** If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 1 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	T3INB	I	St/B	**GPT12E Timer T3 Count/Gate Input**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
81	P1.1	O0 / I	St/B	**Bit 1 of Port 1, General Purpose Input/Output**
	CCU62_COUT62	O1	St/B	**CCU62 Channel 2 Output**
	U1C0_SELO5	O2	St/B	**USIC1 Channel 0 Select/Control 5 Output**
	U2C1_DOUT	O3	St/B	**USIC2 Channel 1 Shift Data Output**
	A9	OH	St/B	**External Bus Interface Address Line 9**
	ESR2_3	I	St/B	**ESR2 Trigger Input 3**
	U2C1_DX0C	I	St/B	**USIC2 Channel 1 Shift Data Input**
82	P10.10	O0 / I	St/B	**Bit 10 of Port 10, General Purpose Input/Output**
	U0C0_SELO0	O1	St/B	**USIC0 Channel 0 Select/Control 0 Output**
	CCU60_COUT63	O2	St/B	**CCU60 Channel 3 Output**
	AD10	OH / IH	St/B	**External Bus Interface Address/Data Line 10**
	U0C0_DX2C	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX1A	I	St/B	**USIC0 Channel 1 Shift Clock Input**
	TDI_B	IH	St/B	**JTAG Test Data Input** If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
83	P10.11	O0 / I	St/B	**Bit 11 of Port 10, General Purpose Input/Output**
	U1C0_SCLKOUT	O1	St/B	**USIC1 Channel 0 Shift Clock Output**
	$\overline{\text{BRKOUT}}$	O2	St/B	**OCDS Break Signal Output**
	AD11	OH / IH	St/B	**External Bus Interface Address/Data Line 11**
	U1C0_DX1D	I	St/B	**USIC1 Channel 0 Shift Clock Input**
	RxDC2B	I	St/B	**CAN Node 2 Receive Data Input**
	TMS_B	IH	St/B	**JTAG Test Mode Selection Input** If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
90	P1.4	O0 / I	St/B	**Bit 4 of Port 1, General Purpose Input/Output**
	CCU62_COUT61	O1	St/B	**CCU62 Channel 1 Output**
	U1C1_SELO4	O2	St/B	**USIC1 Channel 1 Select/Control 4 Output**
	U2C0_SELO5	O3	St/B	**USIC2 Channel 0 Select/Control 5 Output**
	A12	OH	St/B	**External Bus Interface Address Line 12**
	U2C0_DX2B	I	St/B	**USIC2 Channel 0 Shift Control Input**
91	P10.15	O0 / I	St/B	**Bit 15 of Port 10, General Purpose Input/Output**
	U1C0_SELO2	O1	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U1C0_DOUT	O3	St/B	**USIC1 Channel 0 Shift Data Output**
	ALE	OH	St/B	**External Bus Interf. Addr. Latch Enable Output**
	U0C1_DX1C	I	St/B	**USIC0 Channel 1 Shift Clock Input**
92	P1.5	O0 / I	St/B	**Bit 5 of Port 1, General Purpose Input/Output**
	CCU62_COUT60	O1	St/B	**CCU62 Channel 0 Output**
	U1C1_SELO3	O2	St/B	**USIC1 Channel 1 Select/Control 3 Output**
	$\overline{\text{BRKOUT}}$	O3	St/B	**OCDS Break Signal Output**
	A13	OH	St/B	**External Bus Interface Address Line 13**
	U2C0_DX0C	I	St/B	**USIC2 Channel 0 Shift Data Input**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
97	$\overline{\text{PORST}}$	I	In/B	**Power On Reset Input** A low level at this pin resets the XE164xM completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pull-up device will hold this pin high when nothing is driving it.
98	$\overline{\text{ESR1}}$	O0 / I	St/B	**External Service Request 1** After power-up, an internal weak pull-up device holds this pin high when nothing is driving it.
	RxDC0E	I	St/B	**CAN Node 0 Receive Data Input**
	U1C0_DX0F	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2C	I	St/B	**USIC1 Channel 0 Shift Control Input**
	U1C1_DX0C	I	St/B	**USIC1 Channel 1 Shift Data Input**
	U1C1_DX2B	I	St/B	**USIC1 Channel 1 Shift Control Input**
	U2C1_DX2C	I	St/B	**USIC2 Channel 1 Shift Control Input**
99	$\overline{\text{ESR0}}$	O0 / I	St/B	**External Service Request 0** After power-up, $\overline{\text{ESR0}}$ operates as open-drain bidirectional reset with a weak pull-up.
	U1C0_DX0E	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2B	I	St/B	**USIC1 Channel 0 Shift Control Input**
10	V_{DDIM}	-	PS/M	**Digital Core Supply Voltage for Domain M** Decouple with a ceramic capacitor, see Data Sheet for details.
38, 64, 88	V_{DDI1}	-	PS/1	**Digital Core Supply Voltage for Domain 1** Decouple with a ceramic capacitor, see Data Sheet for details. All V_{DDI1} pins must be connected to each other.
14	V_{DDPA}	-	PS/A	**Digital Pad Supply Voltage for Domain A** Connect decoupling capacitors to adjacent $V_{\text{DDP}}/V_{\text{SS}}$ pin pairs as close as possible to the pins. *Note: The A/D_Converters and ports P5, P6 and P15 are fed from supply voltage* V_{DDPA}.

2.2 Identification Registers

The identification registers describe the current version of the XE164xM and of its modules.

Table 6 XE164xM Identification Registers

Short Name	Value	Address	Notes
SCU_IDMANUF	1820_H	$00'F07E_H$	
SCU_IDCHIP	3801_H	$00'F07C_H$	
SCU_IDMEM	$30D0_H$	$00'F07A_H$	
SCU_IDPROG	1313_H	$00'F078_H$	
JTAG_ID	$0017'E083_H$	---	marking EES-AA, ES-AA or AA

3.4 Memory Protection Unit (MPU)

The XE164xM's Memory Protection Unit (MPU) protects user-specified memory areas from unauthorized read, write, or instruction fetch accesses. The MPU can protect the whole address space including the peripheral area. This completes establisched mechanisms such as the register security mechanism or stack overrun/underrun detection.

Four Protection Levels support flexible system programming where operating system, low level drivers, and applications run on separate levels. Each protection level permits different access restrictions for instructions and/or data.

Every access is checked (if the MPU is enabled) and an access violating the permission rules will be marked as invalid and leads to a protection trap.

A set of protection registers for each protection level specifies the address ranges and the access permissions. Applications requiring more than 4 protection levels can dynamically re-program the protection registers.

3.5 Memory Checker Module (MCHK)

The XE164xM's Memory Checker Module calculates a checksum (fractional polynomial division) on a block of data, often called Cyclic Redundancy Code (CRC). It is based on a 32-bit linear feedback shift register and may, therefore, also be used to generate pseudo-random numbers.

The Memory Checker Module is a 16-bit parallel input signature compression circuitry which enables error detection within a block of data stored in memory, registers, or communicated e.g. via serial communication lines. It reduces the probability of error masking due to repeated error patterns by calculating the signature of blocks of data.

The polynomial used for operation is configurable, so most of the commonly used polynomials may be used. Also, the block size for generating a CRC result is configurable via a local counter. An interrupt may be generated if testing the current data block reveals an error.

An autonomous CRC compare circuitry is included to enable redundant error detection, e.g. to enable higher safety integrity levels.

The Memory Checker Module provides enhanced fault detection (beyond parity or ECC) for data and instructions in volatile and non volatile memories. This is especially important for the safety and reliability of embedded systems.

3.10 General Purpose Timer (GPT12E) Unit

The GPT12E unit is a very flexible multifunctional timer/counter structure which can be used for many different timing tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers organized in two separate modules, GPT1 and GPT2. Each timer in each module may either operate independently in a number of different modes or be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation: Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock and divided by a programmable prescaler. Counter Mode allows timer clocking in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes each timer has one associated port pin (TxIN) which serves as a gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The counting direction (up/down) for each timer can be programmed by software or altered dynamically by an external signal on a port pin (TxEUD), e.g. to facilitate position tracking.

In Incremental Interface Mode the GPT1 timers can be directly connected to the incremental position sensor signals A and B through their respective inputs TxIN and TxEUD. Direction and counting signals are internally derived from these two input signals, so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to the basic operating modes, T2 and T4 may be configured as reload or capture register for timer T3. A timer used as capture or reload register is stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at the associated input pin (TxIN). Timer T3 is reloaded with the contents of T2 or T4, triggered either by an external signal or a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be continuously generated without software intervention.

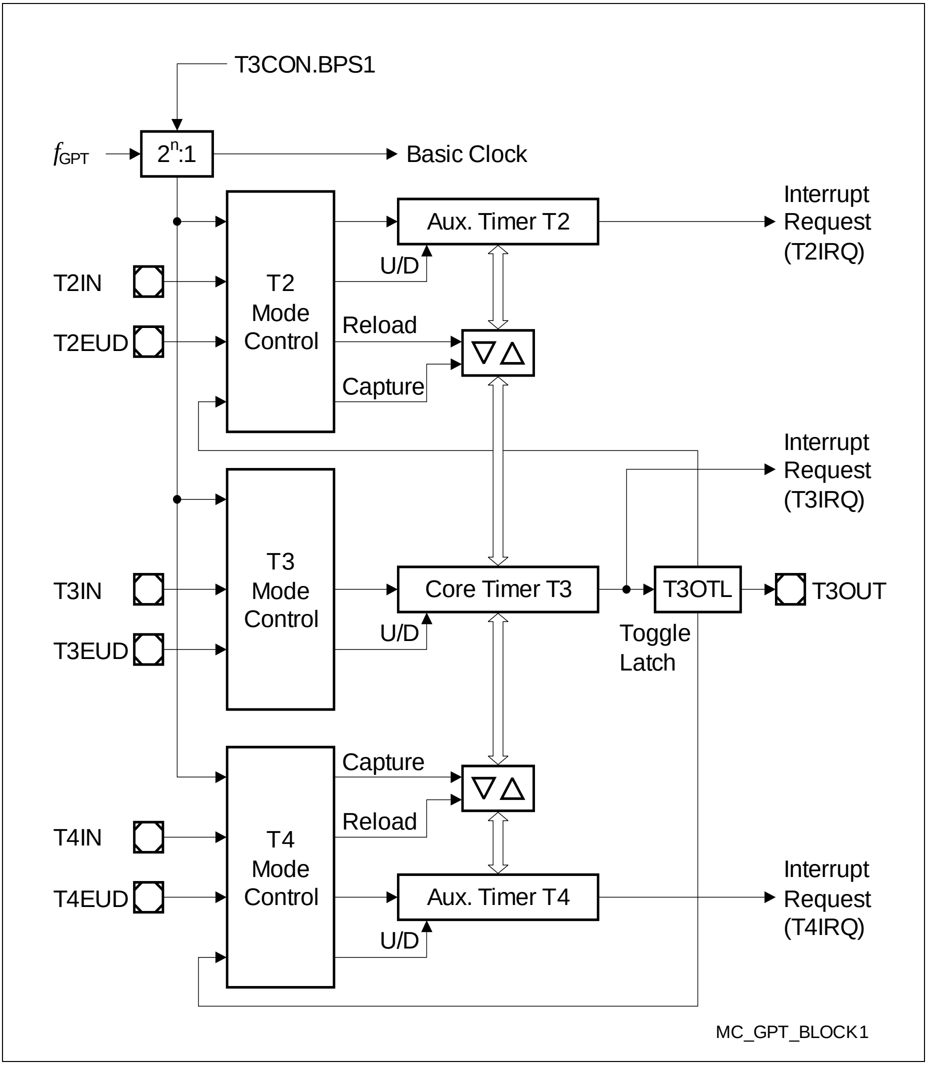

Figure 8 **Block Diagram of GPT1**

4.2.2 DC Parameters for Lower Voltage Area

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Note: Operating Conditions apply.

Table 14 is valid under the following conditions:
$V_{DDP} \geq 3.0$ V; $V_{DDPtyp} = 3.3$ V; $V_{DDP} \leq 4.5$ V

Table 14 DC Characteristics for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs). To be doubled for double bond pins.[1]	C_{IO} CC	–	–	10	pF	not subject to production test
Input Hysteresis[2]	HYS CC	0.07 x V_{DDP}	–	–	V	R_S = 0 Ohm
Absolute input leakage current on pins of analog ports[3]	$\lvert I_{OZ1} \rvert$ CC	–	10	200	nA	$V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Absolute input leakage current for all other pins. To be doubled for double bond pins.[3][1][4]	$\lvert I_{OZ2} \rvert$ CC	–	0.2	2.5	µA	$T_J \leq 110$ °C; $V_{IN} < V_{DDP}$; $V_{IN} > V_{SS}$
		–	0.2	8	µA	$T_J \leq 150$ °C; $V_{IN} < V_{DDP}$; $V_{IN} > V_{SS}$
Pull Level Force Current[5]	$\lvert I_{PLF} \rvert$ SR	150	–	–		[6]
Pull Level Keep Current[7]	$\lvert I_{PLK} \rvert$ SR	–	–	10	µA	[6]
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3	–	0.3 x V_{DDP}	V	
Output High voltage[8]	V_{OH} CC	V_{DDP} - 1.0	–	–	V	$I_{OH} \geq I_{OHmax}$
		V_{DDP} - 0.4	–	–	V	$I_{OH} \geq I_{OHnom}$[9]

Table 17 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Broken wire detection delay against VAGND[2]	t_{BWG} CC	–	–	50	[3]	
Broken wire detection delay against VAREF[2]	t_{BWR} CC	–	–	50	[4]	
Conversion time for 8-bit result[2]	t_{c8} CC	(11 + STC) x t_{ADCI} + 2 x t_{SYS}				
Conversion time for 10-bit result[2]	t_{c10} CC	(13 + STC) x t_{ADCI} + 2 x t_{SYS}				
Total Unadjusted Error	|TUE| CC	–	1	2	LSB	[5]
Wakeup time from analog powerdown, fast mode[2]	t_{WAF} CC	–	–	4	µs	
Wakeup time from analog powerdown, slow mode[2]	t_{WAS} CC	–	–	15	µs	
Analog reference ground	V_{AGND} SR	V_{SS} - 0.05	–	1.5	V	
Analog input voltage range	V_{AIN} SR	V_{AGND}	–	V_{AREF}	V	[6]
Analog reference voltage	V_{AREF} SR	V_{AGND} + 1.0	–	V_{DDPA} + 0.05	V	[5]

---

1) These parameter values cover the complete operating range. Under relaxed operating conditions (room temperature, nominal supply voltage) the typical values can be used for calculation.

2) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result. Values for the basic clock t_{ADCI} depend on programming.

3) The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 500 µs. Result below 10% (66_H).

4) The broken wire detection delay against V_{AREF} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 10 µs. This function is influenced by leakage current, in particular at high temperature. Result above 80% (332_H).

5) TUE is tested at $V_{AREF} = V_{DDPA} = 5.0$ V, $V_{AGND} = 0$ V. It is verified by design for all other voltages within the defined voltage range. The specified TUE is valid only if the absolute sum of input overload currents on analog port pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the measurement time.

6) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

3) f_{WU} in MHz

4) This value includes a hysteresis of approximately 50 mV for rising voltage.

5) V_{LV} = selected SWD voltage level

6) The limit V_{LV} - 0.10 V is valid for the OK1 level. The limit for the OK2 level is V_{LV} - 0.15 V.

Conditions for t_{SPO} Timing Measurement

The time required for the transition from **Power-On** to **Base** mode is called t_{SPO}. It is measured under the following conditions:

Precondition: The pad supply is valid, i.e. V_{DDPB} is above 3.0 V and remains above 3.0 V even though the XE164xM is starting up. No debugger is attached.

Start condition: Power-on reset is removed ($\overline{\text{PORST}}$ = 1).

End condition: External pin toggle caused by first user instruction executed from FLASH after startup.

Conditions for t_{SSO} Timing Measurement

The time required for the transition from **Stopover** to **Stopover Waked-Up** mode is called t_{SSO}. It is measured under the following conditions:

Precondition: The **Stopover** mode has been entered using the procedure defined in the Programmer’s Guide.

Start condition: Pin toggle on $\overline{\text{ESR}}$ pin triggering the startup sequence.

End condition: External pin toggle caused by first user instruction executed from PSRAM after startup.

Coding of bit fields LEVxV in SWD and PVC Configuration Registers

Table 20 Coding of bit fields LEVxV in Register SWDCON0

Code	Default Voltage Level	Notes[1]
0000_B	2.9 V	
0001_B	3.0 V	LEV1V: reset request
0010_B	3.1 V	
0011_B	3.2 V	
0100_B	3.3 V	
0101_B	3.4 V	
0110_B	3.6 V	
0111_B	4.0 V	
1000_B	4.2 V	

4.6.2 Definition of Internal Timing

The internal operation of the XE164xM is controlled by the internal system clock f_{SYS}.

Because the system clock signal f_{SYS} can be generated from a number of internal and external sources using different mechanisms, the duration of the system clock periods (TCSs) and their variation (as well as the derived external timing) depend on the mechanism used to generate f_{SYS}. This must be considered when calculating the timing for the XE164xM.

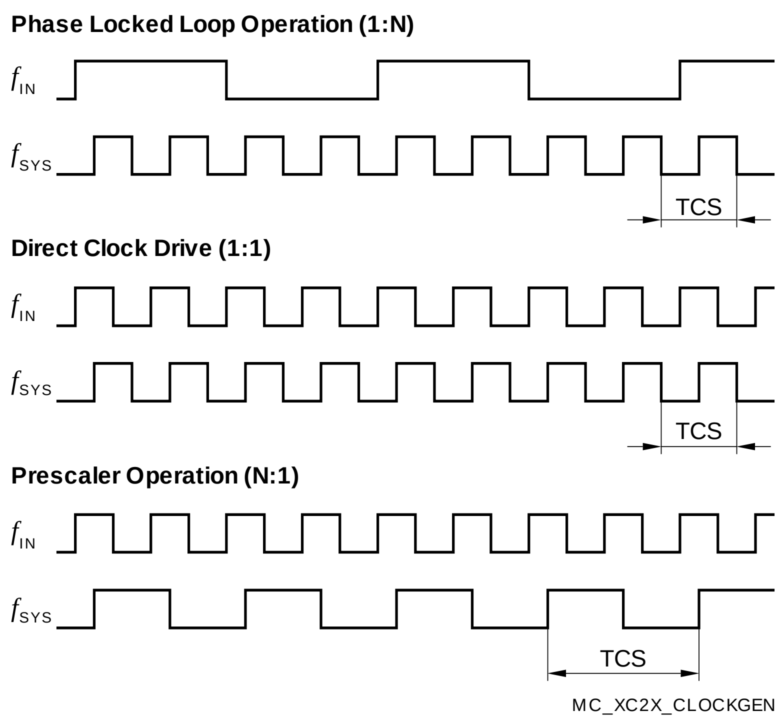

Figure 19 Generation Mechanisms for the System Clock

Note: The example of PLL operation shown in ***Figure 19*** *uses a PLL factor of 1:4; the example of prescaler operation uses a divider factor of 2:1.*

The specification of the external timing (AC Characteristics) depends on the period of the system clock (TCS).

The timing in the AC Characteristics refers to TCSs. Timing must be calculated using the minimum TCS possible under the given circumstances.
The actual minimum value for TCS depends on the jitter of the PLL. Because the PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or oscillator), the accumulated jitter is limited. This means that the relative deviation for periods of more than one TCS is lower than for a single TCS (see formulas and **Figure 20**).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler K2 to generate the system clock signal f_{SYS}. The number of VCO cycles is K2 × **T**, where **T** is the number of consecutive f_{SYS} cycles (TCS).

The maximum accumulated jitter (long-term jitter) D_{Tmax} is defined by:

$\mathbf{D_{Tmax}}$ **[ns] =** $\pm(220 / (K2 \times f_{SYS}) + 4.3)$

This maximum value is applicable, if either the number of clock cycles $T > (f_{SYS} / 1.2)$ or the prescaler value $K2 > 17$.

In all other cases for a timeframe of **T** × TCS the accumulated jitter D_T is determined by:

$\mathbf{D_T}$ **[ns] =** $D_{Tmax} \times [(1 - 0.058 \times K2) \times (T - 1) / (0.83 \times f_{SYS} - 1) + 0.058 \times K2]$

f_{SYS} in [MHz] in all formulas.

Example, for a period of 3 TCSs @ 33 MHz and K2 = 4:

$D_{max} = \pm(220 / (4 \times 33) + 4.3) = 5.97$ ns (Not applicable directly in this case!)

$D_3 = 5.97 \times [(1 - 0.058 \times 4) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 4]$
$= 5.97 \times [0.768 \times 2 / 26.39 + 0.232]$
$= 1.7$ ns

Example, for a period of 3 TCSs @ 33 MHz and K2 = 2:

$D_{max} = \pm(220 / (2 \times 33) + 4.3) = 7.63$ ns (Not applicable directly in this case!)

$D_3 = 7.63 \times [(1 - 0.058 \times 2) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 2]$
$= 7.63 \times [0.884 \times 2 / 26.39 + 0.116]$
$= 1.4$ ns

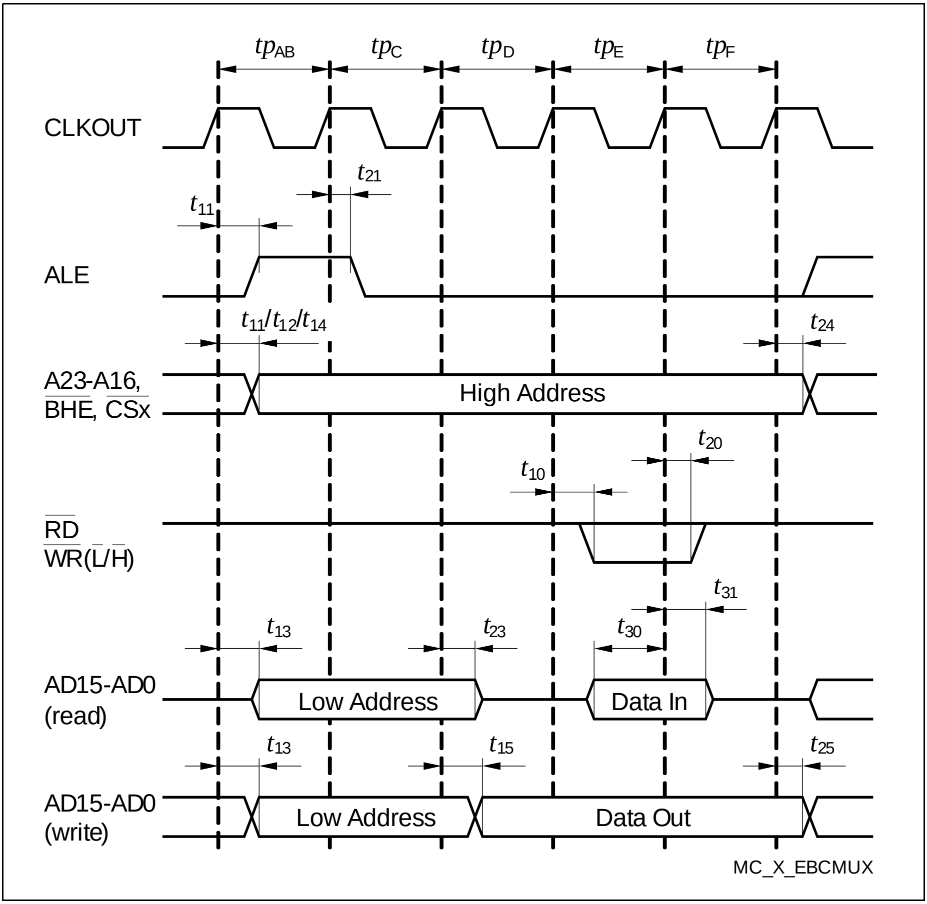

Figure 23 Multiplexed Bus Cycle

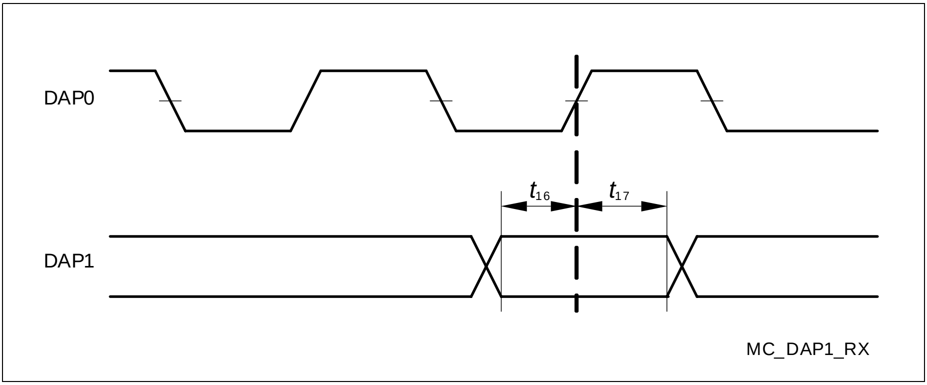

Figure 28 DAP Timing Host to Device

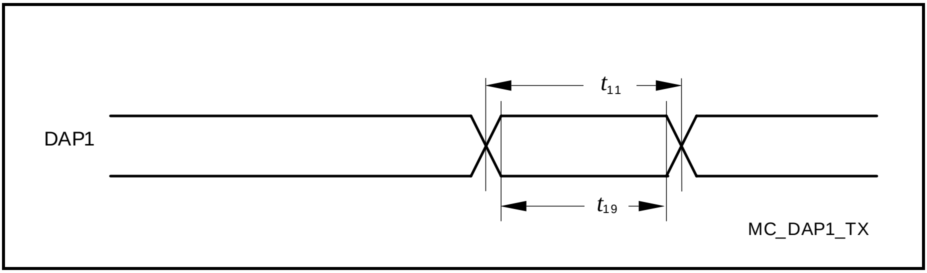

Figure 29 DAP Timing Device to Host

Note: The transmission timing is determined by the receiving debugger by evaluating the sync-request synchronization pattern telegram.

Package Outlines

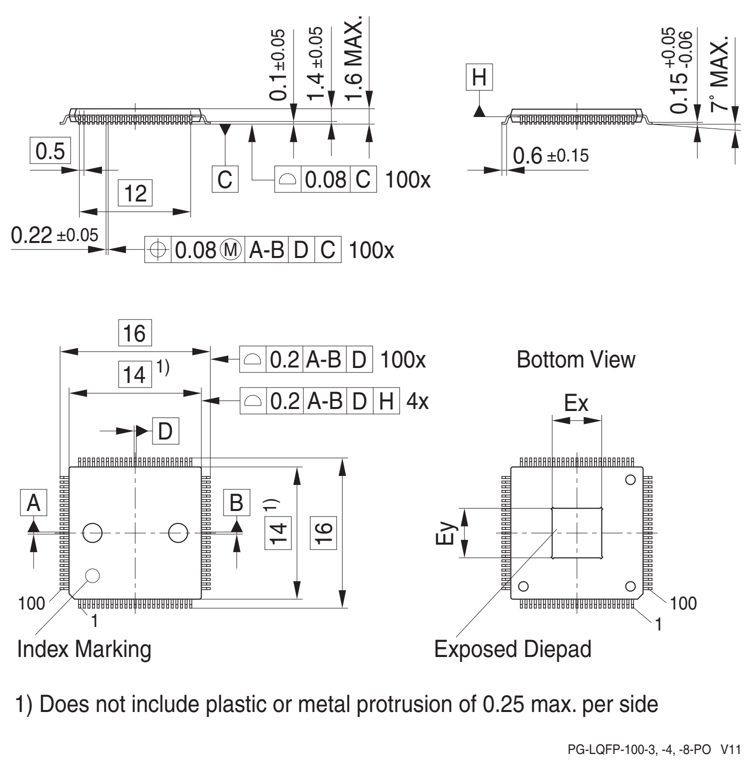

Figure 32 **PG-LQFP-100-8** (Plastic Green Thin Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages**

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