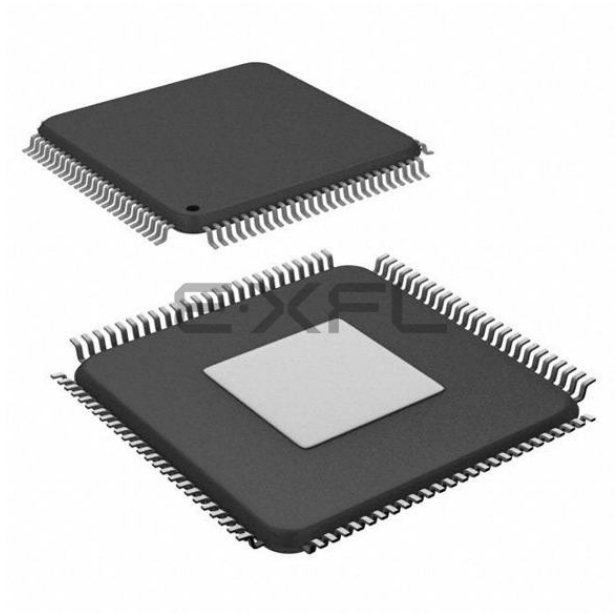
Infineon Technologies - XE164KM72F80LAAFXUMA1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe164km72f80laafxuma1

XE164xM
Revision History: V2.1, 2011-07

Previous Version(s):
V2.0, 2009-03
V1.3, 2008-11
V1.2, 2008-09
V1.1, 2008-06 Preliminary
V1.0, 2008-06 (Intermediate version)

Page	Subjects (major changes since last revisions)
39	ID registers added
86	ADC capacitances corrected (typ. vs. max.)
90	Conditions relaxed for Δf_{INT} Range for f_{WU} adapted according to PCN 2010-013-A Added startup time from power-on t_{SPO}
127	Quality declarations added

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  - Up to 3 capture/compare units for flexible PWM signal generation (CCU6x)
  - Two Synchronizable A/D Converters with a total of up to 16 channels, 10-bit resolution, conversion time below 1 µs, optional data preprocessing (data reduction, range check), broken wire detection
  - Up to 6 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
  - On-chip MultiCAN interface (Rev. 2.0B active) with up to 128 message objects (Full CAN/Basic CAN) on up to 4 CAN nodes and gateway functionality
  - On-chip system timer and on-chip real time clock
- Up to 12 Mbytes external address space for code and data
  - Programmable external bus characteristics for different address ranges
  - Multiplexed or demultiplexed external address/data buses
  - Selectable address bus width
  - 16-bit or 8-bit data bus width
  - Four programmable chip-select signals
- Single power supply from 3.0 V to 5.5 V
- Programmable watchdog timer and oscillator watchdog
- Up to 76 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via Device Access Port (DAP) or JTAG interface
- 100-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

The XE164xM types are offered with several SRAM memory sizes. **Figure 1** shows the allocation rules for PSRAM and DSRAM. Note that the rules differ:

- PSRAM allocation starts from the **lower** address
- DSRAM allocation starts from the **higher** address

For example 8 Kbytes of PSRAM will be allocated at E0’0000h-E0’1FFFh and 8 Kbytes of DSRAM will be at 00’C000h-00’DFFFh.

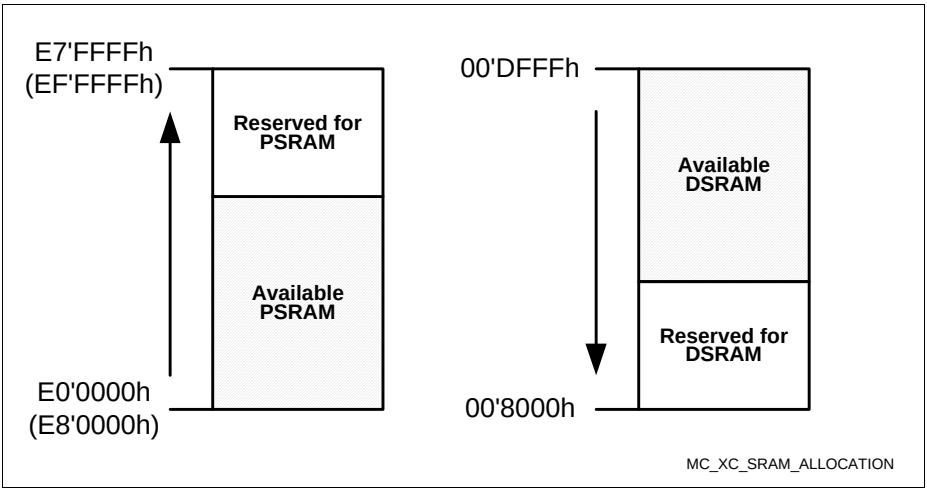

Figure 1 SRAM Allocation

2.1 Pin Configuration and Definition

The pins of the XE164xM are described in detail in **Table 5**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.

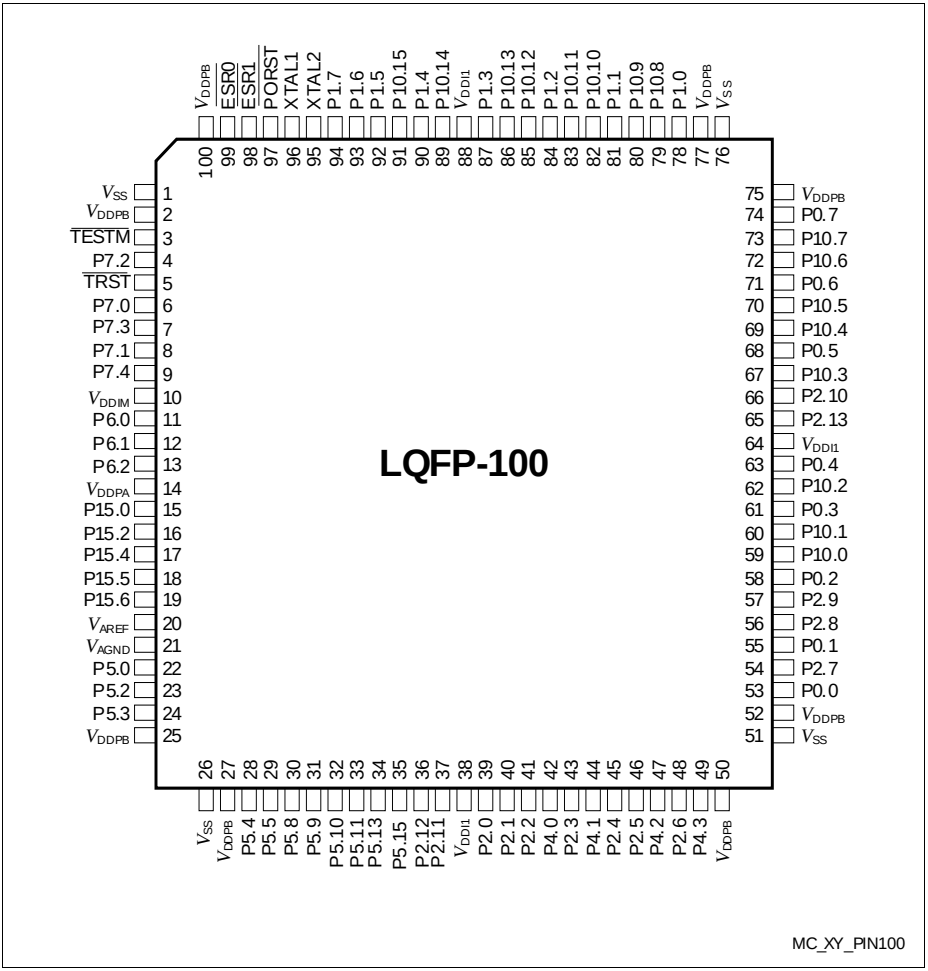

Figure 3 XE164xM Pin Configuration (top view)

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
86	P10.13	O0 / I	St/B	**Bit 13 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	TxDC3	O2	St/B	**CAN Node 3 Transmit Data Output**
	U1C0_SELO 3	O3	St/B	**USIC1 Channel 0 Select/Control 3 Output**
	$\overline{WR}$/$\overline{WRL}$	OH	St/B	**External Bus Interface Write Strobe Output** Active for each external write access, when $\overline{WR}$, active for ext. writes to the low byte, when $\overline{WRL}$.
	U1C0_DX0D	I	St/B	**USIC1 Channel 0 Shift Data Input**
87	P1.3	O0 / I	St/B	**Bit 3 of Port 1, General Purpose Input/Output**
	CCU62_COU T63	O1	St/B	**CCU62 Channel 3 Output**
	U1C0_SELO 7	O2	St/B	**USIC1 Channel 0 Select/Control 7 Output**
	U2C0_SELO 4	O3	St/B	**USIC2 Channel 0 Select/Control 4 Output**
	A11	OH	St/B	**External Bus Interface Address Line 11**
	ESR2_4	I	St/B	**ESR2 Trigger Input 4**
	CCU62_T12 HRB	I	St/B	**External Run Control Input for T12 of CCU62**
89	P10.14	O0 / I	St/B	**Bit 14 of Port 10, General Purpose Input/Output**
	U1C0_SELO 1	O1	St/B	**USIC1 Channel 0 Select/Control 1 Output**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	$\overline{RD}$	OH	St/B	**External Bus Interface Read Strobe Output**
	ESR2_2	I	St/B	**ESR2 Trigger Input 2**
	U0C1_DX0C	I	St/B	**USIC0 Channel 1 Shift Data Input**
	RxDC3C	I	St/B	**CAN Node 3 Receive Data Input**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
90	P1.4	O0 / I	St/B	**Bit 4 of Port 1, General Purpose Input/Output**
	CCU62_COUT61	O1	St/B	**CCU62 Channel 1 Output**
	U1C1_SELO4	O2	St/B	**USIC1 Channel 1 Select/Control 4 Output**
	U2C0_SELO5	O3	St/B	**USIC2 Channel 0 Select/Control 5 Output**
	A12	OH	St/B	**External Bus Interface Address Line 12**
	U2C0_DX2B	I	St/B	**USIC2 Channel 0 Shift Control Input**
91	P10.15	O0 / I	St/B	**Bit 15 of Port 10, General Purpose Input/Output**
	U1C0_SELO2	O1	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U1C0_DOUT	O3	St/B	**USIC1 Channel 0 Shift Data Output**
	ALE	OH	St/B	**External Bus Interf. Addr. Latch Enable Output**
	U0C1_DX1C	I	St/B	**USIC0 Channel 1 Shift Clock Input**
92	P1.5	O0 / I	St/B	**Bit 5 of Port 1, General Purpose Input/Output**
	CCU62_COUT60	O1	St/B	**CCU62 Channel 0 Output**
	U1C1_SELO3	O2	St/B	**USIC1 Channel 1 Select/Control 3 Output**
	$\overline{\text{BRKOUT}}$	O3	St/B	**OCDS Break Signal Output**
	A13	OH	St/B	**External Bus Interface Address Line 13**
	U2C0_DX0C	I	St/B	**USIC2 Channel 0 Shift Data Input**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
97	$\overline{\text{PORST}}$	I	In/B	**Power On Reset Input** A low level at this pin resets the XE164xM completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pull-up device will hold this pin high when nothing is driving it.
98	$\overline{\text{ESR1}}$	O0 / I	St/B	**External Service Request 1** After power-up, an internal weak pull-up device holds this pin high when nothing is driving it.
	RxDC0E	I	St/B	**CAN Node 0 Receive Data Input**
	U1C0_DX0F	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2C	I	St/B	**USIC1 Channel 0 Shift Control Input**
	U1C1_DX0C	I	St/B	**USIC1 Channel 1 Shift Data Input**
	U1C1_DX2B	I	St/B	**USIC1 Channel 1 Shift Control Input**
	U2C1_DX2C	I	St/B	**USIC2 Channel 1 Shift Control Input**
99	$\overline{\text{ESR0}}$	O0 / I	St/B	**External Service Request 0** After power-up, $\overline{\text{ESR0}}$ operates as open-drain bidirectional reset with a weak pull-up.
	U1C0_DX0E	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2B	I	St/B	**USIC1 Channel 0 Shift Control Input**
10	V_{DDIM}	-	PS/M	**Digital Core Supply Voltage for Domain M** Decouple with a ceramic capacitor, see Data Sheet for details.
38, 64, 88	V_{DDI1}	-	PS/1	**Digital Core Supply Voltage for Domain 1** Decouple with a ceramic capacitor, see Data Sheet for details. All V_{DDI1} pins must be connected to each other.
14	V_{DDPA}	-	PS/A	**Digital Pad Supply Voltage for Domain A** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The A/D_Converters and ports P5, P6 and P15 are fed from supply voltage V_{DDPA}.*

3.1 Memory Subsystem and Organization

The memory space of the XE164xM is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Table 7 XE164xM Memory Map [1)]

Address Area	Start Loc.	End Loc.	Area Size[2)]	Notes
IMB register space	$FF'FF00_H$	$FF'FFFF_H$	256 Bytes	–
Reserved (Access trap)	$F0'0000_H$	$FF'FEFF_H$	<1 Mbyte	Minus IMB registers
Reserved for EPSRAM	$E8'8000_H$	$EF'FFFF_H$	480 Kbytes	Mirrors EPSRAM
Emulated PSRAM	$E8'0000_H$	$E8'7FFF_H$	32 Kbytes	With Flash timing
Reserved for PSRAM	$E0'8000_H$	$E7'FFFF_H$	480 Kbytes	Mirrors PSRAM
Program SRAM	$E0'0000_H$	$E0'7FFF_H$	32 Kbytes	Maximum speed
Reserved for Flash	$CD'0000_H$	$DF'FFFF_H$	<1.25 Mbytes	–
Program Flash 3	$CC'0000_H$	$CC'FFFF_H$	64 Kbytes	–
Program Flash 2	$C8'0000_H$	$CB'FFFF_H$	256 Kbytes	–
Program Flash 1	$C4'0000_H$	$C7'FFFF_H$	256 Kbytes	–
Program Flash 0	$C0'0000_H$	$C3'FFFF_H$	256 Kbytes	[3)]
External memory area	$40'0000_H$	$BF'FFFF_H$	8 Mbytes	–
Available Ext. IO area[4)]	$21'0000_H$	$3F'FFFF_H$	< 2 Mbytes	Minus USIC/CAN
Reserved	$20'BC00_H$	$20'FFFF_H$	17 Kbytes	–
USIC alternate regs.	$20'B000_H$	$20'BFFF_H$	4 Kbytes	Accessed via EBC
MultiCAN alternate regs.	$20'8000_H$	$20'AFFF_H$	12 Kbytes	Accessed via EBC
Reserved	$20'6000_H$	$20'7FFF_H$	8 Kbytes	–
USIC registers	$20'4000_H$	$20'5FFF_H$	8 Kbytes	Accessed via EBC
MultiCAN registers	$20'0000_H$	$20'3FFF_H$	16 Kbytes	Accessed via EBC
External memory area	$01'0000_H$	$1F'FFFF_H$	< 2 Mbytes	Minus segment 0
SFR area	$00'FE00_H$	$00'FFFF_H$	0.5 Kbyte	–
Dual-Port RAM	$00'F600_H$	$00'FDFF_H$	2 Kbytes	–
Reserved for DPRAM	$00'F200_H$	$00'F5FF_H$	1 Kbyte	–
ESFR area	$00'F000_H$	$00'F1FF_H$	0.5 Kbyte	–
XSFR area	$00'E000_H$	$00'EFFF_H$	4 Kbytes	–

3.4 Memory Protection Unit (MPU)

The XE164xM's Memory Protection Unit (MPU) protects user-specified memory areas from unauthorized read, write, or instruction fetch accesses. The MPU can protect the whole address space including the peripheral area. This completes established mechanisms such as the register security mechanism or stack overrun/underrun detection.

Four Protection Levels support flexible system programming where operating system, low level drivers, and applications run on separate levels. Each protection level permits different access restrictions for instructions and/or data.

Every access is checked (if the MPU is enabled) and an access violating the permission rules will be marked as invalid and leads to a protection trap.

A set of protection registers for each protection level specifies the address ranges and the access permissions. Applications requiring more than 4 protection levels can dynamically re-program the protection registers.

3.5 Memory Checker Module (MCHK)

The XE164xM's Memory Checker Module calculates a checksum (fractional polynomial division) on a block of data, often called Cyclic Redundancy Code (CRC). It is based on a 32-bit linear feedback shift register and may, therefore, also be used to generate pseudo-random numbers.

The Memory Checker Module is a 16-bit parallel input signature compression circuitry which enables error detection within a block of data stored in memory, registers, or communicated e.g. via serial communication lines. It reduces the probability of error masking due to repeated error patterns by calculating the signature of blocks of data.

The polynomial used for operation is configurable, so most of the commonly used polynomials may be used. Also, the block size for generating a CRC result is configurable via a local counter. An interrupt may be generated if testing the current data block reveals an error.

An autonomous CRC compare circuitry is included to enable redundant error detection, e.g. to enable higher safety integrity levels.

The Memory Checker Module provides enhanced fault detection (beyond parity or ECC) for data and instructions in volatile and non volatile memories. This is especially important for the safety and reliability of embedded systems.

3.6 Interrupt System

The architecture of the XE164xM supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Where in a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XE164xM has eight PEC channels, each whith fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of 7/11[1)] CPU clocks, the XE164xM can react quickly to the occurrence of non-deterministic events.

Interrupt Nodes and Source Selection

The interrupt system provides 96 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

Trap Processing

The XE164xM provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called ‘Hardware Traps’. A hardware trap causes an immediate system reaction similar to a standard interrupt service (branching

1) Depending if the jump cache is used or not.

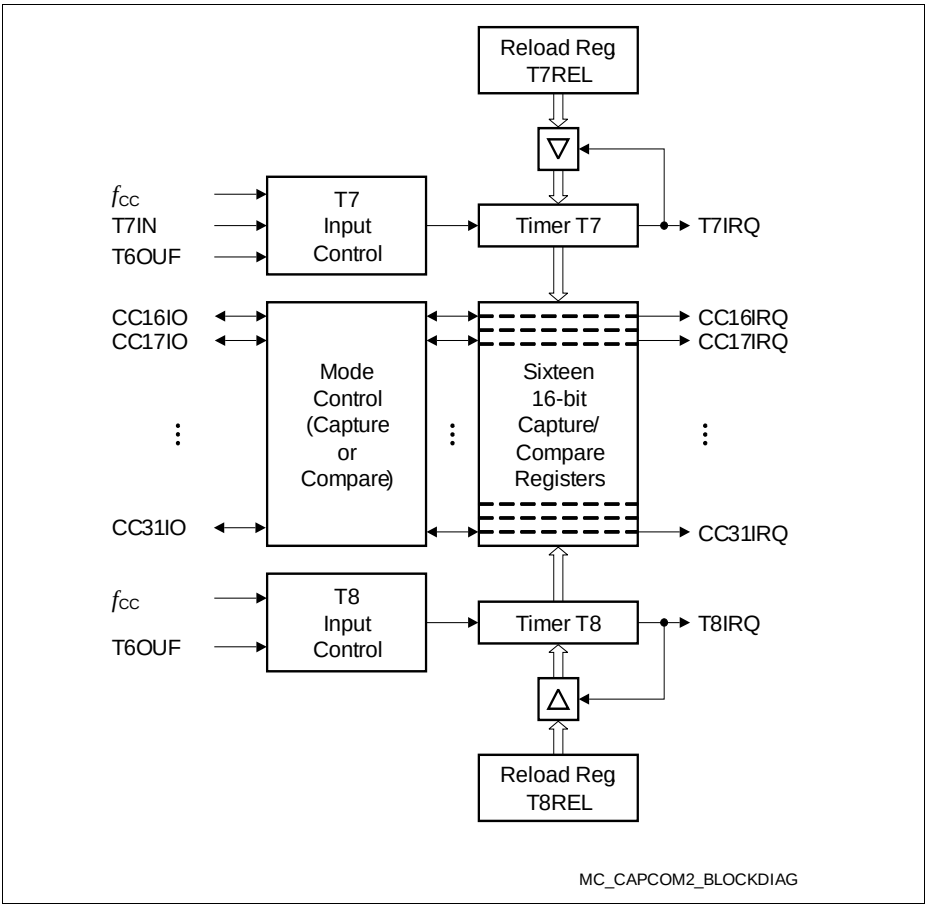

Figure 6 CAPCOM2 Unit Block Diagram

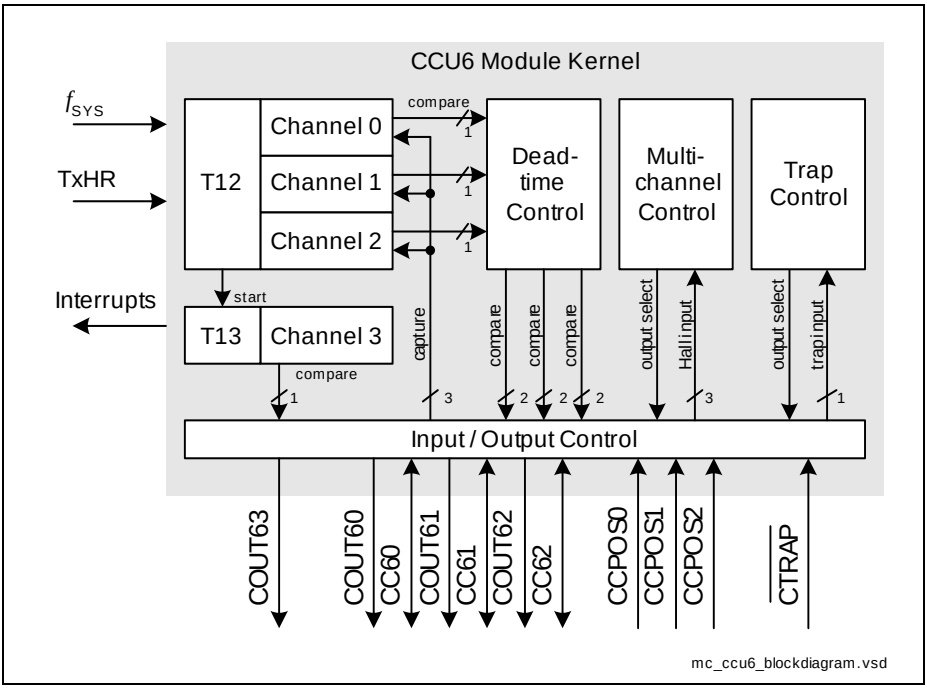

Figure 7 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

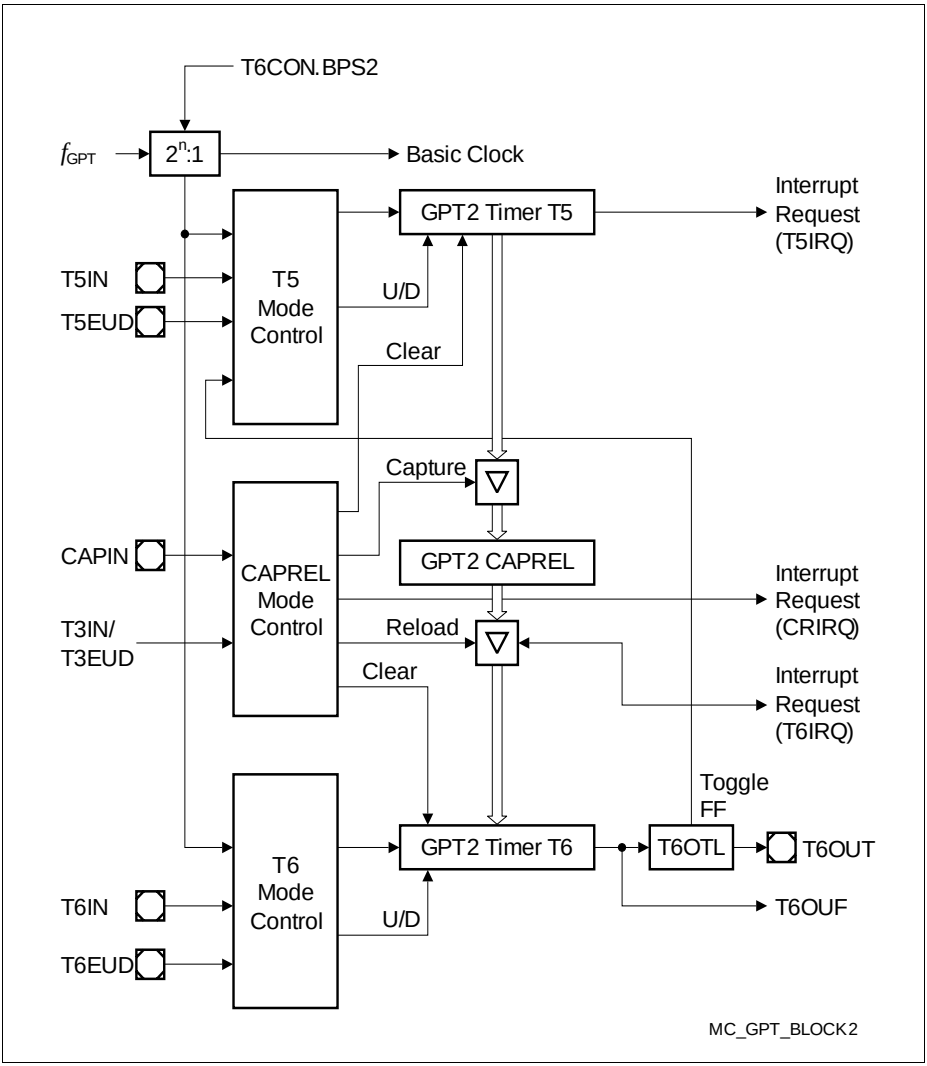

Figure 9 Block Diagram of GPT2

Pullup/Pulldown Device Behavior

Most pins of the XE164xM feature pullup or pulldown devices. For some special pins these are fixed; for the port pins they can be selected by the application.

The specified current values indicate how to load the respective pin depending on the intended signal level. **Figure 13** shows the current paths.

The shaded resistors shown in the figure may be required to compensate system pull currents that do not match the given limit values.

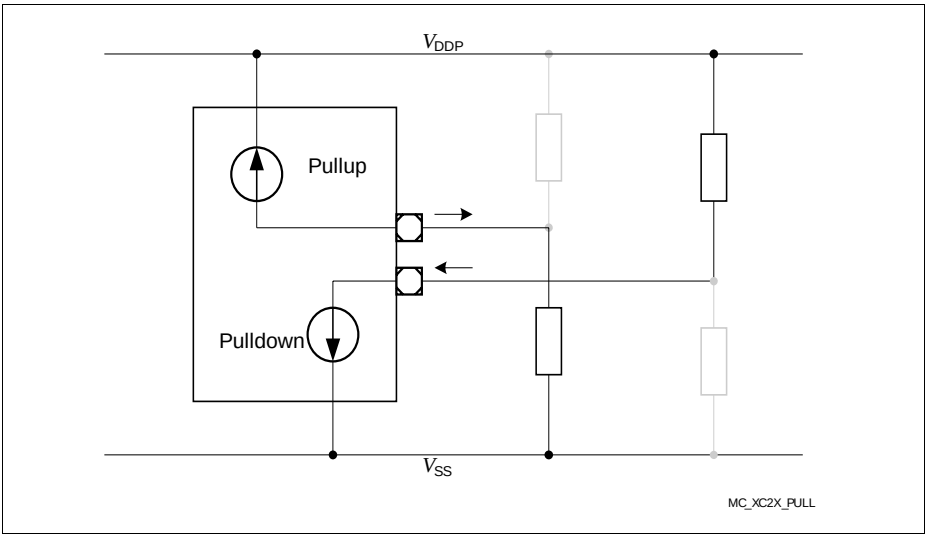

Figure 13 Pullup/Pulldown Current Definition

2) The pad supply voltage pins (V_{DDPB}) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers input stages are switched.
   In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to 3 + 0.6 x f_{SYS}.
3) Please consider the additional conditions described in section "Active Mode Power Supply Current".

Active Mode Power Supply Current

The actual power supply current in active mode not only depends on the system frequency but also on the configuration of the XE164xM's subsystem.

Besides the power consumed by the device logic the power supply pins also provide the current that flows through the pin output drivers.
A small current is consumed because the drivers' input stages are switched.

The IO power domains can be supplied separately. Power domain A (V_{DDPA}) supplies the A/D converters and Port 6. Power domain B (V_{DDPB}) supplies the on-chip EVVRs and all other ports.
During operation domain A draws a maximum current of 1.5 mA for each active A/D converter module from V_{DDPA}.

In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to (3 + 0.6×f_{SYS}) mA.

4.6.3 External Clock Input Parameters

These parameters specify the external clock generation for the XE164xM. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2
- By supplying an **external clock signal**
  - This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain)

If connected to CLKIN1, the input signal must reach the defined input levels V_{IL} and V_{IH}. If connected to XTAL1, a minimum amplitude V_{AX1} (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

Note: The given clock timing parameters (t_1 … t_4) are only valid for an external clock input signal.

Note: Operating Conditions apply.

Table 24 External Clock Input Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Oscillator frequency	f_{OSC} SR	4	–	40	MHz	Input = clock signal
		4	–	16	MHz	Input = crystal or ceramic resonator
XTAL1 input current absolute value	$\|I_{IL}\|$ CC	–	–	20	µA	
Input clock high time	t_1 SR	6	–	–	ns	
Input clock low time	t_2 SR	6	–	–	ns	
Input clock rise time	t_3 SR	–	–	8	ns	
Input clock fall time	t_4 SR	–	–	8	ns	
Input voltage amplitude on XTAL1[1)]	V_{AX1} SR	0.3 x V_{DDIM}	–	–	V	4 to 16 MHz
		0.4 x V_{DDIM}	–	–	V	16 to 25 MHz
		0.5 x V_{DDIM}	–	–	V	25 to 40 MHz
Input voltage range limits for signal on XTAL1	V_{IX1} SR	-1.7 + V_{DDIM}	–	1.7	V	[2)]

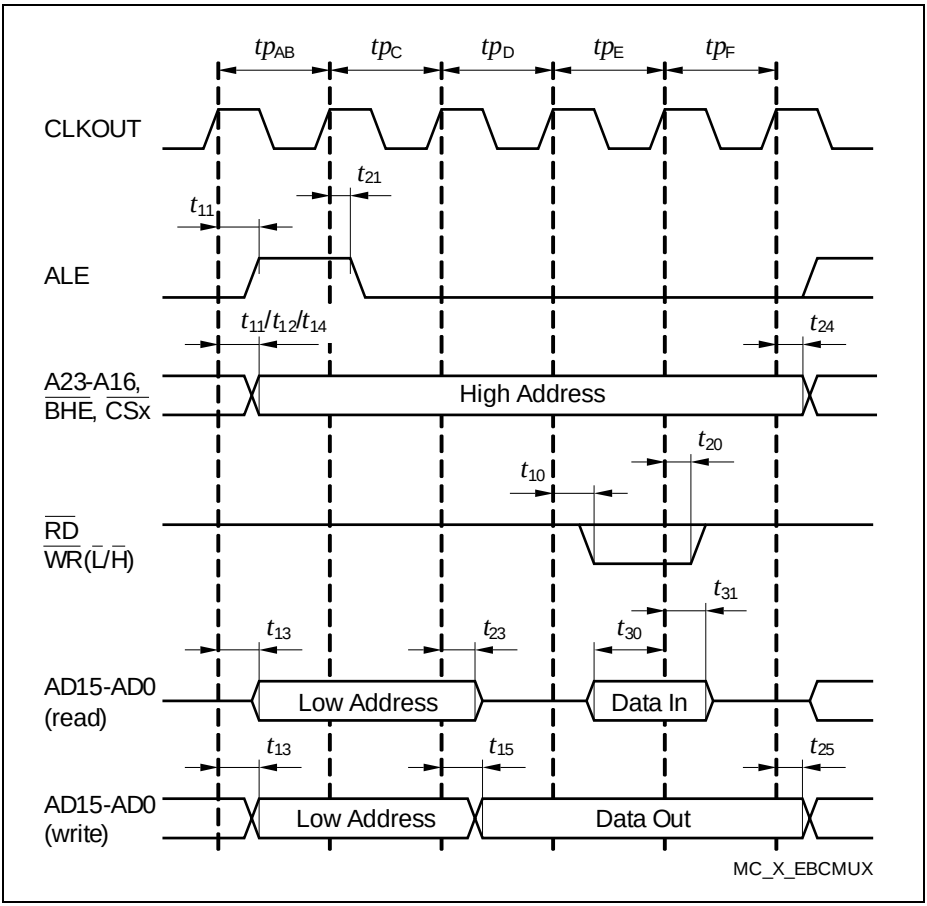

Figure 23 Multiplexed Bus Cycle

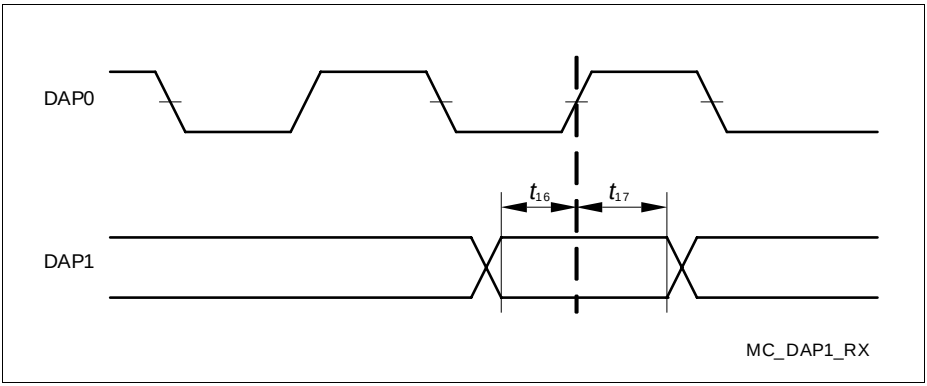

Figure 28 DAP Timing Host to Device

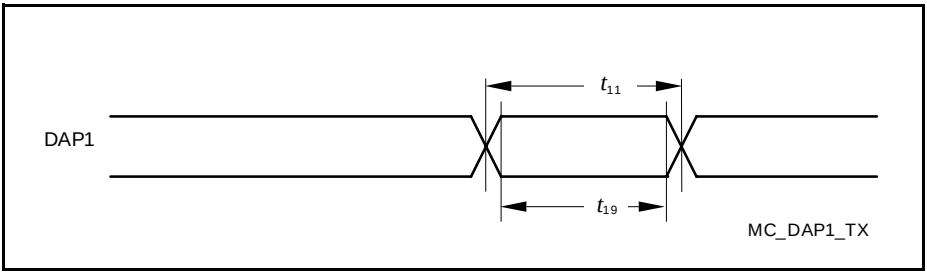

Figure 29 DAP Timing Device to Host

Note: The transmission timing is determined by the receiving debugger by evaluating the sync-request synchronization pattern telegram.

Table 38 JTAG Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50[1]	–	–	ns	[2]
TCK high time	t_2 SR	16	–	–	ns	
TCK low time	t_3 SR	16	–	–	ns	
TCK clock rise time	t_4 SR	–	–	8	ns	
TCK clock fall time	t_5 SR	–	–	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	
TDO valid from TCK falling edge (propagation delay)[3]	t_8 CC	–	32	36	ns	
TDO high impedance to valid output from TCK falling edge[4][3]	t_9 CC	–	32	36	ns	
TDO valid output to high impedance from TCK falling edge[3]	t_{10} CC	–	32	36	ns	
TDO hold after TCK falling edge[3]	t_{18} CC	5	–	–	ns	

1) The debug interface cannot operate faster than the overall system, therefore $t_1 \geq t_{SYS}$.

2) Under typical conditions, the interface can operate at transfer rates up to 20 MHz.

3) The falling edge on TCK is used to generate the TDO timing.

4) The setup time for TDO is given implicitly by the TCK cycle time.

Package Outlines

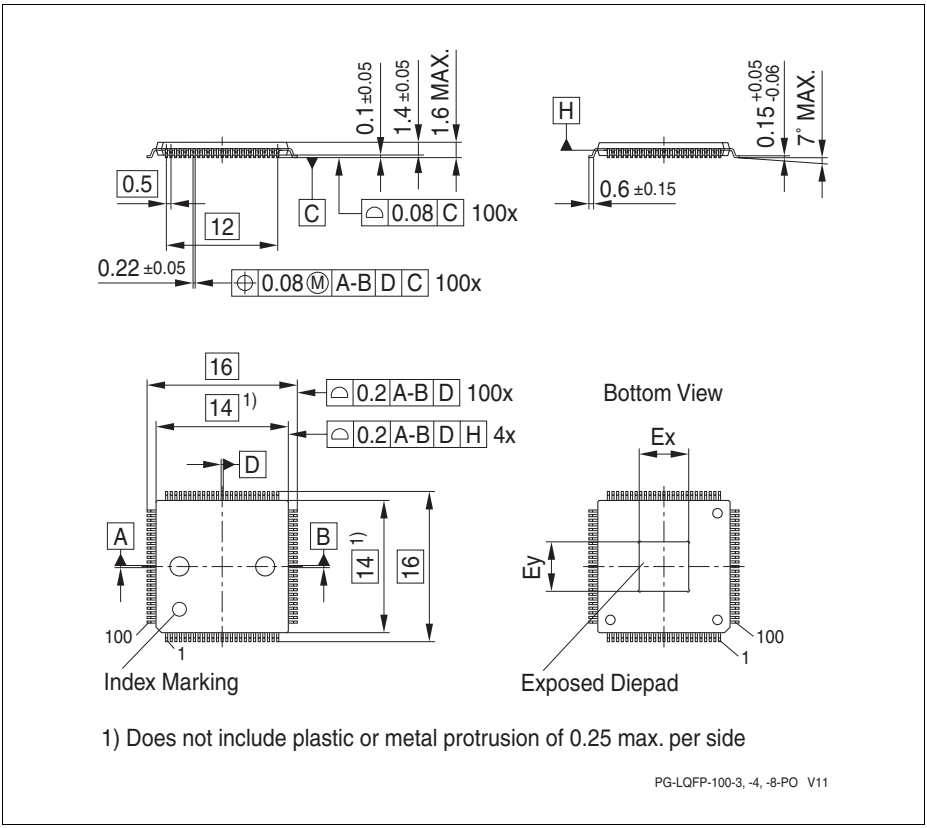

Figure 32 PG-LQFP-100-8 (Plastic Green Thin Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages**