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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V
Operating Temperature	-40°C ~ 110°C (TJ)
Security Features	-
Package / Case	483-BCBGA Exposed Pad
Supplier Device Package	483-HiTCE-CBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pcx7457vgh1000nc

  - Instruction cache can provide four instructions per clock cycle; data cache can provide four words per clock cycle
  - Caches can be disabled in software
  - Caches can be locked in software
  - MESI data cache coherency maintained in hardware
  - Separate copy of data cache tags for efficient snooping
  - Parity support on cache and tags
  - No snooping of instruction cache except for icbi instruction
  - Data cache supports AltiVec LRU and transient instructions
  - Critical double- and/or quad-word forwarding is performed as needed. Critical quad-word forwarding is used for AltiVec loads and instruction fetches. Other accesses use critical double-word forwarding
- Level 2 (L2) cache interface
  - On-chip, 512 Kbyte, eight-way set-associative unified instruction and data cache
  - Fully pipelined to provide 32 bytes per clock cycle to the L1 caches
  - A total nine-cycle load latency for an L1 data cache miss that hits in L2
  - PLRU replacement algorithm
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - 64-byte, two-sectored line size
  - Parity support on cache
- Level 3 (L3) cache interface (not implemented on PC7447)
  - Provides critical double-word forwarding to the requesting unit
  - Internal L3 cache controller and tags
  - External data SRAMs
  - Support for 1, 2, and 4M bytes (MB) total SRAM space
  - Support for 1 or 2 MB of cache space
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - 64-byte (1 MB) or 128-byte (2 MB) sectored line size
  - Private memory capability for half (1 MB minimum) or all of the L3 SRAM space for a total of 1-, 2-, or 4-MB of private memory
  - Supports MSUG2 dual data rate (DDR) synchronous Burst SRAMs, PB2 pipelined synchronous Burst SRAMs, and pipelined (register-register) Late Write synchronous Burst SRAMs
  - Supports parity on cache and tags
  - Configurable core-to-L3 frequency divisors
  - 64-bit external L3 data bus sustains 64-bit per L3 clock cycle
- Separate memory management units (MMUs) for Instructions and data
  - 52-bit virtual address; 32- or 36-bit physical address
  - Address translation for 4 Kbyte pages, variable-sized blocks, and 256M bytes segments

  - Memory programmable as write-back/write-through, caching-inhibited/caching-allowed, and memory coherency enforced/memory coherency not enforced on a page or block basis
  - Separate IBATs and DBATs (eight each) also defined as SPRs
  - Separate instruction and data translation lookaside buffers (TLBs)
    Both TLBs are 128-entry, two-way set-associative, and use LRU replacement algorithm
    TLBs are hardware- or software-reloadable (that is, on a TLB miss a page table search is performed in hardware or by system software)

- Efficient data flow
  - Although the VR/LSU interface is 128 bits, the L1/L2/L3 bus interface allows up to 256 bits
  - The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs
  - L2 cache is fully pipelined to provide 256 bits per processor clock cycle to the L1 cache
  - As many as eight outstanding, out-of-order, cache misses are allowed between the L1 data cache and L2/L3 bus
  - As many as 16 out-of-order transactions can be present on the MPX bus
  - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed)
  - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - Hardware-enforced, MESI cache coherency protocols for data cache
  - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - 1.6V processor core
  - The following three power-saving modes are available to the system:

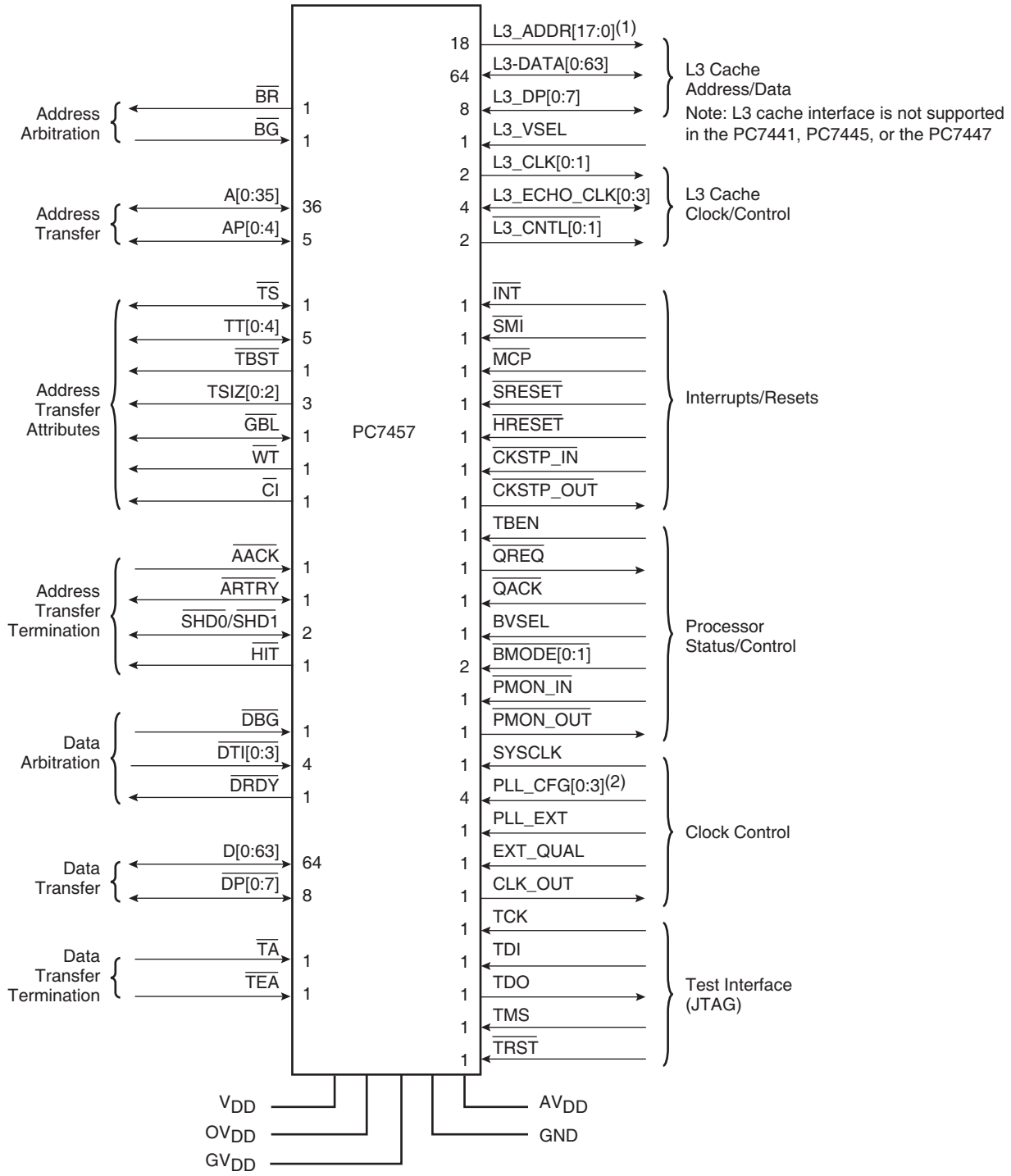
    Nap—Instruction fetching is halted. Only those clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a QREQ/QACK processor-system handshake protocol

    Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled

    Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed on exiting the deep sleep state

4. Signal Description

Figure 4-1. PC7457 Microprocessor Signal Groups



Notes: 1. For the PC7457, there are 19 L3_ADDR signals, (L3_ADDR[0:18].
2. For the PC7447 and PM7457, there are 5 PLL_CFG signals, (PLL_CFG[0:4].

5. Detailed Specification

This specification describes the specific requirements for the microprocessor PC7457 in compliance with Atmel standard screening.

6. Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics
2. MIL-PRF-38535: Appendix A: General specifications for microcircuits

The microcircuits are in accordance with the applicable documents and as specified herein.

6.1 Design and Construction

6.1.1 Terminal Connections

Depending on the package, the terminal connections are as shown in "Recommended Operating Conditions(1)" on page 12 and Figure 4-1 on page 10.

6.1.2 Absolute Maximum Ratings(1)

Symbol	Characteristic		Maximum Value	Unit
V_{DD}(2)	Core supply voltage		-0.3 to 1.60	V
AV_{DD}(2)	PLL supply voltage		-0.3 to 1.60	V
OV_{DD}(3)(4)	Processor bus supply voltage	BVSEL = 0	-0.3 to 1.95	V
OV_{DD}(3)(5)		BVSEL = $\overline{\text{HRESET}}$ or OV_{DD}	-0.3 to 2.7	V
GV_{DD}(3)(6)	L3 bus supply voltage	L3VSEL = ¬$\overline{\text{HRESET}}$	-0.3 to 1.65	V
GV_{DD}(3)(7)		L3VSEL = 0	-0.3 to 1.95	V
GV_{DD}(3)(8)		L3VSEL = $\overline{\text{HRESET}}$ or GV_{DD}	-0.3 to 2.7	V
V_{IN}(9)(10)	Input voltage	Processor bus	-0.3 to OV_{DD} + 0.3	V
V_{IN}(9)(10)		L3 bus	-0.3 to GV_{DD} + 0.3	V
V_{IN}		JTAG signals	-0.3 to OV_{DD} + 0.3	V
T_{STG}	Storage temperature range		-55 to 150	°C

Notes:
1. Functional and tested operating conditions are given in "Recommended Operating Conditions(1)" on page 12. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: V_{DD}/AV_{DD} must not exceed OV_{DD}/GV_{DD} by more than 1V during normal operation; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. Caution: OV_{DD}/GV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2V during normal operation; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. BVSEL must be set to 0, such that the bus is in 1.8V mode.
5. BVSEL must be set to $\overline{\text{HRESET}}$ or 1, such that the bus is in 2.5V mode.
6. L3VSEL must be set to ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), such that the bus is in 1.5V mode.
7. L3VSEL must be set to 0, such that the bus is in 1.8V mode.
8. L3VSEL must be set to $\overline{\text{HRESET}}$ or 1, such that the bus is in 2.5V mode.
9. Caution: V_{IN} must not exceed OV_{DD} or GV_{DD} by more than 0.3V at any time including during power-on reset.
10. V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 6-1.

7.2 Dynamic Characteristics

This section provides the AC electrical characteristics for the PC7457. After fabrication, functional parts are sorted by maximum processor core frequency as shown in section “Clock AC Specifications” and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency; See “Ordering Information” on page 59.

7.2.1 Clock AC Specifications

Table 7-2 provides the clock AC timing specifications as defined in Figure 7-1 and represents the tested operating frequencies of the devices. The maximum system bus frequency, f_{SYSCLK}, given in Table 7-2 is considered a practical maximum in a typical single-processor system. The actual maximum SYSCLK frequency for any application of the PC7457 will be a function of the AC timings of the PC7457, the AC timings for the system controller, bus loading, printed-circuit board topology, trace lengths, and so forth, and may be less than the value given in Table 7-2.

Table 7-2. Clock AC Timing Specifications (See “Recommended Operating Conditions(1)” on page 12)

		Maximum Processor Core Frequency						
		600 MHz		867 MHz		1000 MHz		
		V_{DD} = 1.1V		V_{DD} = 1.1V		V_{DD} = 1.1V		
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{CORE}(1)	Processor frequency	500	600	500	867	500	1000	MHz
f_{VCO}(1)	VCO frequency	1000	1200	1000	1733	1000	2000	MHz
f_{SYSCLK}(1)(2)	SYSCLK frequency	33	167	33	167	33	167	MHz
t_{SYSCLK}(2)	SYSCLK cycle time	6	30	6	30	6	30	ns
t_{KR}, t_{KF}(3)	SYSCLK rise and fall time	–	1	–	1	–	1	ns
t_{KHKL}/t_{SYSCLK}(4)	SYSCLK duty cycle measured at $OV_{DD}/2$	40	60	40	60	–	–	%
	SYSCLK jitter(5)(6)	–	150	–	150	–	–	ps
	Internal PLL relock time(7)	–	100	–	100	–	–	µs

		Maximum Processor Core Frequency								
		867 MHz		1000 MHz		1200 MHz		1267 MHz		
		V_{DD} = 1.3V		V_{DD} = 1.3V		V_{DD} = 1.3V		V_{DD} = 1.3V		
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{CORE}(1)	Processor frequency	600	867	600	1000	600	1200	600	1267	MHz
f_{VCO}(1)	VCO frequency	1200	1733	1200	2000	1200	2400	1200	2534	MHz
f_{SYSCLK}(1)(2)	SYSCLK frequency	33	167	33	167	33	167	33	167	MHz
t_{SYSCLK}(2)	SYSCLK cycle time	6	30	6	30	6	30	6	30	ns
t_{KR}, t_{KF}(3)	SYSCLK rise and fall time	–	1	–	1	–	1	–	1	ns

7.2.2 Processor Bus AC Specifications

Table 7-3 provides the processor bus AC timing specifications for the PC7457 as defined in Figure 7-10 on page 33 and Figure 7-2 on page 23. Timing specifications for the L3 bus are provided in section "L3 Clock AC Specifications" on page 24.

Table 7-3. Processor Bus AC Timing Specifications[1] (at Recommended Operating Conditions, see page 12.)

Symbol[2]	Parameter	All Speed Grades			Unit
		V_{DD} = 1.1V	Min V_{DD} = 1.3V	Max	
	Input setup times:				
t_{AVKH}	A[0:35], AP[0:4]	2.0	1.8	–	
t_{DVKH}	D[0:63], DP[0:7]	2.0	1.8	–	
t_{IVKH}	$\overline{AACK}$, $\overline{ARTRY}$, $\overline{BG}$, $\overline{CKSTP\_IN}$, $\overline{DBG}$, DTI[0:3], $\overline{GBL}$, TT[0:3], $\overline{QACK}$, $\overline{TA}$, TBEN, $\overline{TEA}$, $\overline{TS}$, EXT_QUAL, $\overline{PMON\_IN}$, $\overline{SHD}$[0:1],	2.0	1.8	–	ns
t_{MVKH}[8]	BMODE[0:1], $\overline{BMODE}$[0:1], BVSEL, L3VSEL	2	1.8	–	
	Input hold times:				
t_{AXKH}	A[0:35], AP[0:4]	0	0	–	
t_{DXKH}	D[0:63], DP[0:7]	0	0	–	
t_{IXKH}	$\overline{AACK}$, $\overline{ARTRY}$, $\overline{BG}$, $\overline{CKSTP\_IN}$, $\overline{DBG}$, DTI[0:3], $\overline{GBL}$, TT[0:3], $\overline{QACK}$, $\overline{TA}$, TBEN, $\overline{TEA}$, $\overline{TS}$, EXT_QUAL, $\overline{PMON\_IN}$, $\overline{SHD}$[0:1]	0	0	–	ns
t_{MXKH}[8]	BMODE[0:1], $\overline{BMODE}$[0:1], BVSEL, L3VSEL	0	0	–	
	Output valid times: A[0:35], AP[0:4]				
t_{KHAV}	D[0:63], DP[0:7]	–	–	2	ns
t_{KHDV}	$\overline{AACK}$, $\overline{ARTRY}$, $\overline{BR}$, $\overline{CI}$, $\overline{CKSTP\_IN}$, $\overline{DRDY}$, DTI[0:3],	–	–	2	
t_{KHOV}	$\overline{GBL}$, $\overline{HIT}$, $\overline{PMON\_OUT}$, $\overline{QREQ}$, $\overline{TBST}$, TSIZ[0:2], TT[0:3], $\overline{TS}$, $\overline{SHD}$[0:1], $\overline{WT}$	–	–	2	
	Output hold times: A[0:35], AP[0:4]				
t_{KHAX}	D[0:63], DP[0:7]	0.5	0.5	–	ns
t_{KHDX}	$\overline{AACK}$, $\overline{ARTRY}$, $\overline{BR}$, $\overline{CI}$, $\overline{CKSTP\_IN}$, $\overline{DRDY}$, DTI[0:3],	0.5	0.5	–	
t_{KHOX}	$\overline{GBL}$, $\overline{HIT}$, $\overline{PMON\_OUT}$, $\overline{QREQ}$, $\overline{TBST}$, TSIZ[0:2], TT[0:3], $\overline{TS}$, $\overline{SHD}$[0:1], $\overline{WT}$	0.5	0.5	–	
t_{KHOE}	SYSCLK to output enable	0.5	0.5	–	ns
t_{KHOZ}	SYSCLK to output high impedance (all except $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHD0}$, $\overline{SHD1}$)	–	–	3.5	ns
t_{KHTSPZ}[3][4][5]	SYSCLK to $\overline{TS}$ high impedance after precharge	–	–	1	t_{SYSCLK}
t_{KHARP}[3][5][6][7]	Maximum delay to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ precharge	–	–	1	t_{SYSCLK}
t_{KHARPZ}[3][5][6][7]	SYSCLK to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ high impedance after precharge	–	–	2	t_{SYSCLK}

Notes: 1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50Ω load (see Figure 7-10 on page 33). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

Note that SYSCLK input jitter and L3_CLK[0:1] output jitter are already comprehended in the L3 bus AC timing specifications and do not need to be separately accounted for in an L3 AC timing analysis.

Clock skews, where applicable, do need to be accounted for in an AC timing analysis.Freescale is similarly limited by system constraints and cannot perform tests of the L3 interface on a socketed part on a functional tester at the maximum frequencies of Table 7-4. Therefore, functional operation and AC timing information are tested at core-to-L3 divisors which result in L3 frequencies at 250 MHz or lower.

Table 7-4. L3_CLK Output AC Timing Specifications at Recommended Operating Conditions (see page 12)[6]

Symbol	Parameter	All Speed Grades						Unit
		Min	Typical	Max	Min	Typical	Max	
f_{L3_CLK}[1]	L3 clock frequency	–	200		–	250	–	MHz
t_{L3_CLK}[1]	L3 clock cycle time	–	5	–	–	4	–	ns
t_{CHCL}/t_{L3_CLK}[2]	L3 clock duty cycle	–	50	–	–	50	–	%
$t_{L3CSKW1}$[3]	L3 clock output-to-output skew (L3_CLK0 to L3_CLK1)	–	–	100	–	–	100	ps
$t_{L3CSKW2}$[4]	L3 clock output-to-output skew (L3_CLK[0:1] to L3_ECHO_CLK[1:3])	–	–	100	–	–	100	ps
	L3 clock jitter[5]	–	–	±75	–	–	±75	ps

Notes:
1. The maximum L3 clock frequency (and minimum L3 clock period) will be system dependent. See "L3 Clock AC Specifications" on page 24 for an explanation that this maximum frequency is not functionally tested at speed by Freescale. The minimum L3 clock frequency and period are f_{SYSCLK} and t_{SYSCLK}, respectively.
2. The nominal duty cycle of the L3 output clocks is 50% measured at midpoint voltage.
3. Maximum possible skew between L3_CLK0 and L3_CLK1. This parameter is critical to the address and control signals which are common to both SRAM chips in the L3.
4. Maximum possible skew between L3_CLK0 and L3_ECHO_CLK1 or between L3_CLK1 and L3_ECHO_CLK3 for PB2 or Late Write SRAM. This parameter is critical to the read data signals because the processor uses the feedback loop to latch data driven from the SRAM, each of which drives data based on L3_CLK0 or L3_CLK1.
5. Guaranteed by design and not tested. The input jitter on SYSCLK affects L3 output clocks and the L3 address, data and control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L3 timing analysis. The clock-to-clock jitter shown here is uncertainty in the internal clock period caused by supply voltage noise or thermal effects. This is also comprehended in the AC timing specifications and need not be considered in the L3 timing analysis.
6. L3 I/O voltage mode must be configured by L3VSEL as described in Table 6-1 on page 13, and voltage supplied at GV_{DD} must match mode selected as specified in "Recommended Operating Conditions[1]" on page 12.

More specifically, certain signals within groups should be delay-matched with others in the same group while intergroup routing is less critical. Only the address and control signals are common to both SRAMs and additional timing margin is available for these signals. The double-clocked data signals are grouped with individual clocks as shown in Figure 7-6 on page 30 or Figure 7-8 on page 32, depending on the type of SRAM. For example, for the MSUG2 DDR SRAM (see Figure 7-6); L3DATA[0:31], L3DP[0:3], and L3_CLK[0] form a closely coupled group of outputs from the PC7457; while L3DATA[0:15], L3DP[0:1], and L3_ECHO_CLK[0] form a closely coupled group of inputs.

The PC7450 RISC Microprocessor Family User's Manual refers to logical settings called "sample points" used in the synchronization of reads from the receive FIFO. The computation of the correct value for this setting is system-dependent and is described in the PC7450 RISC Microprocessor Family User's Manual.

Three specifications are used in this calculation and are given in Table 7-5 on page 27. It is essential that all three specifications are included in the calculations to determine the sample points as incorrect settings can result in errors and unpredictable behavior. For more information, see the PC7450 RISC Microprocessor Family User's Manual.

Table 7-5. Sample Points Calculation Parameters

Symbol	Parameter	Max	Unit
t_{AC}	Delay from processor clock to internal_L3_CLK(1)	3/4	t_{L3_CLK}
t_{CO}	Delay from internal_L3_CLK to L3_CLK[n] output pins(2)	3	ns
t_{ECI}	Delay from L3_ECHO_CLK[n] to receive latch(3)	3	ns

Notes:
1. This specification describes a logical offset between the internal clock edge used to launch the L3 address and control signals (this clock edge is phase-aligned with the processor clock edge) and the internal clock edge used to launch the L3_CLK[n] signals. With proper board routing, this offset ensures that the L3_CLK[n] edge will arrive at the SRAM within a valid address window and provide adequate setup and hold time. This offset is reflected in the L3 bus interface AC timing specifications, but must also be separately accounted for in the calculation of sample points and, thus, is specified here.
2. This specification is the delay from a rising or falling edge on the internal_L3_CLK signal to the corresponding rising or falling edge at the L3CLK[n] pins.
3. This specification is the delay from a rising or falling edge of L3_ECHO_CLK[n] to data valid and ready to be sampled from the FIFO.

7.2.4.1 Effects of L3OHCR Settings on L3 Bus AC Specifications

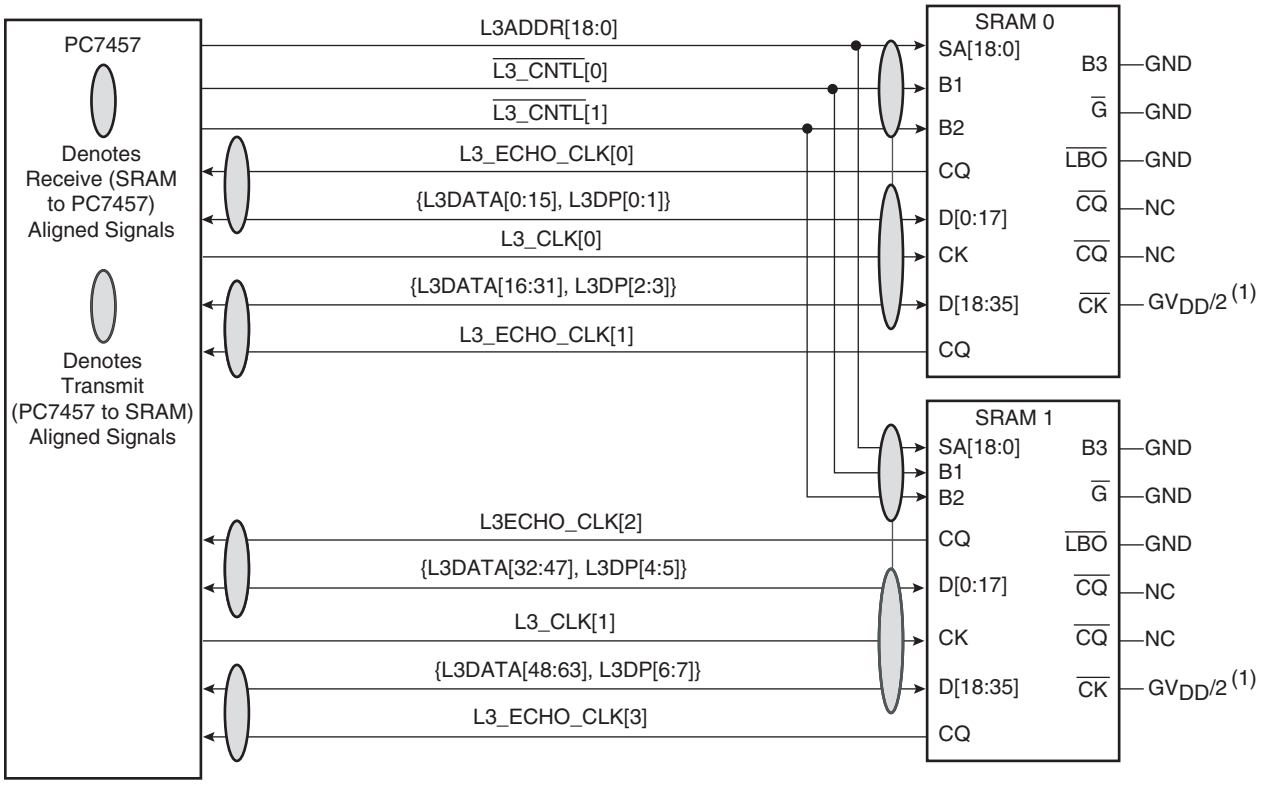
The AC timing of the L3 interface can be adjusted using the L3 Output Hold Control Register (L3OCHR).

Each field controls the timing for a group of signals. The AC timing specifications presented herein represent the AC timing when the register contains the default value of 0x0000_0000. Incrementing a field delays the associated signals, increasing the output valid time and hold time of the affected signals. In the special case of delaying an L3_CLK signal, the net effect is to decrease the output valid and output hold times of all signals being latched relative to that clock signal. The amount of delay added is summarized in Table 7-6 on page 28. Note that these settings affect output timing parameters only and don't impact input timing parameters of the L3 bus in any way.

8. Assumes default value of L3OHCR. See "Effects of L3OHCR Settings on L3 Bus AC Specifications" on page 27 for more information.
9. L3 I/O voltage mode must be configured by L3VSEL as described in Table 6-1 on page 13, and voltage supplied at GV_{DD} must match mode selected as specified in "Recommended Operating Conditions(1)" on page 12.

Figure 7-6 shows the typical connection diagram for the PC7457 interfaced to MSUG2 DDR SRAMs.

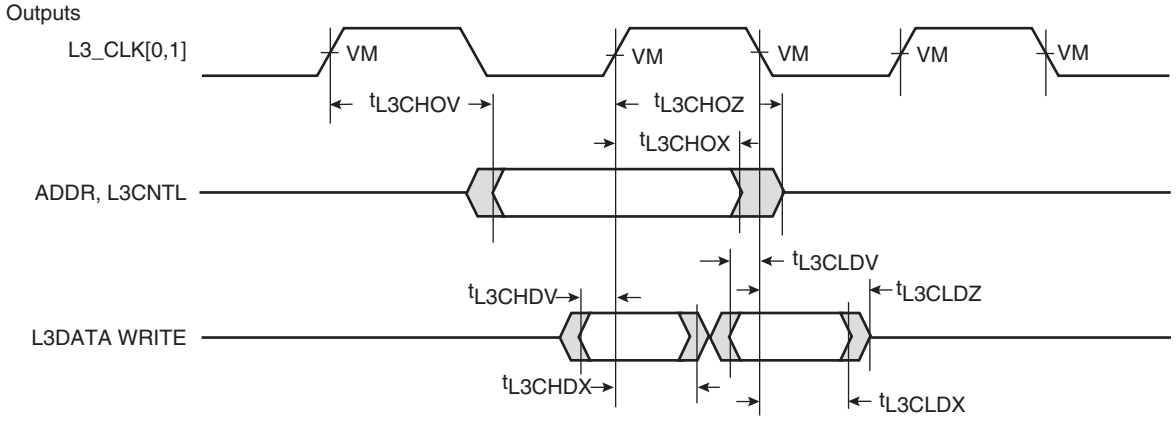
Figure 7-6. Typical Source Synchronous 4M bytes L3 Cache DDR Interface



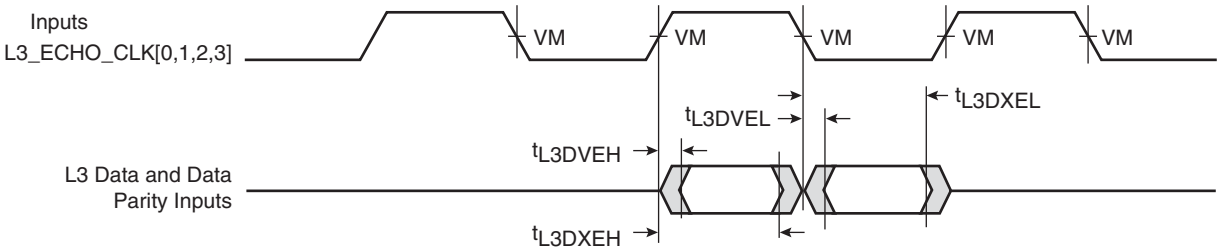
Note: 1. Or as recommended by SRAM manufacturer for single-ended clocking.

Figure 7-7 shows the L3 bus timing diagrams for the PC7457 interfaced to MSUG2 SRAMs.

Figure 7-7. L3 Bus Timing Diagrams for L3 Cache DDR SRAMs



Note: t_{L3CHDV} and t_{L3CLDV} as drawn here will be negative numbers, that is, output valid time will be time before the clock edge.



Notes: 1. t_{L3DVEH} and t_{L3DVEL} as drawn here will be negative numbers, that is, input setup time will be time after the clock edge.
2. VM = Midpoint Voltage ($GV_{DD}/2$)

7.2.5 L3 Bus AC Specifications for PB2 and Late Write SRAMs

When using PB2 or Late Write SRAMs at the L3 interface, the parts should be connected as shown in Figure 7-8 on page 32. These SRAMs are synchronous to the PC7457; one L3_CLKn signal is output to each SRAM to latch address, control, and write data. Read data is launched by the SRAM synchronous to the delayed L3_CLKn signal it received. The PC7457 needs a copy of that delayed clock which launched the SRAM read data to know when the returning data will be valid. Therefore, L3_ECHO_CLK1 and L3_ECHO_CLK3 must be routed halfway to the SRAMs and returned to the PC7457 inputs L3_ECHO_CLK0 and L3_ECHO_CLK2, respectively. Thus, L3_ECHO_CLK0 and L3_ECHO_CLK2 are phase-aligned with the input clock received at the SRAMs. The PC7457 will latch the incoming data on the rising edge of L3_ECHO_CLK0 and L3_ECHO_CLK2.Table 7-8 provides the L3 bus interface AC timing specifications for the configuration shown in Figure 7-8, assuming the timing relationships of Figure 7-9 and the loading of Figure 7-5 on page 26.

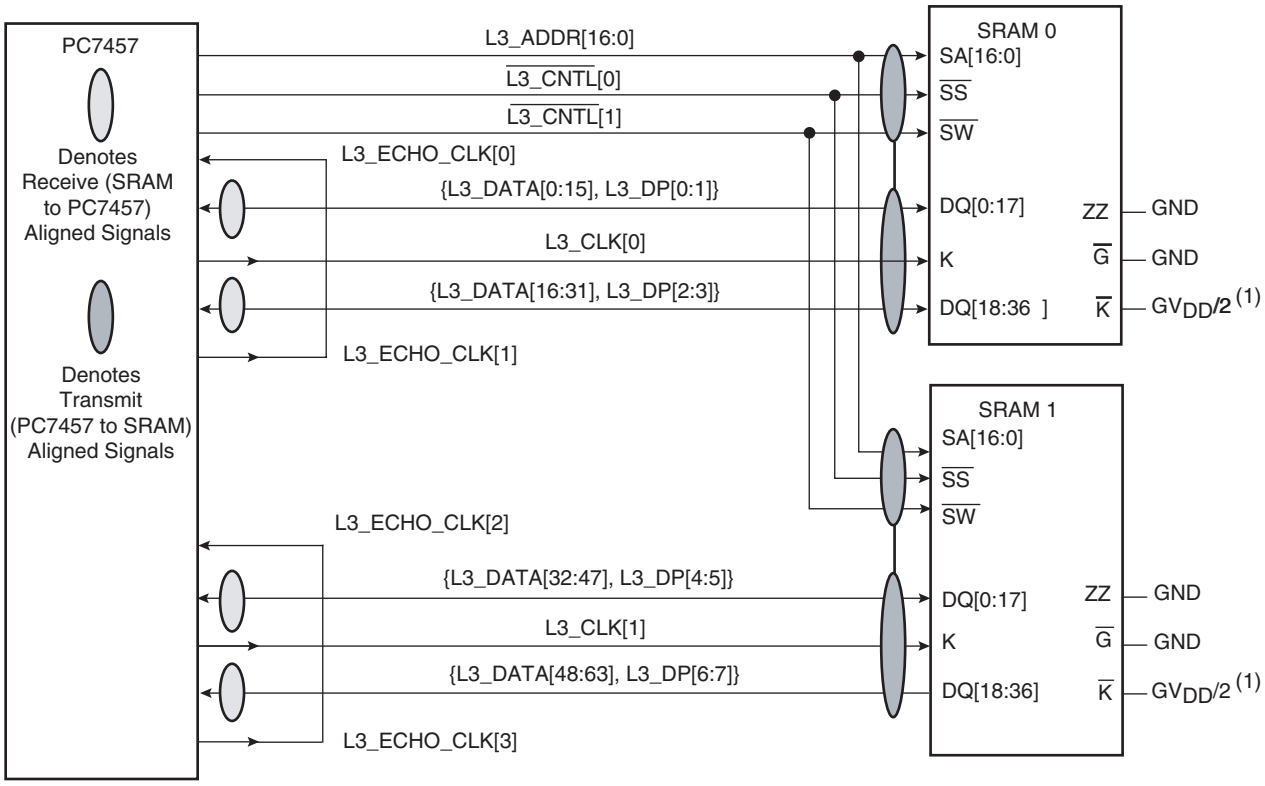
Table 7-8. L3 Bus Interface AC Timing Specifications for PB2 and Late Write SRAMs at Recommended Operating Conditions (see page 12)

Symbol	Parameter	All Speed Grades		Unit
		Min	Max	
t_{L3CR}, t_{L3CF}	L3_CLK rise and fall time(1)(2)	–	0.75	ns
t_{L3DVEH}	Setup times: Data and parity(2)(3)	0.1	–	ns
t_{L3DXEH}	Input hold times: Data and parity(2)(3)	–	0.7	ns
t_{L3CHDV}	Valid times: Data and parity(2)(4)(5)	–	2.5	ns
t_{L3CHOV}	Valid times: All other outputs(5)	–	1.8	ns
t_{L3CHDX}	Output hold times: Data and parity(2)(4)(5)	1.4	–	ns
t_{L3CHOX}	Output hold times: All other outputs(2)(5)	1.0	–	ns
t_{L3CHDZ}	L3_CLK to high impedance: Data and parity(2)	–	3.0	ns
t_{L3CHOZ}	L3_CLK to high impedance: All other outputs(2)	–	3.0	ns

Notes: 1. Rise and fall times for the L3_CLK output are measured from 20% to 80% of GV_{DD}.
2. Timing behavior and characterization are currently being evaluated.
3. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L3_ECHO_CLKn (see Figure 7-7 on page 30). Input timings are measured at the pins.
4. All output specifications are measured from the midpoint voltage of the rising edge of L3_CLKn to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (see Figure 7-7).
5. Assumes default value of L3OHCR. See "Effects of L3OHCR Settings on L3 Bus AC Specifications" on page 27" for more information.

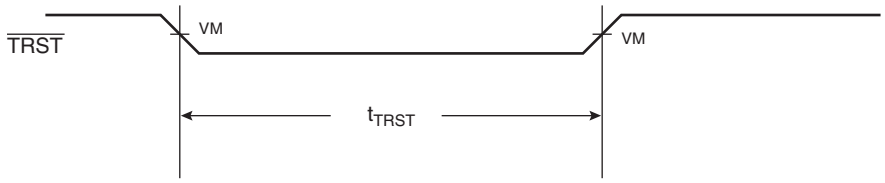
Figure 7-8 shows the typical connection diagram for the PC7457 interfaced to PB2 SRAMs or Late Write SRAMs.

Figure 7-8. Typical Synchronous 1M Byte L3 Cache Late Write or PB2 Interface



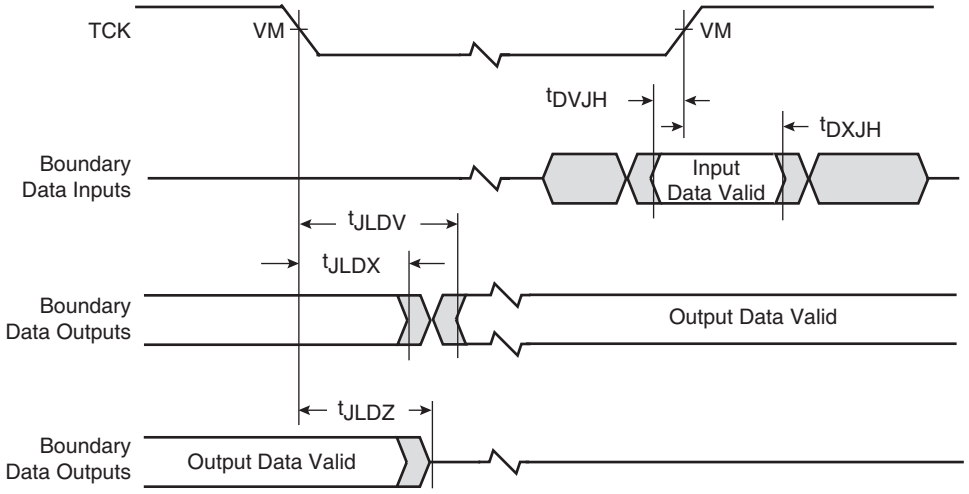
Note: 1. Or as recommended by SRAM manufacturer for single-ended clocking.

Figure 7-13. $\overline{\text{TRST}}$ Timing Diagram



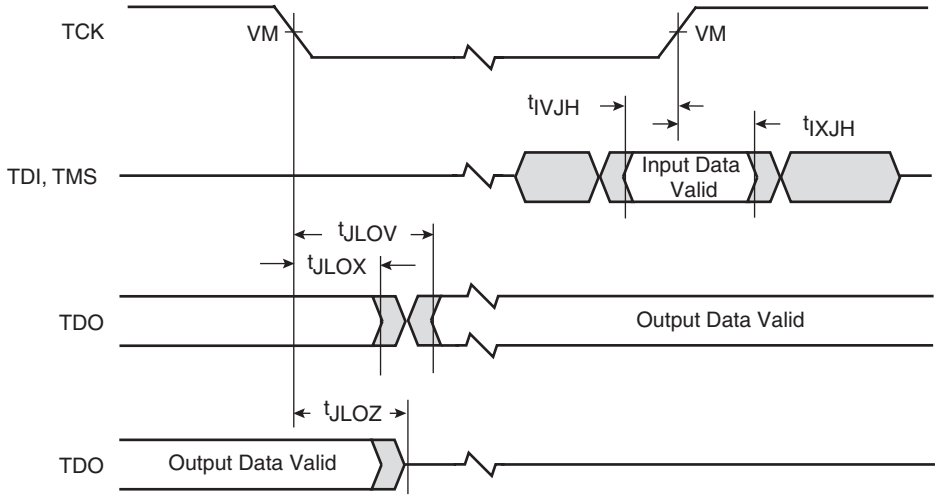
Note: VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 7-14. Boundary-scan Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 7-15. Test Access Port Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

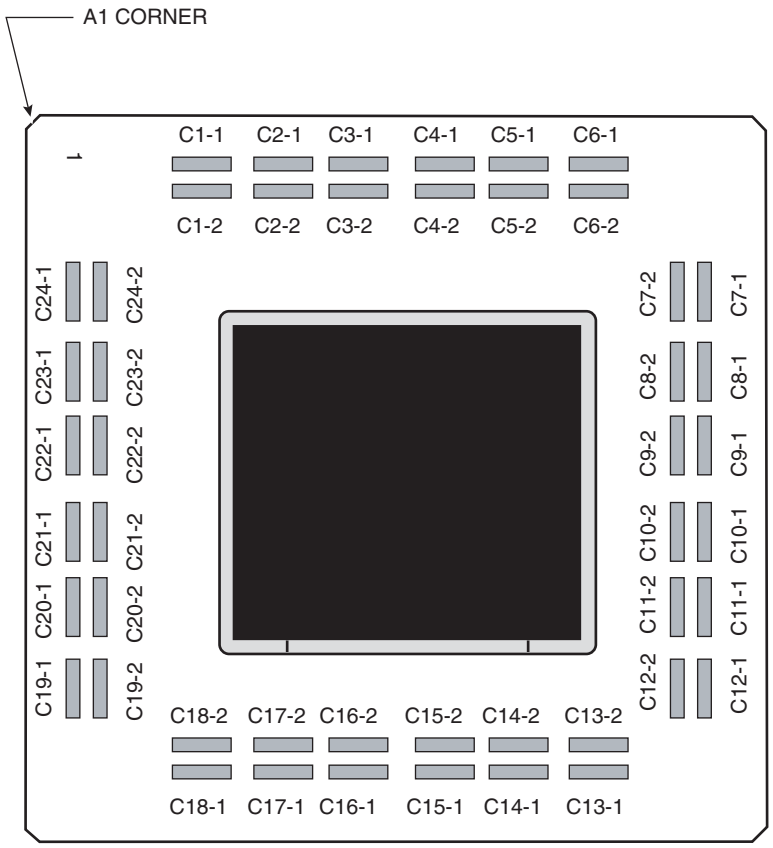
Table 8-1. Pinout Listing for the PC7457, 483 CBGA and HCTE Packages (Continued)

Signal Name	Pin Number	Active	I/O	I/F Select[1]
$\overline{\text{INT}}$	J6	Low	Input	BVSEL
L1_TSTCLK[10]	H4	High	Input	BVSEL
L2_TSTCLK[12]	J2	High	Input	BVSEL
L3VSEL[6][7]	A4	High	Input	N/A
L3ADDR[18:0]	H11, F20, J16, E22, H18, G20, F22, G22, H20, K16, J18, H22, J20, J22, K18, K20, L16, K22, L18	High	Output	L3VSEL
L3_CLK[0:1]	V22, C17	High	Output	L3VSEL
$\overline{\text{L3\_CNTL}}$[0:1]	L20, L22	Low	Output	L3VSEL
L3DATA[0:63]	AA19, AB20, U16, W18, AA20, AB21, AA21, T16, W20, U18, Y22, R16, V20, W22, T18, U20, N18, N20, N16, N22, M16, M18, M20, M22, R18, T20, U22, T22, R20, P18, R22, M15, G18, D22, E20, H16, C22, F18, D20, B22, G16, A21, G15, E17, A20, C19, C18, A19, A18, G14, E15, C16, A17, A16, C15, G13, C14, A14, E13, C13, G12, A13, E12, C12	High	I/O	L3VSEL
L3DP[0:7]	AB19, AA22, P22, P16, C20, E16, A15, A12	High	I/O	L3VSEL
L3_ECHO_CLK[0,2]	V18, E18	High	Input	L3VSEL
L3_ECHO_CLK[1,3]	P20, E14	High	I/O	L3VSEL
$\overline{\text{LSSD\_MODE}}$[7][13]	F6	Low	Input	BVSEL
$\overline{\text{MCP}}$	B8	Low	Input	BVSEL
No Connect[14]	A8, A11, B6, B11, C11, D11, D3, D5, E11, E7, F2, F11, G2, H9	–	–	N/A
OV_{DD}	B3, C5, C7, C10, D2, E3, E9, F5, G3, G9, H7, J5, K3, L7, M5, N3, P7, R4, T3, U5, U7, U11, U15, V3, V9, V13, Y2, Y5, Y7, Y10, Y17, Y19, AA4, AA15	–	–	N/A
PLL_CFG[0:4]	A2, F7, C2, D4, H8	High	Input	BVSEL
$\overline{\text{PMON\_IN}}$[15]	E6	Low	Input	BVSEL
$\overline{\text{PMON\_OUT}}$	B4	Low	Output	BVSEL
$\overline{\text{QACK}}$	K7	Low	Input	BVSEL
$\overline{\text{QREQ}}$	Y1	Low	Output	BVSEL
$\overline{\text{SHD}}$[0:1]	L4, L8	Low	I/O	BVSEL
$\overline{\text{SMI}}$	G8	Low	Input	BVSEL
$\overline{\text{SRESET}}$	G1	Low	Input	BVSEL
SYSCLK	D6	–	Input	BVSEL
$\overline{\text{TA}}$	N8	Low	Input	BVSEL
TBEN	L3	High	Input	BVSEL
$\overline{\text{TBST}}$	B7	Low	Output	BVSEL
TCK	J7	High	Input	BVSEL
TDI[7]	E4	High	Input	BVSEL
TDO	H1	High	Output	BVSEL
$\overline{\text{TEA}}$	T1	Low	Input	BVSEL

10. Substrate Capacitors for the PC7457, 483 CBGA

Figure 10-1 shows the connectivity of the substrate capacitor pads for the PC7457, 483 CBGA. All capacitors are 100 nF.

Figure 10-1. Substrate Bypass Capacitors for the PC7457, 483 CBGA

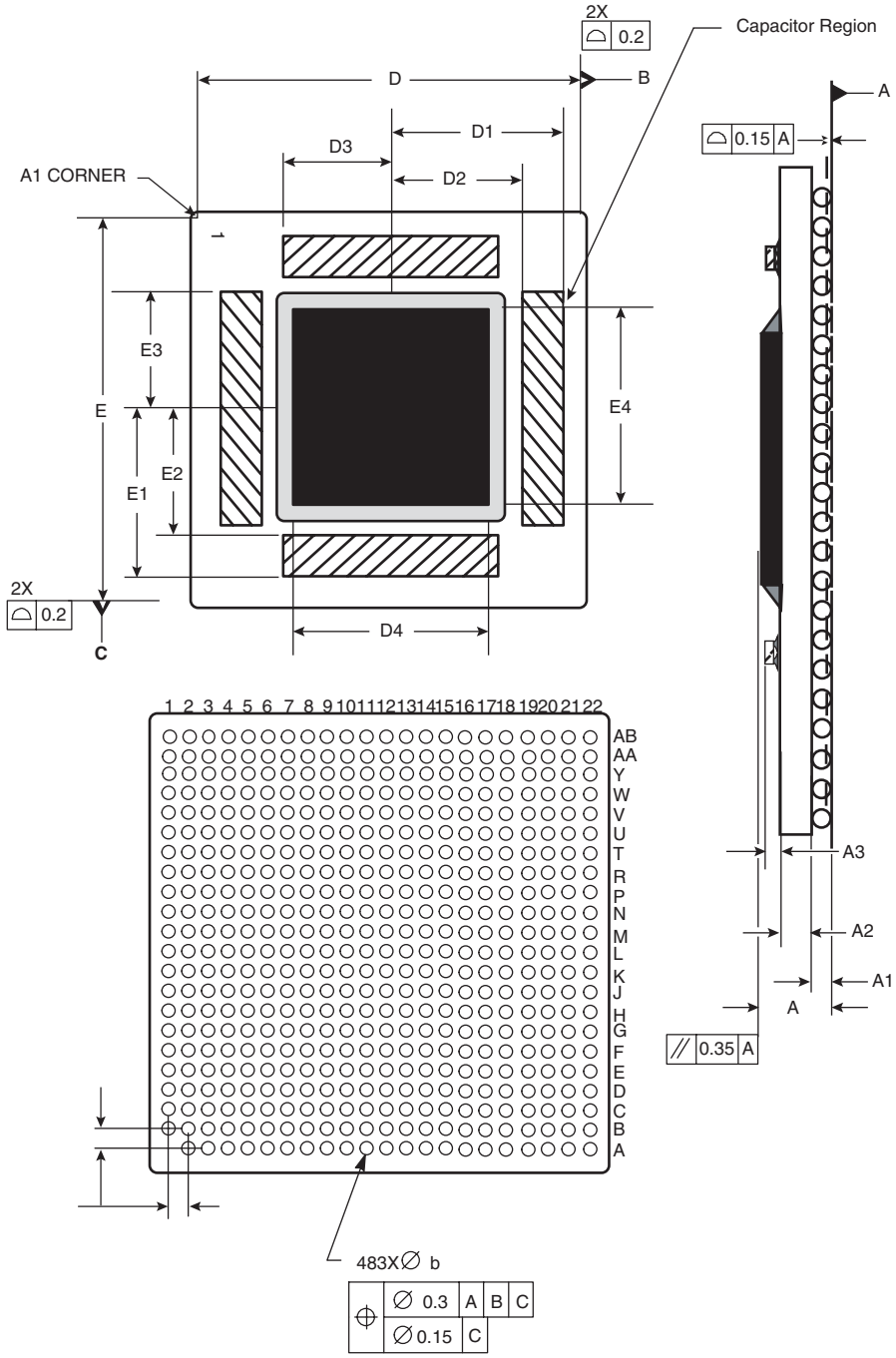


Capacitor	Pad Number	
	-1	-2
C1	GND	OV_{DD}
C2	GND	V_{DD}
C3	GND	GV_{DD}
C4	GND	V_{DD}
C5	GND	V_{DD}
C6	GND	GV_{DD}
C7	GND	V_{DD}
C8	GND	V_{DD}
C9	GND	GV_{DD}
C10	GND	V_{DD}
C11	GND	V_{DD}
C12	GND	GV_{DD}
C13	GND	V_{DD}
C14	GND	V_{DD}
C15	GND	V_{DD}
C16	GND	OV_{DD}
C17	GND	V_{DD}
C18	GND	OV_{DD}
C19	GND	V_{DD}
C20	GND	V_{DD}
C21	GND	OV_{DD}
C22	GND	V_{DD}
C23	GND	V_{DD}
C24	GND	V_{DD}

13. Mechanical Dimensions for the PC7457, 483 HCTE ROHS compliant

Figure 13-1 provides the mechanical dimensions and bottom surface nomenclature for the PC7457, 483 HCTE package.

Figure 13-1. Mechanical Dimensions and Bottom Surface Nomenclature for the PC7457, 483 HCTE Package

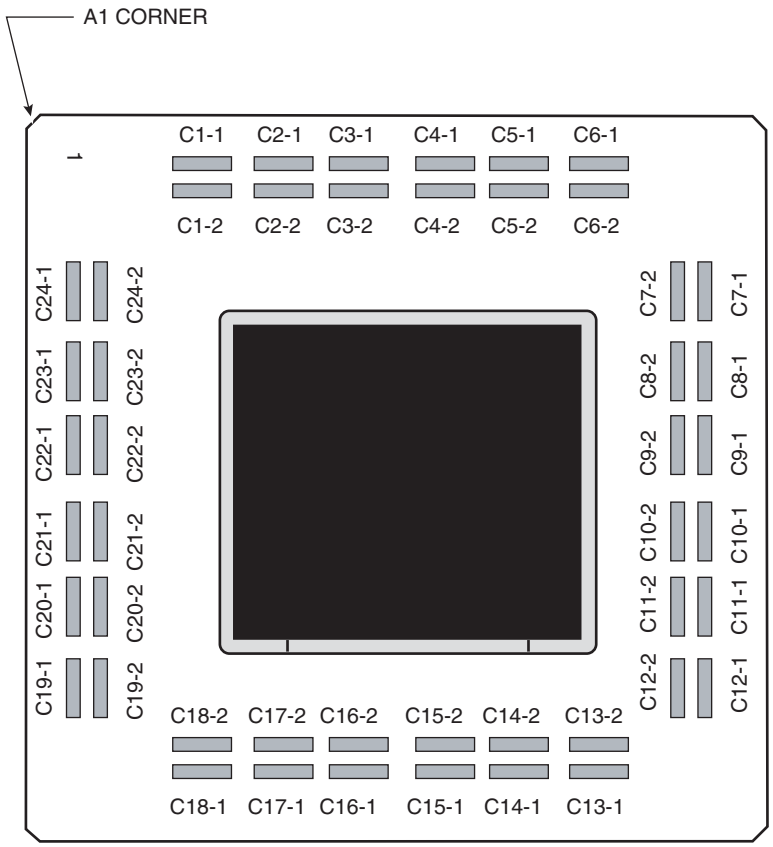


	Millimeters	
DIM	MIN	MAX
A	2.32	2.80
A1	0.4	0.6
A2	1.10	1.30
A3	–	0.6
b	0.6	0.9
D	29 BSC	
D1	–	12.5
D2	8.5	–
D3	–	8.4
D4	10.9	11.1
e	1.27 BSC	
E	29 BSC	
E1	–	12.5
E2	8.5	–
E3	–	8.4
E4	9.55	9.75

14. Substrate Capacitors for the PC7457, 483 HCTE ROHS Compliant

Figure 12-1 shows the connectivity of the substrate capacitor pads for the PC7457, 483 HCTE. All capacitors are 100 nF.

Figure 14-1. Substrate Bypass Capacitors for the PC7457, 483 HCTE



Capacitor	Pad Number	
	-1	-2
C1	GND	OV_{DD}
C2	GND	V_{DD}
C3	GND	GV_{DD}
C4	GND	V_{DD}
C5	GND	V_{DD}
C6	GND	GV_{DD}
C7	GND	V_{DD}
C8	GND	V_{DD}
C9	GND	GV_{DD}
C10	GND	V_{DD}
C11	GND	V_{DD}
C12	GND	GV_{DD}
C13	GND	V_{DD}
C14	GND	V_{DD}
C15	GND	V_{DD}
C16	GND	OV_{DD}
C17	GND	V_{DD}
C18	GND	OV_{DD}
C19	GND	V_{DD}
C20	GND	V_{DD}
C21	GND	OV_{DD}
C22	GND	V_{DD}
C23	GND	V_{DD}
C24	GND	V_{DD}

Table 15-1. PC7457 Microprocessor PLL Configuration Example for 1267 MHz Parts (Continued)

PLL_CFG[0:4]	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
			Bus (SYSCLK) Frequency							
			33.3 MHz	50 MHz	66.6 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz
10101	10x	2x			667 (1333)	750 (1500)	830 (1660)	1000 (2000)		
10001	10.5x	2x			700 (1400)	938 (1876)	872 (1744)	1050 (2100)		
10011	11x	2x			733 (1466)	825 (1650)	913 (1826)	1100 (2200)		
00000	11.5x	2x			766 (532)	863 (1726)	955 (1910)	1150 (2300)		
10111	12x	2x		600 (1200)	800 (1600)	900 (1800)	996 (1992)	1200 (2400)		
11111	12.5x	2x		600 (1200)	833 (1666)	938 (1876)	1038 (2076)	1250 (2500)		
01011	13x	2x		650 (1300)	865 (1730)	975 (1950)	1079 (2158)			
11100	13.5x	2x		675 (1350)	900 (1800)	1013 (2026)	1121 (2242)			
11001	14x	2x		700 (1400)	933 (1866)	1050 (2100)	1162 (2324)			
00011	15x	2x		750 (1500)	1000 (2000)	1125 (2250)	1245 (2490)			
11011	16x	2x		800 (1600)	1066 (2132)	1200 (2400)				
00001	17x	2x		850 (1900)	1132 (2264)					
00101	18x	2x	600 (1200)	900 (1800)	1200 (2400)					
00111	20x	2x	667 (1334)	1000 (2000)						
01001	21x	2x	700 (1400)	1050 (2100)						
01101	24x	2x	800 (1600)	1200 (2400)						
11101	28x	2x	933 (1866)							
00110	PLL bypass		PLL off, SYSCLK clocks core circuitry directly							
11110	PLL off		PLL off, no core clocking occurs							

Notes: 1. PLL_CFG[0:4] settings not listed are reserved.

2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the PC7455; See “Clock AC Specifications” on page 20. for valid SYSCLK, core, and VCO frequencies.

3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly and the PLL is disabled. However, the bus interface unit requires a 2x clock to function. Therefore, an additional signal, EXT_QUAL, must be driven at one-half the frequency of SYSCLK and offset in phase to meet the required input setup t_{IVKH} and hold time t_{IXKH} (see Table 7-3 on page 22). The result is that the processor bus frequency is one-half SYSCLK while the internal processor is clocked at SYSCLK frequency. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the PC7455 regardless of the SYSCLK input.

15.1.2 L3 Clocks

The PC7457 generates the clock for the external L3 synchronous data SRAMs by dividing the core clock frequency of the PC7457. The core-to-L3 frequency divisor for the L3 PLL is selected through the L3_CLK bits of the L3CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the PC7457 core, and timing analysis of the circuit board routing. Table 15-2 shows various example L3 clock frequencies that can be obtained for a given set of core frequencies.

Table 15-2. Sample Core-to-L3 Frequencies[1]

Core Frequency (MHz)	÷2	÷2.5	÷3	÷3.5	÷4	÷4.5	÷5	÷5.5	÷6	÷6.5	÷7	÷7.5	÷8
500	250	200	167	143	125	111	100	91	83	77	71	67	63
533	266	213	178	152	133	118	107	97	89	82	76	71	67
550	275	220	183	157	138	122	110	100	92	85	79	73	69
600	300	240	200	171	150	133	120	109	100	92	86	80	75
650	325	260	217	186	163	144	130	118	108	100	93	87	81
666	333	266	222	190	167	148	133	121	111	102	95	89	83
700	350	280	233	200	175	156	140	127	117	108	100	93	88
733	367	293	244	209	183	163	147	133	122	113	105	98	92
800	400	320	266	230	200	178	160	145	133	123	114	107	100
866	433	347	289	248	217	192	173	157	145	133	124	115	108
933	467	373	311	266	233	207	187	170	156	144	133	124	117
1000	500	400	333	285	250	222	200	182	166	154	143	133	125
1050[2]	525	420	350	300	263	233	191	191	175	162	150	140	131
1100[2]	550	440	367	314	275	244	200	200	183	169	157	147	138
1150[2]	575	460	383	329	288	256	209	209	192	177	164	153	144
1200[2]	600	480	400	343	300	267	218	218	200	185	171	160	150
1250[2]	638	500	417	357	313	278	227	227	208	192	179	167	156
1300[2]	650	520	433	371	325	289	236	236	217	200	186	173	163

Notes:
1. The core and L3 frequencies are for reference only. Note that maximum L3 frequency is design dependent. Some examples may represent core or L3 frequencies which are not useful, not supported, or not tested for the PC7457; see "L3 Clock AC Specifications" on page 24 for valid L3_CLK frequencies and for more information regarding the maximum L3 frequency.
2. Not all core frequencies are supported by all speed grades; see Table 7-2 on page 20 for minimum and maximum core frequency specifications.

18. Document Revision History

Table 18-1 provides a revision history for this hardware specification.

Table 18-1. Document Revision History

Revision Number	Date	Substantive Change(s)
D	03/06	Remove PC7447. Modification Table 6-1 on page 13? and ordering information
C	06/2005	Updated document to new Atmel template
		Updated section numbering and changed reference from part number specifications to addendums
		Added Rev. 1.2 devices, including increased L3 clock max frequency to 250 MHz and improved L3 AC timing
		Table 6-2 on page 13: Added CTE information
		Table 7-2 on page 20: Modified jitter specifications to conform to JEDEC standards, changed jitter specification to cycle-to-cycle jitter (instead of long- and short-term jitter); changed jitter bandwidth recommendations
		Table 7-7 on page 29: Deleted note 9 and renumbered.
		Table 7-8 on page 31: Deleted note 5 and renumbered
		Table 8-1 on page 38: Revised note 6
		Added Section 15.1.3 ”System Bus Clock (SYSCLK) and Spread Spectrum Sources” on page 50
		Section 15.2 ”PLL Power Supply Filtering” on page 50: Changed filter resistor recommendations. Recommend 10Ω resistor for all production devices, including production Rev. 1.1 devices. 400Ω resistor needed only for early Rev. 1.1 devices.
		Table 18-1: Reversed the order of revision numbers.
		Section 15.1.1 on page 47: Corrected note regarding different PLL configurations for earlier devices; all PC7457 devices to date conform to this table
		Section 15.6 on page 52: Added information about unused L3_ADDR signals.
		HCTE package information
		Preliminary specification α-site release subsequent to preliminary specification β-site Motorola changed to Freescale
B	11/2004	Figure 7-3 on page 22: Corrected pin lists for input and output AC timing to correctly show $\overline{\text{HIT}}$ as an output-only signal
		Added specifications for 1267 MHz devices; removed specs for 1300 MHz devices.
		Changed recommendations regarding use of L3 clock jitter in AC timing analysis in Section “L3 Clock AC Specifications” on page 24; the L3 jitter is now fully comprehended in the AC timing specs and does not need to be included in the timing analysis