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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	933MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V
Operating Temperature	-40°C ~ 110°C (TJ)
Security Features	-
Package / Case	360-BCBGA
Supplier Device Package	360-HiTCE-CBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pcx7457vgu933nc

  - Instruction cache can provide four instructions per clock cycle; data cache can provide four words per clock cycle
  - Caches can be disabled in software
  - Caches can be locked in software
  - MESI data cache coherency maintained in hardware
  - Separate copy of data cache tags for efficient snooping
  - Parity support on cache and tags
  - No snooping of instruction cache except for icbi instruction
  - Data cache supports AltiVec LRU and transient instructions
  - Critical double- and/or quad-word forwarding is performed as needed. Critical quad-word forwarding is used for AltiVec loads and instruction fetches. Other accesses use critical double-word forwarding
- Level 2 (L2) cache interface
  - On-chip, 512 Kbyte, eight-way set-associative unified instruction and data cache
  - Fully pipelined to provide 32 bytes per clock cycle to the L1 caches
  - A total nine-cycle load latency for an L1 data cache miss that hits in L2
  - PLRU replacement algorithm
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - 64-byte, two-sectored line size
  - Parity support on cache
- Level 3 (L3) cache interface (not implemented on PC7447)
  - Provides critical double-word forwarding to the requesting unit
  - Internal L3 cache controller and tags
  - External data SRAMs
  - Support for 1, 2, and 4M bytes (MB) total SRAM space
  - Support for 1 or 2 MB of cache space
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - 64-byte (1 MB) or 128-byte (2 MB) sectored line size
  - Private memory capability for half (1 MB minimum) or all of the L3 SRAM space for a total of 1-, 2-, or 4-MB of private memory
  - Supports MSUG2 dual data rate (DDR) synchronous Burst SRAMs, PB2 pipelined synchronous Burst SRAMs, and pipelined (register-register) Late Write synchronous Burst SRAMs
  - Supports parity on cache and tags
  - Configurable core-to-L3 frequency divisors
  - 64-bit external L3 data bus sustains 64-bit per L3 clock cycle
- Separate memory management units (MMUs) for Instructions and data
  - 52-bit virtual address; 32- or 36-bit physical address
  - Address translation for 4 Kbyte pages, variable-sized blocks, and 256M bytes segments

  - Memory programmable as write-back/write-through, caching-inhibited/caching-allowed, and memory coherency enforced/memory coherency not enforced on a page or block basis
  - Separate IBATs and DBATs (eight each) also defined as SPRs
  - Separate instruction and data translation lookaside buffers (TLBs)
    Both TLBs are 128-entry, two-way set-associative, and use LRU replacement algorithm
    TLBs are hardware- or software-reloadable (that is, on a TLB miss a page table search is performed in hardware or by system software)

- Efficient data flow
  - Although the VR/LSU interface is 128 bits, the L1/L2/L3 bus interface allows up to 256 bits
  - The L1 data cache is fully pipelined to provide 128 bits/cycle to or from the VRs
  - L2 cache is fully pipelined to provide 256 bits per processor clock cycle to the L1 cache
  - As many as eight outstanding, out-of-order, cache misses are allowed between the L1 data cache and L2/L3 bus
  - As many as 16 out-of-order transactions can be present on the MPX bus
  - Store merging for multiple store misses to the same line. Only coherency action taken (address-only) for store misses merged to all 32 bytes of a cache block (no data tenure needed)
  - Three-entry finished store queue and five-entry completed store queue between the LSU and the L1 data cache
  - Separate additional queues for efficient buffering of outbound data (such as castouts and write-through stores) from the L1 data cache and L2 cache
- Multiprocessing support features include the following:
  - Hardware-enforced, MESI cache coherency protocols for data cache
  - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations
- Power and thermal management
  - 1.6V processor core
  - The following three power-saving modes are available to the system:

    Nap—Instruction fetching is halted. Only those clocks for the time base, decrementer, and JTAG logic remain running. The part goes into the doze state to snoop memory operations on the bus and then back to nap using a QREQ/QACK processor-system handshake protocol

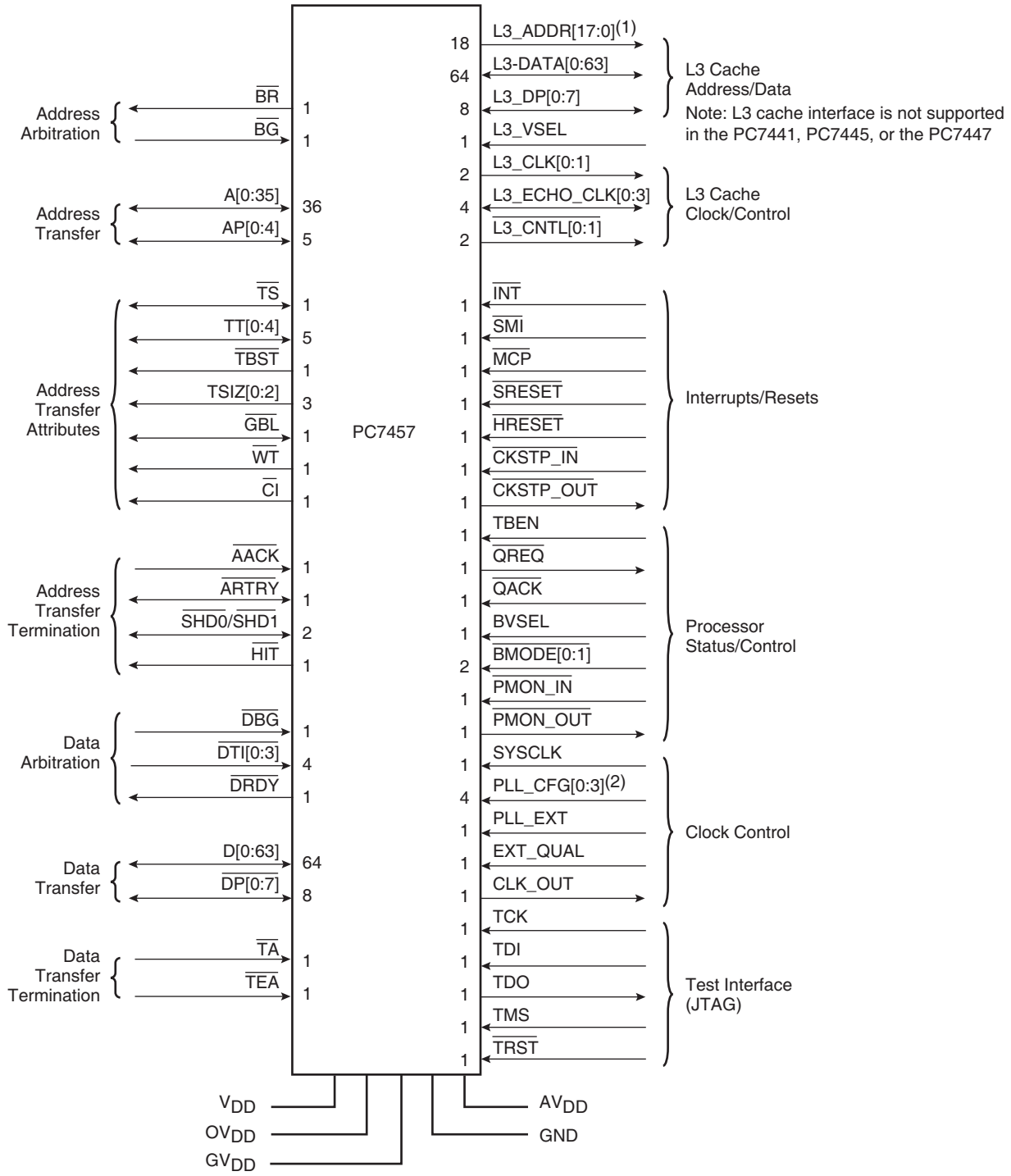
    Sleep—Power consumption is further reduced by disabling bus snooping, leaving only the PLL in a locked and running state. All internal functional units are disabled

    Deep sleep—When the part is in the sleep state, the system can disable the PLL. The system can then disable the SYSCLK source for greater system power savings. Power-on reset procedures for restarting and relocking the PLL must be followed on exiting the deep sleep state

  - Thermal management facility provides software-controllable thermal management. Thermal management is performed through the use of three supervisor-level registers and a PC7457-specific thermal management exception
  - Instruction cache throttling provides control of instruction fetching to limit power consumption
- Performance monitor can be used to help debug system designs and improve software efficiency
- In-system testability and debugging features through JTAG boundary-scan capability
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
  - Array built-in self test (ABIST) – factory test only
- Reliability and serviceability
  - Parity checking on system bus and L3 cache bus
  - Parity checking on the L2 and L3 cache tag arrays

4. Signal Description

Figure 4-1. PC7457 Microprocessor Signal Groups



Notes: 1. For the PC7457, there are 19 L3_ADDR signals, (L3_ADDR[0:18].
2. For the PC7447 and PM7457, there are 5 PLL_CFG signals, (PLL_CFG[0:4].

Table 6-1. Input Threshold Voltage Setting

BVSEL Signal	Processor Bus Input Threshold is Relative to:	L3VSEL Signal[1]	L3 Bus Input Threshold is Relative to:	Notes
0	1.8V	0	1.8V	(2)(3)
¬$\overline{\text{HRESET}}$	Not available	¬$\overline{\text{HRESET}}$	1.5V	(2)(4)
$\overline{\text{HRESET}}$	2.5V	$\overline{\text{HRESET}}$	2.5V	(2)
1	2.5V	1	2.5V	(2)

Notes:
1. Not implemented on PC7447.
2. Caution: The input threshold selection must agree with the OV_{DD}/GV_{DD} voltages supplied. See notes in "Absolute Maximum Ratings[1]" on page 11.
3. If used, pull-down resistors should be less than 250Ω
4. Applicable to L3 bus interface only. ¬$\overline{\text{HRESET}}$ is the inverse of $\overline{\text{HRESET}}$.

6.2 Thermal Characteristics

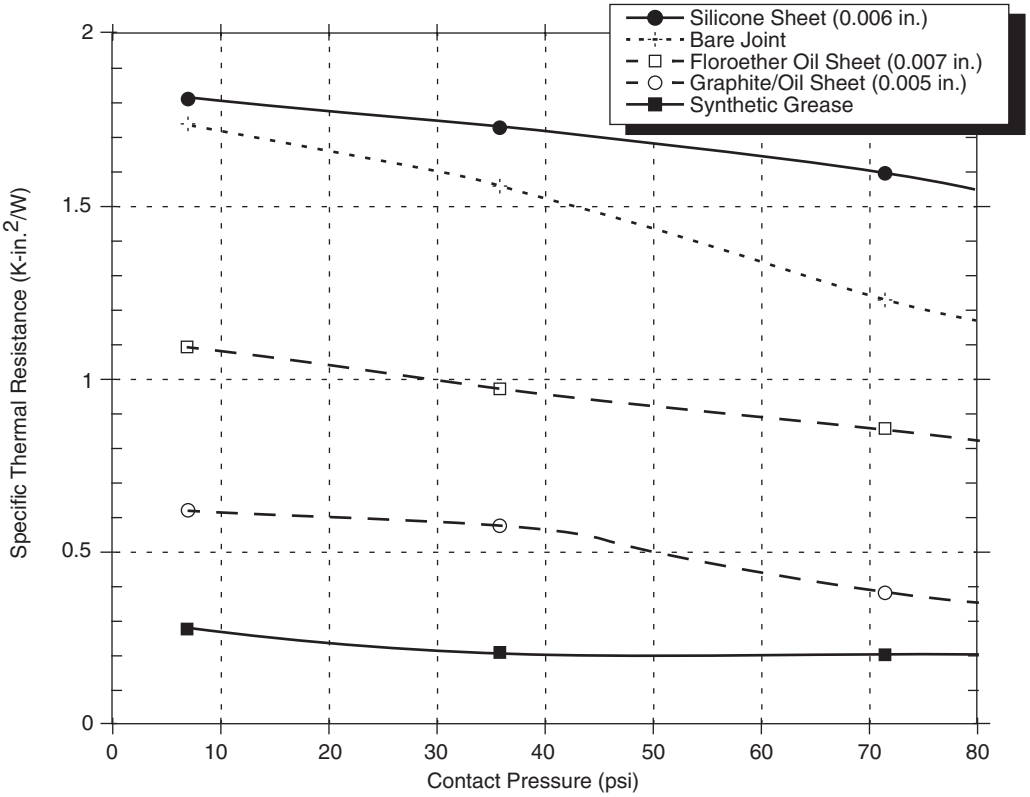
6.2.1 Package Characteristics

Table 6-2. Package Thermal Characteristics[1]

Symbol	Characteristic	Value		Unit
		PC7447 CBGA	PC7457 CBGA	
$R_{\theta JA}$[2][3]	Junction-to-ambient thermal resistance, natural convection	22	20	°C/W
$R_{\theta JMA}$[2][4]	Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	14	14	°C/W
$R_{\theta JMA}$[2][4]	Junction-to-ambient thermal resistance, 200 ft./min. airflow, single-layer (1s) board	16	15	°C/W
$R_{\theta JMA}$[2][4]	Junction-to-ambient thermal resistance, 200 ft./min. airflow, four-layer (2s2p) board	11	11	°C/W
$R_{\theta JB}$[5]	Junction-to-board thermal resistance	6	6	°C/W
$R_{\theta JC}$[6]	Junction-to-case thermal resistance	< 0.1	< 0.1	°C/W
	Coefficient of thermal expansion	6.8	6.8	ppm/°C

Notes:
1. See "Thermal Management Information" on page 15 for more details about thermal management.
2. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
3. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
4. Per JEDEC JESD51-6 with the board horizontal.
5. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
6. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.

Figure 6-4. Thermal Performance of Select Thermal Interface Material



6.2.5.1 *Heat Sink Selection Example*

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$T_J = T_I + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$

where:

T_J is the die-junction temperature
T_I is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
$R_{\theta JC}$ is the junction-to-case thermal resistance
$R_{\theta int}$ is the adhesive or interface material thermal resistance
$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance
P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_J) should be maintained less than the value specified in "Recommended Operating Conditions(1)" on page 12. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40° C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10° C.

The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 1.5° C/W. For example, assuming a Ta of 30° C, a Tr of 5° C, a CBGA package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 18.7W, the following expression for T_J is obtained:

Die-junction temperature: T_J = 30° C + 5° C + (0.1° C/W + 1.5° C/W + θ_{sa}) × 18.7W

7.2 Dynamic Characteristics

This section provides the AC electrical characteristics for the PC7457. After fabrication, functional parts are sorted by maximum processor core frequency as shown in section “Clock AC Specifications” and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency; See “Ordering Information” on page 59.

7.2.1 Clock AC Specifications

Table 7-2 provides the clock AC timing specifications as defined in Figure 7-1 and represents the tested operating frequencies of the devices. The maximum system bus frequency, f_{SYSCLK}, given in Table 7-2 is considered a practical maximum in a typical single-processor system. The actual maximum SYSCLK frequency for any application of the PC7457 will be a function of the AC timings of the PC7457, the AC timings for the system controller, bus loading, printed-circuit board topology, trace lengths, and so forth, and may be less than the value given in Table 7-2.

Table 7-2. Clock AC Timing Specifications (See “Recommended Operating Conditions(1)” on page 12)

		Maximum Processor Core Frequency						
		600 MHz		867 MHz		1000 MHz		
		V_{DD} = 1.1V		V_{DD} = 1.1V		V_{DD} = 1.1V		
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{CORE}(1)	Processor frequency	500	600	500	867	500	1000	MHz
f_{VCO}(1)	VCO frequency	1000	1200	1000	1733	1000	2000	MHz
f_{SYSCLK}(1)(2)	SYSCLK frequency	33	167	33	167	33	167	MHz
t_{SYSCLK}(2)	SYSCLK cycle time	6	30	6	30	6	30	ns
t_{KR}, t_{KF}(3)	SYSCLK rise and fall time	–	1	–	1	–	1	ns
t_{KHKL}/t_{SYSCLK}(4)	SYSCLK duty cycle measured at $OV_{DD}/2$	40	60	40	60	–	–	%
	SYSCLK jitter(5)(6)	–	150	–	150	–	–	ps
	Internal PLL relock time(7)	–	100	–	100	–	–	µs

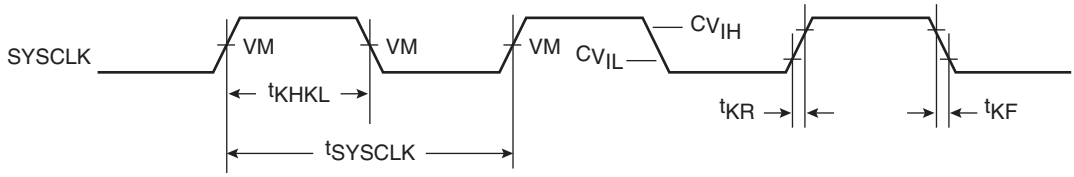
		Maximum Processor Core Frequency								
		867 MHz		1000 MHz		1200 MHz		1267 MHz		
		V_{DD} = 1.3V		V_{DD} = 1.3V		V_{DD} = 1.3V		V_{DD} = 1.3V		
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{CORE}(1)	Processor frequency	600	867	600	1000	600	1200	600	1267	MHz
f_{VCO}(1)	VCO frequency	1200	1733	1200	2000	1200	2400	1200	2534	MHz
f_{SYSCLK}(1)(2)	SYSCLK frequency	33	167	33	167	33	167	33	167	MHz
t_{SYSCLK}(2)	SYSCLK cycle time	6	30	6	30	6	30	6	30	ns
t_{KR}, t_{KF}(3)	SYSCLK rise and fall time	–	1	–	1	–	1	–	1	ns

Symbol	Characteristic	Maximum Processor Core Frequency								Unit
		867 MHz		1000 MHz		1200 MHz		1267 MHz		
		V_{DD} = 1.3V		V_{DD} = 1.3V		V_{DD} = 1.3V		V_{DD} = 1.3V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{KHKL}/t_{SYSCLK}[4]	SYSCLK duty cycle measured at $OV_{DD}/2$	40	60	40	60	40	60	40	60	%
	SYSCLK jitter[5][6]	–	±150	–	±150	–	±150	–	±150	ps
	Internal PLL relock time[7]	–	100	–	100	–	100	–	100	µs

Notes:
1. Caution: The SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency and PLL (VCO) frequency don't exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in "Core Clocks and PLL Configuration" on page 47 for valid PLL_CFG[0:4] settings
2. Assumes lightly-loaded, single-processor system.
3. Rise and fall times for the SYSCLK input measured from 0.4V to 1.4V.
4. Timing is guaranteed by design and characterization.
5. This represents total input jitter, short-term and long-term combined, and is guaranteed by design.
6. The SYSCLK driver's closed loop jitter bandwidth should be less than 1.5 MHz at -3 dB.
7. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

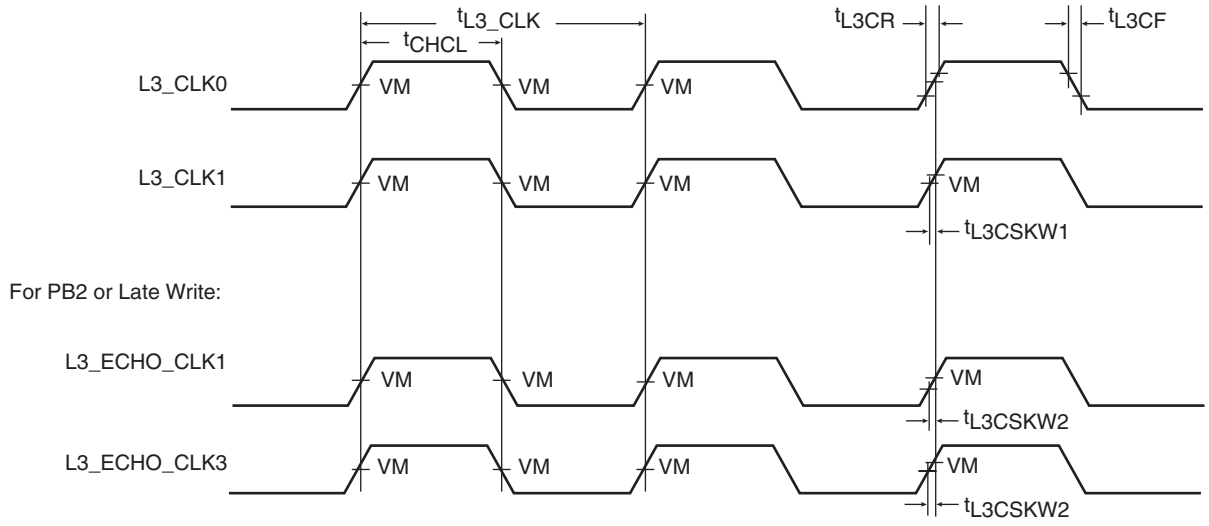
Figure 7-1 provides the SYSCLK input timing diagram.

Figure 7-1. SYSCLK Input Timing Diagram



VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 7-4. L3_CLK_OUT Output Timing Diagram

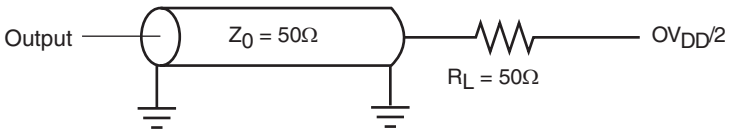


7.2.4 L3 Bus AC Specifications

The PC7457 L3 interface supports three different types of SRAM: source-synchronous, double data rate (DDR) MSUG2 SRAM, Late Write SRAMs, and pipeline burst (PB2) SRAMs. Each requires a different protocol on the L3 interface and a different routing of the L3 clock signals. The type of SRAM is programmed in L3CR[22:23] and the PC7457 then follows the appropriate protocol for that type. The designer must connect and route the L3 signals appropriately for each type of SRAM. Following are some observations about the L3 interface.

- The routing for the point-to-point signals (L3_CLK[0:1], L3DATA[0:63], L3DP[0:7], and L3_ECHO_CLK[0:3]) to a particular SRAM must be delay matched
- For 1M byte of SRAM, use L3_ADDR[16:0] (L3_ADDR[0] is LSB)
- For 2M bytes of SRAM, use L3_ADDR[17:0] (L3_ADDR[0] is LSB)
- No pull-up resistors are required for the L3 interface
- For high speed operations, L3 interface address and control signals should be a "T" with minimal stubs to the two loads; data and clock signals should be point-to-point to their single load. Figure 7-5 shows the AC test load for the L3 interface

Figure 7-5. AC Test Load for the L3 Interface



In general, if routing is short, delay-matched, and designed for incident wave reception and minimal reflection, there is a high probability that the AC timing of the PC7457 L3 interface will meet the maximum frequency operation of appropriately chosen SRAMs. This is despite the pessimistic, guard-banded AC specifications (see Table 7-6 on page 28, Table 7-7 on page 29, and Table 7-8 on page 31), the limitations of functional testers described in Section "L3 Clock AC Specifications" on page 24 and the uncertainty of clocks and signals which inevitably make worst-case critical path timing analysis pessimistic.

More specifically, certain signals within groups should be delay-matched with others in the same group while intergroup routing is less critical. Only the address and control signals are common to both SRAMs and additional timing margin is available for these signals. The double-clocked data signals are grouped with individual clocks as shown in Figure 7-6 on page 30 or Figure 7-8 on page 32, depending on the type of SRAM. For example, for the MSUG2 DDR SRAM (see Figure 7-6); L3DATA[0:31], L3DP[0:3], and L3_CLK[0] form a closely coupled group of outputs from the PC7457; while L3DATA[0:15], L3DP[0:1], and L3_ECHO_CLK[0] form a closely coupled group of inputs.

The PC7450 RISC Microprocessor Family User's Manual refers to logical settings called "sample points" used in the synchronization of reads from the receive FIFO. The computation of the correct value for this setting is system-dependent and is described in the PC7450 RISC Microprocessor Family User's Manual.

Three specifications are used in this calculation and are given in Table 7-5 on page 27. It is essential that all three specifications are included in the calculations to determine the sample points as incorrect settings can result in errors and unpredictable behavior. For more information, see the PC7450 RISC Microprocessor Family User's Manual.

Table 7-5. Sample Points Calculation Parameters

Symbol	Parameter	Max	Unit
t_{AC}	Delay from processor clock to internal_L3_CLK(1)	3/4	t_{L3_CLK}
t_{CO}	Delay from internal_L3_CLK to L3_CLK[n] output pins(2)	3	ns
t_{ECI}	Delay from L3_ECHO_CLK[n] to receive latch(3)	3	ns

Notes:
1. This specification describes a logical offset between the internal clock edge used to launch the L3 address and control signals (this clock edge is phase-aligned with the processor clock edge) and the internal clock edge used to launch the L3_CLK[n] signals. With proper board routing, this offset ensures that the L3_CLK[n] edge will arrive at the SRAM within a valid address window and provide adequate setup and hold time. This offset is reflected in the L3 bus interface AC timing specifications, but must also be separately accounted for in the calculation of sample points and, thus, is specified here.
2. This specification is the delay from a rising or falling edge on the internal_L3_CLK signal to the corresponding rising or falling edge at the L3CLK[n] pins.
3. This specification is the delay from a rising or falling edge of L3_ECHO_CLK[n] to data valid and ready to be sampled from the FIFO.

7.2.4.1 Effects of L3OHCR Settings on L3 Bus AC Specifications

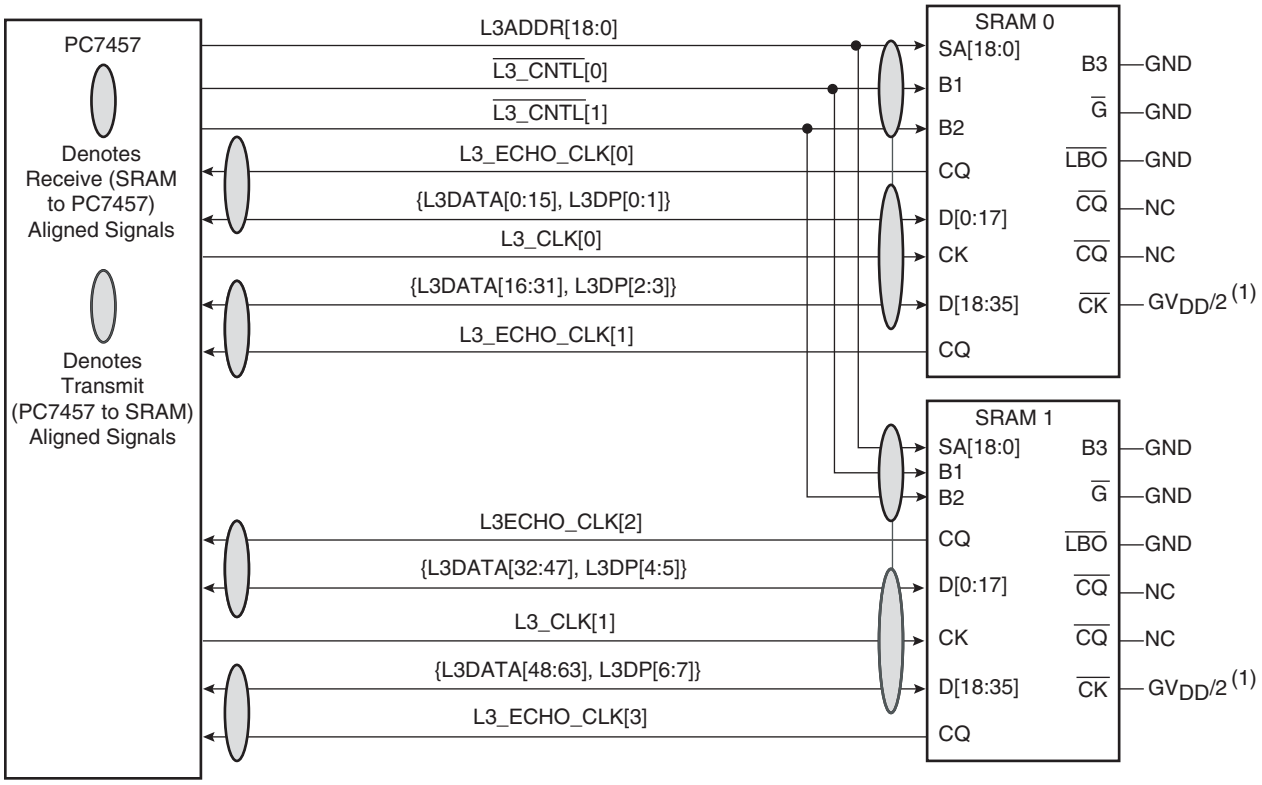
The AC timing of the L3 interface can be adjusted using the L3 Output Hold Control Register (L3OCHR).

Each field controls the timing for a group of signals. The AC timing specifications presented herein represent the AC timing when the register contains the default value of 0x0000_0000. Incrementing a field delays the associated signals, increasing the output valid time and hold time of the affected signals. In the special case of delaying an L3_CLK signal, the net effect is to decrease the output valid and output hold times of all signals being latched relative to that clock signal. The amount of delay added is summarized in Table 7-6 on page 28. Note that these settings affect output timing parameters only and don't impact input timing parameters of the L3 bus in any way.

8. Assumes default value of L3OHCR. See "Effects of L3OHCR Settings on L3 Bus AC Specifications" on page 27 for more information.
9. L3 I/O voltage mode must be configured by L3VSEL as described in Table 6-1 on page 13, and voltage supplied at GV_{DD} must match mode selected as specified in "Recommended Operating Conditions(1)" on page 12.

Figure 7-6 shows the typical connection diagram for the PC7457 interfaced to MSUG2 DDR SRAMs.

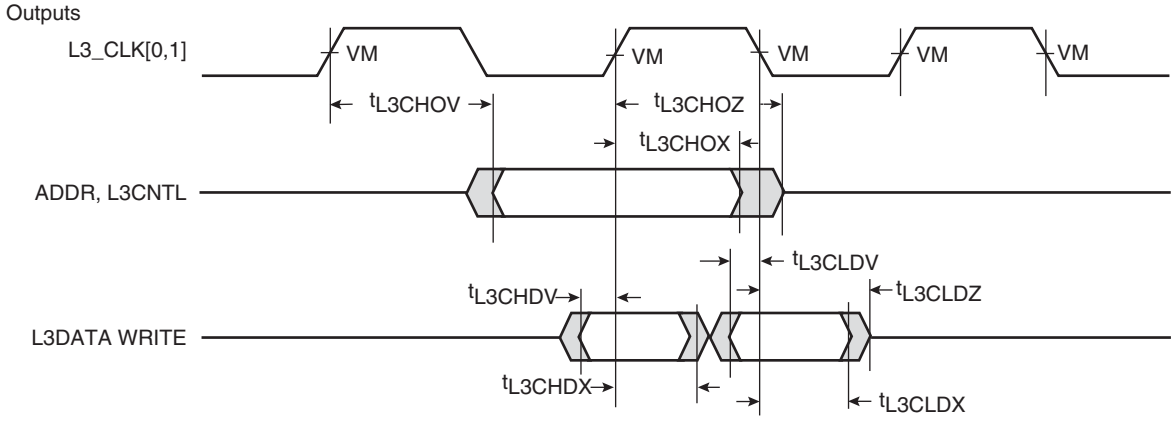
Figure 7-6. Typical Source Synchronous 4M bytes L3 Cache DDR Interface



Note: 1. Or as recommended by SRAM manufacturer for single-ended clocking.

Figure 7-7 shows the L3 bus timing diagrams for the PC7457 interfaced to MSUG2 SRAMs.

Figure 7-7. L3 Bus Timing Diagrams for L3 Cache DDR SRAMs



Note: t_{L3CHDV} and t_{L3CLDV} as drawn here will be negative numbers, that is, output valid time will be time before the clock edge.

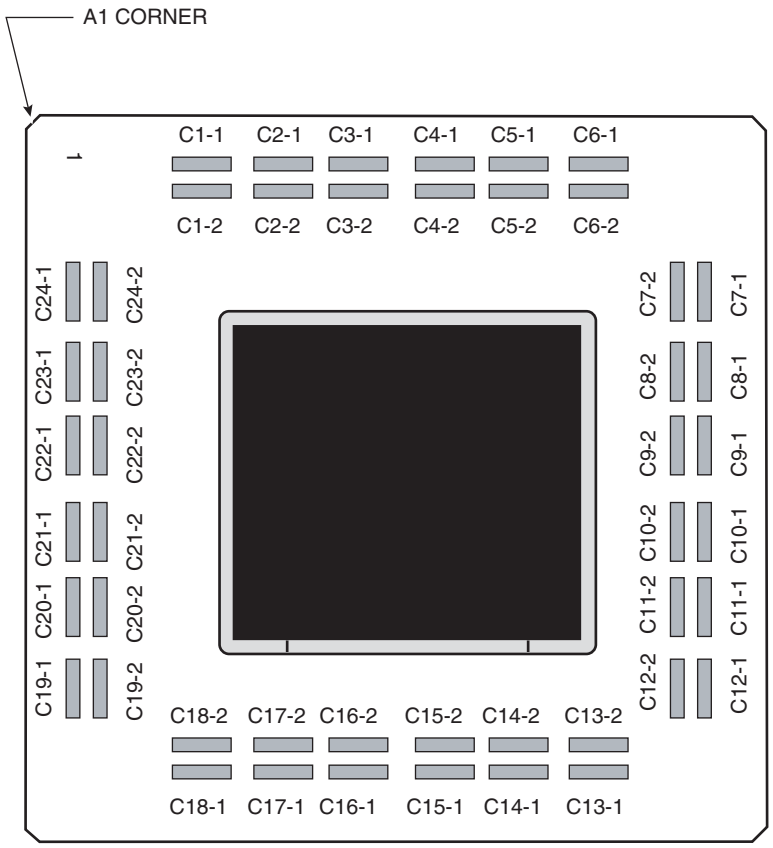
Table 8-1. Pinout Listing for the PC7457, 483 CBGA and HCTE Packages

Signal Name	Pin Number	Active	I/O	I/F Select[1]
A[0:35][2]	E10, N4, E8, N5, C8, R2, A7, M2, A6, M1, A10, U2, N2, P8, M8, W4, N6, U6, R5, Y4, P1, P4, R6, M7, N7, AA3, U4, W2, W1, W3, V4, AA1, D10, J4, G10, D9	High	I/O	BVSEL
$\overline{\text{AACK}}$	U1	Low	Input	BVSEL
AP[0:4]	L5, L6, J1, H2, G5	High	I/O	BVSEL
$\overline{\text{ARTRY}}$[3]	T2	Low	I/O	BVSEL
AVDD	B2	–	Input	N/A
$\overline{\text{BG}}$	R3	Low	Input	BVSEL
$\overline{\text{BMODE0}}$[4]	C6	Low	Input	BVSEL
$\overline{\text{BMODE1}}$[5]	C4	Low	Input	BVSEL
$\overline{\text{BR}}$	K1	Low	Output	BVSEL
BVSEL[6][7]	G6	High	Input	N/A
$\overline{\text{CI}}$[3]	R1	Low	Output	BVSEL
$\overline{\text{CKSTP\_IN}}$	F3	Low	Input	BVSEL
$\overline{\text{CKSTP\_OUT}}$	K6	Low	Output	BVSEL
CLK_OUT	N1	High	Output	BVSEL
D[0:63]	AB15, T14, R14, AB13, V14, U14, AB14, W16, AA11, Y11, U12, W13, Y14, U13, T12, W12, AB12, R12, AA13, AB11, Y12, V11, T11, R11, W10, T10, W11, V10, R10, U10, AA10, U9, V7, T8, AB4, Y6, AB7, AA6, Y8, AA7, W8, AB10, AA16, AB16, AB17, Y18, AB18, Y16, AA18, W14, R13, W15, AA14, V16, W6, AA12, V6, AB9, AB6, R7, R9, AA9, AB8, W9	High	I/O	BVSEL
$\overline{\text{DBG}}$	V1	Low	Input	BVSEL
DP[0:7]	AA2, AB3, AB2, AA8, R8, W5, U8, AB5	High	I/O	BVSEL
$\overline{\text{DRDY}}$[8]	T6	Low	Output	BVSEL
DTI[0:3])[9]	P2, T5, U3, P6	High	Input	BVSEL
EXT_QUAL[10]	B9	High	Input	BVSEL
GBL	M4	Low	I/O	BVSEL
GND	A22, B1, B5, B12, B14, B16, B18, B20, C3, C9, C21, D7, D13, D15, D17, D19, E2, E5, E21, F10, F12, F14, F16, F19, G4, G7, G17, G21, H13, H15, H19, H5, J3, J10, J12, J14, J17, J21, K5, K9, K11, K13, K15, K19, L10, L12, L14, L17, L21, M3, M6, M9, M11, M13, M19, N10, N12, N14, N17, N21, P3, P9, P11, P13, P15, P19, R17, R21, T13, T15, T19, T4, T7, T9, U17, U21, V2, V5, V8, V12, V15, V19, W7, W17, W21, Y3, Y9, Y13, Y15, Y20, AA5, AA17, AB1, AB22	–	–	N/A
GV_{DD}[11]	B13, B15, B17, B19, B21, D12, D14, D16, D18, D21, E19, F13, F15, F17, F21, G19, H12, H14, H17, H21, J19, K17, K21, L19, M17, M21, N19, P17, P21, R15, R19, T17, T21, U19, V17, V21, W19, Y21	–	–	N/A
$\overline{\text{HIT}}$[8]	K2	Low	Output	BVSEL
$\overline{\text{HRESET}}$	A3	Low	Input	BVSEL

10. Substrate Capacitors for the PC7457, 483 CBGA

Figure 10-1 shows the connectivity of the substrate capacitor pads for the PC7457, 483 CBGA. All capacitors are 100 nF.

Figure 10-1. Substrate Bypass Capacitors for the PC7457, 483 CBGA

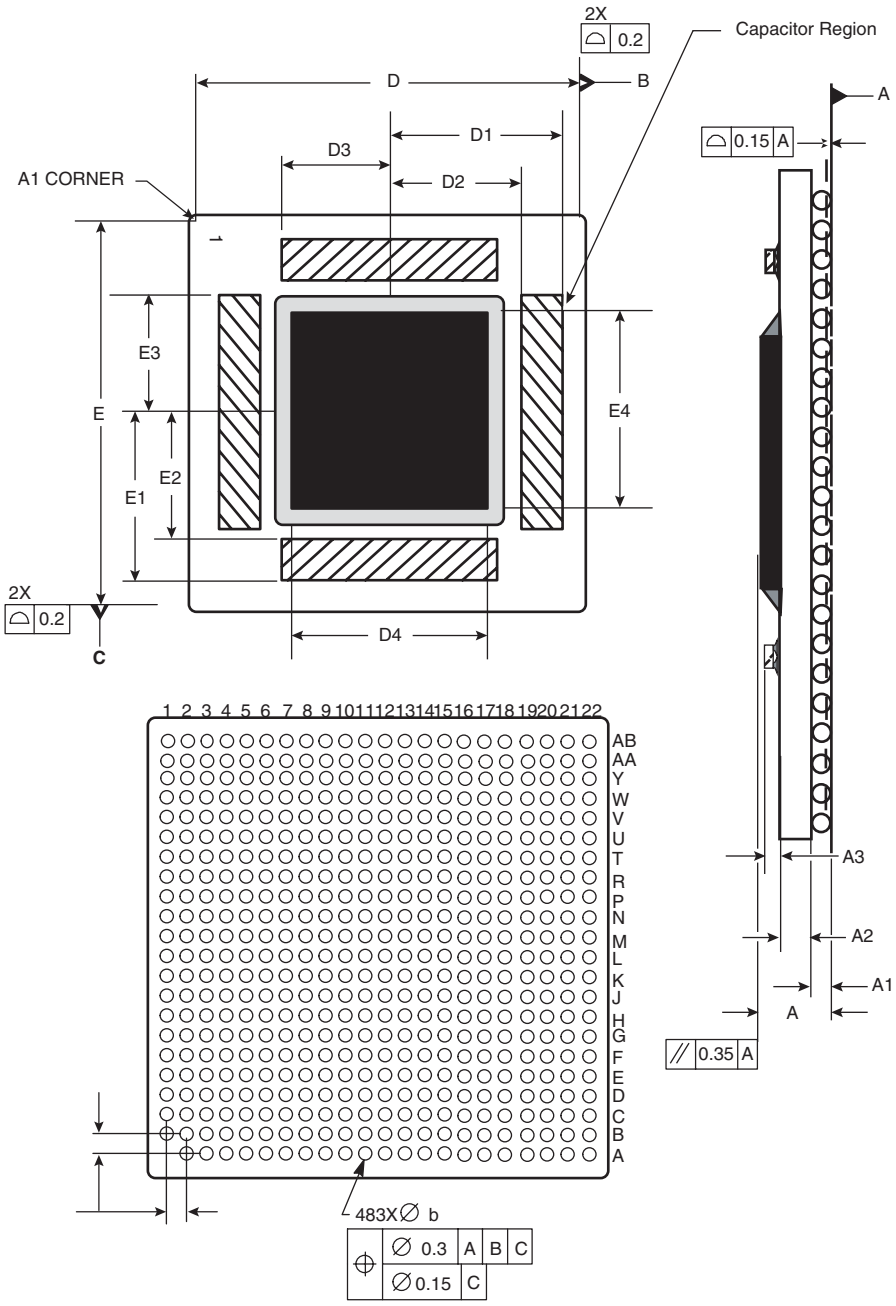


Capacitor	Pad Number	
	-1	-2
C1	GND	OV_{DD}
C2	GND	V_{DD}
C3	GND	GV_{DD}
C4	GND	V_{DD}
C5	GND	V_{DD}
C6	GND	GV_{DD}
C7	GND	V_{DD}
C8	GND	V_{DD}
C9	GND	GV_{DD}
C10	GND	V_{DD}
C11	GND	V_{DD}
C12	GND	GV_{DD}
C13	GND	V_{DD}
C14	GND	V_{DD}
C15	GND	V_{DD}
C16	GND	OV_{DD}
C17	GND	V_{DD}
C18	GND	OV_{DD}
C19	GND	V_{DD}
C20	GND	V_{DD}
C21	GND	OV_{DD}
C22	GND	V_{DD}
C23	GND	V_{DD}
C24	GND	V_{DD}

11. Mechanical Dimensions for the PC7457, 483 HCTE

Figure 11-1 provides the mechanical dimensions and bottom surface nomenclature for the PC7457, 483 HCTE package.

Figure 11-1. Mechanical Dimensions and Bottom Surface Nomenclature for the PC7457, 483 HCTE Package



	Millimeters	
DIM	MIN	MAX
A	2.72	3.20
A1	0.80	1
A2	1.10	1.30
A3	–	0.6
b	0.82	0.93
D	29 BSC	
D1	–	12.5
D2	8.5	–
D3	–	8.4
D4	10.9	11.1
e	1.27 BSC	
E	29 BSC	
E1	–	12.5
E2	8.5	–
E3	–	8.4
E4	9.55	9.75

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metallized feature with various shapes. Bottom side. A1 corner is designated with a ball missing from the array

3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly and the PLL is disabled. However, the bus interface unit requires a 2x clock to function. Therefore, an additional signal, EXT_QUAL, must be driven at one-half the frequency of SYSCLK and offset in phase to meet the required input setup t_{IVKH} and hold time t_{IXKH} (see Table 7-3 on page 22). The result is that the processor bus frequency is one-half SYSCLK while the internal processor is clocked at SYSCLK frequency. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the PC7455 regardless of the SYSCLK input.

15.1.2 L3 Clocks

The PC7457 generates the clock for the external L3 synchronous data SRAMs by dividing the core clock frequency of the PC7457. The core-to-L3 frequency divisor for the L3 PLL is selected through the L3_CLK bits of the L3CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the PC7457 core, and timing analysis of the circuit board routing. Table 15-2 shows various example L3 clock frequencies that can be obtained for a given set of core frequencies.

Table 15-2. Sample Core-to-L3 Frequencies[1]

Core Frequency (MHz)	÷2	÷2.5	÷3	÷3.5	÷4	÷4.5	÷5	÷5.5	÷6	÷6.5	÷7	÷7.5	÷8
500	250	200	167	143	125	111	100	91	83	77	71	67	63
533	266	213	178	152	133	118	107	97	89	82	76	71	67
550	275	220	183	157	138	122	110	100	92	85	79	73	69
600	300	240	200	171	150	133	120	109	100	92	86	80	75
650	325	260	217	186	163	144	130	118	108	100	93	87	81
666	333	266	222	190	167	148	133	121	111	102	95	89	83
700	350	280	233	200	175	156	140	127	117	108	100	93	88
733	367	293	244	209	183	163	147	133	122	113	105	98	92
800	400	320	266	230	200	178	160	145	133	123	114	107	100
866	433	347	289	248	217	192	173	157	145	133	124	115	108
933	467	373	311	266	233	207	187	170	156	144	133	124	117
1000	500	400	333	285	250	222	200	182	166	154	143	133	125
1050[2]	525	420	350	300	263	233	191	191	175	162	150	140	131
1100[2]	550	440	367	314	275	244	200	200	183	169	157	147	138
1150[2]	575	460	383	329	288	256	209	209	192	177	164	153	144
1200[2]	600	480	400	343	300	267	218	218	200	185	171	160	150
1250[2]	638	500	417	357	313	278	227	227	208	192	179	167	156
1300[2]	650	520	433	371	325	289	236	236	217	200	186	173	163

Notes:
1. The core and L3 frequencies are for reference only. Note that maximum L3 frequency is design dependent. Some examples may represent core or L3 frequencies which are not useful, not supported, or not tested for the PC7457; see "L3 Clock AC Specifications" on page 24 for valid L3_CLK frequencies and for more information regarding the maximum L3 frequency.
2. Not all core frequencies are supported by all speed grades; see Table 7-2 on page 20 for minimum and maximum core frequency specifications.

15.1.3 System Bus Clock (SYSCLK) and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 7-2 on page 20 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the PC7457 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the PC7457 is compatible with spread spectrum sources if the recommendations listed in Table 20 are observed.

Table 15-3. Spread Specturm Clock Source Recommendations (at Recommended Operating Conditions, see page 12.)

Parameter	Min	Max	Unit	Notes
Frequency modulation	–	50	kHz	(1)
Frequency spread	–	1.0	%	(1)(2)

Notes: 1. Guaranteed by design.

2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 7-2 on page 20.

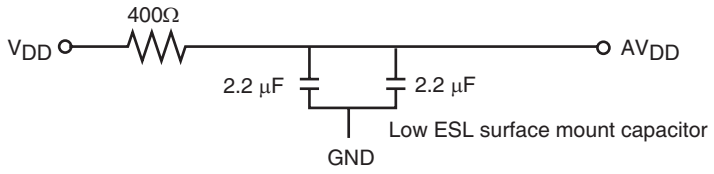
It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core or bus frequency should avoid violating the stated limits by using down-spreading only.

15.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the PC7457 to provide power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500_kHz to 10 MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 9-1 using surface mount capacitors with minimum effective series inductance (ESL) is recommended.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 CBGA footprint and very close to the periphery of the 483 CBGA footprint, without the inductance of vias.

Figure 15-1. PLL Power Supply Filter Circuit



Previous revisions of this document required a 400Ω resistor for Rev. 1.1 (Rev. B) devices instead of the 10Ω resistor shown above. All production devices require a 10Ω resistor. For more information, see the PC7450 Family Chip Errata for the PC7457 and PC7447.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Because the PC7457 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the PC7457 or by other receivers in the system. It is recommended that these signals be pulled up through weak (4.7 kΩ) pull-up resistors by the system, or that they may be otherwise driven by the system during inactive periods of the bus. The snooped address and transfer attribute inputs are A[0:35], AP[0:4], TT[0:4], $\overline{\text{CI}}$, $\overline{\text{WT}}$, and $\overline{\text{GBL}}$.

If extended addressing is not used, A[0:3] are unused and must be pulled low to GND through weak pull-down resistors. If the PC7457 is in 60x bus mode, DTI[0:3] must be pulled low to GND through weak pull-down resistors.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, don't require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are D[0:63] and DP[0:7].

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins don't require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, then all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

The L3 interface does not normally require pull-up resistors.

15.7 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 15-1 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. While Freescale recommends that the COP header be designed into the system as shown in Figure 15-1 on page 50, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 15-1 adds many benefits – breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface – and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 15-1; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 15-1 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 15-1 is usually connected to the PCI bridge chip in a system and is an input to the PC7457 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the PC7457 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is deasserted when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged via logic so that it also can be driven by the PCI bridge.

18. Document Revision History

Table 18-1 provides a revision history for this hardware specification.

Table 18-1. Document Revision History

Revision Number	Date	Substantive Change(s)
D	03/06	Remove PC7447. Modification Table 6-1 on page 13? and ordering information
C	06/2005	Updated document to new Atmel template
		Updated section numbering and changed reference from part number specifications to addendums
		Added Rev. 1.2 devices, including increased L3 clock max frequency to 250 MHz and improved L3 AC timing
		Table 6-2 on page 13: Added CTE information
		Table 7-2 on page 20: Modified jitter specifications to conform to JEDEC standards, changed jitter specification to cycle-to-cycle jitter (instead of long- and short-term jitter); changed jitter bandwidth recommendations
		Table 7-7 on page 29: Deleted note 9 and renumbered.
		Table 7-8 on page 31: Deleted note 5 and renumbered
		Table 8-1 on page 38: Revised note 6
		Added Section 15.1.3 ”System Bus Clock (SYSCLK) and Spread Spectrum Sources” on page 50
		Section 15.2 ”PLL Power Supply Filtering” on page 50: Changed filter resistor recommendations. Recommend 10Ω resistor for all production devices, including production Rev. 1.1 devices. 400Ω resistor needed only for early Rev. 1.1 devices.
		Table 18-1: Reversed the order of revision numbers.
		Section 15.1.1 on page 47: Corrected note regarding different PLL configurations for earlier devices; all PC7457 devices to date conform to this table
		Section 15.6 on page 52: Added information about unused L3_ADDR signals.
		HCTE package information
		Preliminary specification α-site release subsequent to preliminary specification β-site Motorola changed to Freescale
B	11/2004	Figure 7-3 on page 22: Corrected pin lists for input and output AC timing to correctly show $\overline{\text{HIT}}$ as an output-only signal
		Added specifications for 1267 MHz devices; removed specs for 1300 MHz devices.
		Changed recommendations regarding use of L3 clock jitter in AC timing analysis in Section “L3 Clock AC Specifications” on page 24; the L3 jitter is now fully comprehended in the AC timing specs and does not need to be included in the timing analysis

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