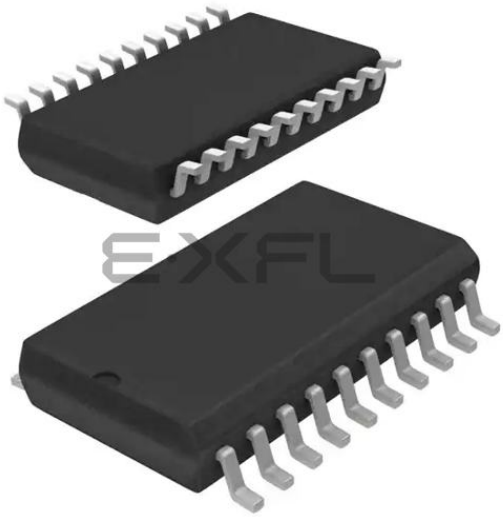

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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	SaTCR LNBs and Switchers
Core Processor	STM8
Program Memory Type	-
Controller Series	-
RAM Size	-
Interface	DiSEqC, I²C
Number of I/O	-
Voltage - Supply	2.95V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8splnb1m6

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1.1.1 Pins description

Figure 3. TSSOP20/SO20W pinout

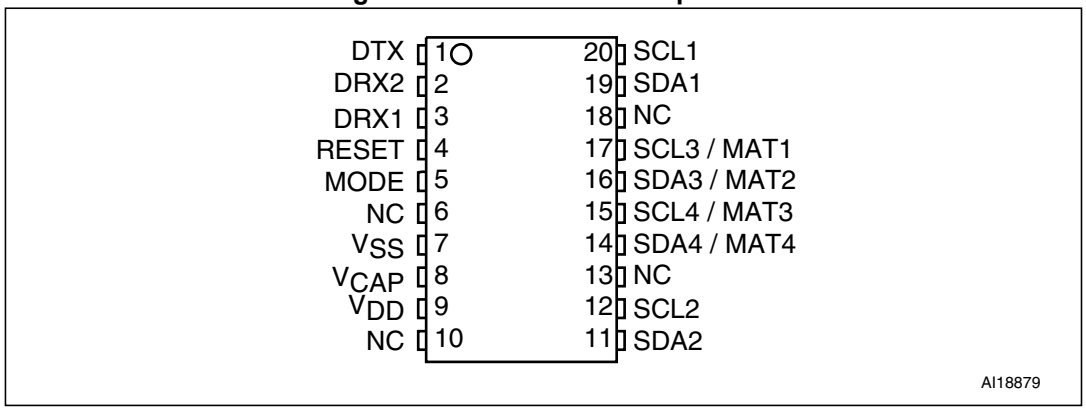


Figure 4. UFQFPN20 pinout

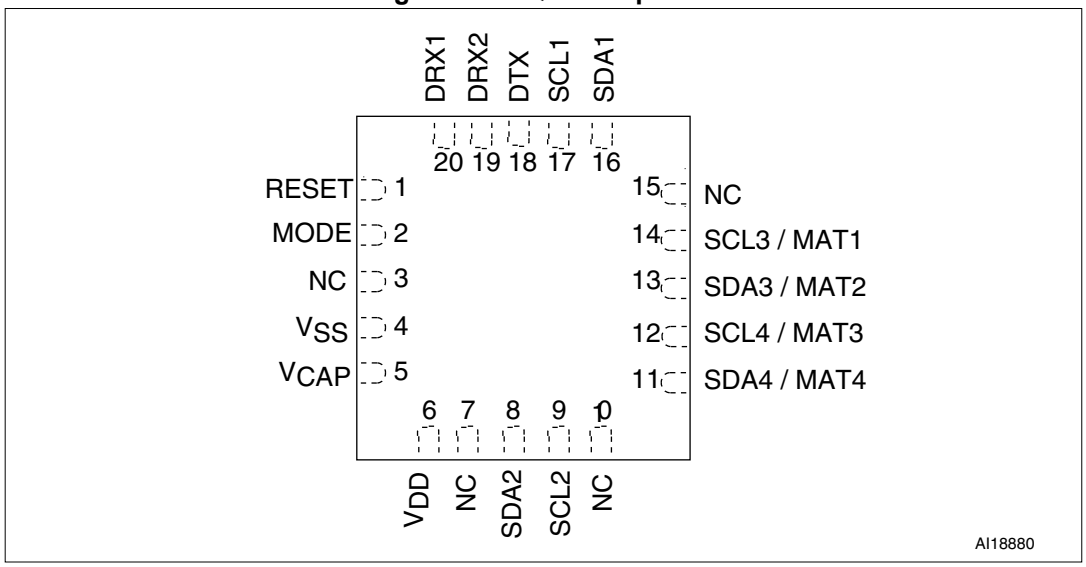


Table 1. STM8SPLNB1 pins description

pin no. TSSOP20 /SO20W	pin no. UFQFPN20	pin name	description	note
9	6	V_{DD}	+5 V power supply	+/- 10 % tolerance
7	4	V_{SS}	ground	_
4	1	RESET	device reset	0.1 µF capacitor to ground (active low)
8	5	V_{CAP}	filtering capacitor	1 µF capacitor to ground
3	20	DRX1	DiSEqC receive data input 2	HF signal after low pass filtering
2	19	DRX2	DiSEqC receive data input 2	HF signal after low pass filtering - secondary channel (less priority - see later description)

1. Selection of incremental order mode: *pin MODE* (see *Table 1: STM8SPLNB1 pins description*) is left open or I2C addressing mode EEPROM parameter (see *Table 14: STM8SPLNB1 EEPROM parameters*) is set to 1.

Another option is to decrease number of I^2C channels and use the remaining pins for legacy matrix LNB control - e.g. to have 2 I^2C channels (4 pins) and 4 legacy matrix output pins - see *Table 16: Application types*.

Operation mode and device behavior depends from final hardware configuration. This behavior is selected through configuration parameters - see *Table 14: STM8SPLNB1 EEPROM parameters*.

Note: Advantage of using incremental order mode is in applications with up to 4 SaTCRs - which is common in practice. Then each SaTCR owns one I^2C bus. I2C communication with another SaTCRs is running on different I^2C bus - so it does not disturb HF signal on given SaTCR (SaTCR is sensitive to I^2C bus signal transients).
Advantage of using ST7LNB1 compatible mode is in applications where is used SaTCRs control together with legacy matrix outputs (MAT1-MAT4) - see Section 1.1.1: Pins description. In this case there remains free only 2 I^2C buses for SaTCRs control (MAT1-MAT4 pins occupy I^2C3 and I^2C4 bus). In ST7LNB1 compatible mode 2 I^2C buses can address up to 4 SaTCRs - 2 SaTCRs per I^2C bus. Disadvantage is the I^2C bus disturbance to SaTCR which is not addressed - shared I^2C bus (HF filters on I^2C buses is recommended).

2.1 Supported DiSEqC commands

In the following *Table 4: STM8SPLNB1 DiSEqC™ supported commands* are listed DiSEqC commands supported by STM8SPLNB1. For more details about commands, refer to the *DiSEqC™ slave microcontroller specifications* at www.eutelsat.com.

Table 4. STM8SPLNB1 DiSEqC™ supported commands

command number	command name	function
0x00	RESET	Reset DiSEqC™ microcontroller
0x0D	config read	Read configuration parameters from EEPROM
0x0F	config write	Write configuration parameters to EEPROM
0x38	write to port	DiSEqC 1.0: Write to port group command - Legacy commands
0x5A	operation command	DiSEqC-ST normal operation commands: ODU_Changechannel or ODU_SatCROFF
0x5B	installation command	DiSEqC-ST installation commands: ODU_Config, ODU_EEPvar.LOFREQ or ODU_SatCRxON

2.2.4 Command 0x38

This command is used to write to port group command - legacy support.

For application supporting the legacy (except for application number 1), the backwards signaling (13/18 V, 22 kHz tone) is recognized until a valid DiSEqC 1.0 command is detected.

The following *Table 8: Command 0x38 format* presents the truth table for the legacy commands.

Table 8. Command 0x38 format

command	equivalent backward signalling	selected feed	band	polarity	satellite
E0 xx 38 F0	13V / 0kHz	0	Low	Vertical	A
E0 xx 38 F1	13V / 22kHz	1	High	Vertical	A
E0 xx 38 F2	18V / 0kHz	2	Low	Horizontal	A
E0 xx 38 F3	18V / 22kHz	3	High	Horizontal	A

2.2.5 Command 0x5A

This command is used during LNB (or switched) normal operation (default operation after configuration). Command 0x5A is DiSEqC command (see *Table 9: Command 0x5A format*) with two data bytes. In dependence from those data bytes are performed two subcommands which descriptions are in *Table 10: Subcommands 0x5A format - ODU_SaTCR_Op*.

Table 9. Command 0x5A format

frame	DiSEqC™ address	command	data1	data2
0xE0/0xE2	[device address]	0x5A	[data1](1)	[data2](1)

1. See *Table 10: Subcommands 0x5A format - ODU_SaTCR_Op* for details.

Table 10. Subcommands 0x5A format - ODU_SaTCR_Op

subcommand	data1			data2	description
	[7:5]	[4:2]	[1:0]	[7:0]	
ODU_ChangeChannel	SaTCR(1)	Feed(2)	Tun[9:8](3)	Tun[7:0](3)	This command is used for the channel selection.
ODU_PowerOff	SaTCR(1)	0		0x00	This command is used to put a SaTCR in low power mode.

1. SaTCR number - see *Table 2: SaTCRs implementation - ST7LNB1 compatible mode*.
2. Feed parameter - see *Table 11: Feeds* and *Table 15: Truth table for support of 8 RF inputs*.
3. Tuning word - see notes in *Table 14: STM8SPLNB1 EEPROM parameters* for description.

Table 14. STM8SPLNB1 EEPROM parameters (continued)

index	parameter	description	default value
12	AppliNum	Application number (refer to *Table 17: DiSEqC Applications*)	0x04
13	High L.O freq Number	Refer to *Table 18: Local oscillator frequencies*	0x04
14	Low L.O freq Number	Refer to *Table 18: Local oscillator frequencies*	0x02
15	SaTCR1 matrix truth table	(4)	0xAC
16			0x35
17	SaTCR2 matrix truth table		0x59
18			0x6A
19	SaTCR3 matrix truth table		0x56
1A			0x9A
1B	SaTCR4 matrix truth table		0x95
1C			0xA6
1D	SaTCR5 matrix truth table		0xFF
1E			0xFF
1F	SaTCR6 matrix truth table		0xFF
20			0xFF
21	SaTCR7 matrix truth table		0xFF
22			0xFF
23	SaTCR8 matrix truth table / legacy matrix		0xFF
24			0xFF
25	SaTCRs GAIN(5)	SaTCRs 1 to 4 Gain	0xFF
26		SaTCRs 5 to 8 Gain	0xFF
27	SaTCRs number	(6)	0x04
28	I^2C addressing mode	defines SaTCRs assignment to I^2C bus(7)	0x00
29	Software Version Number	version number identification	0x15
2A	Reserved	(8)	0x00
2B			0x00

1. Address 0x00 is also recognized as valid address.
2. SaTCRx BPF = BPFx center frequency [MHz]/2.

Table 18. Local oscillator frequencies

LofreqNum (hex)		Local oscillator frequency
Standard RF band	0x00	none
	0x01	not known
	0x02	9.750 GHz
	0x03	10.000 GHz
	0x04	10.600 GHz
	0x05	10.750 GHz
	0x06	11.000 GHz
	0x07	11.250 GHz
	0x08	11.475 GHz
	0x09	20.250 GHz
	0x0A	5.150 GHz
	0x0B	1.585 GHz
	0x0C	13.850 GHz
	0x0D	not allocated
	0x0E	not allocated
	0x0F	not allocated
Wide RF band	0x10	not allocated
	0x11	10.000 GHz
	0x12	10.200 GHz
	0x13	13.250 GHz
	0x14	13.450 GHz
	0x15 - 0x1F	not allocated

4 Electrical characteristics

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

4.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 Σ).

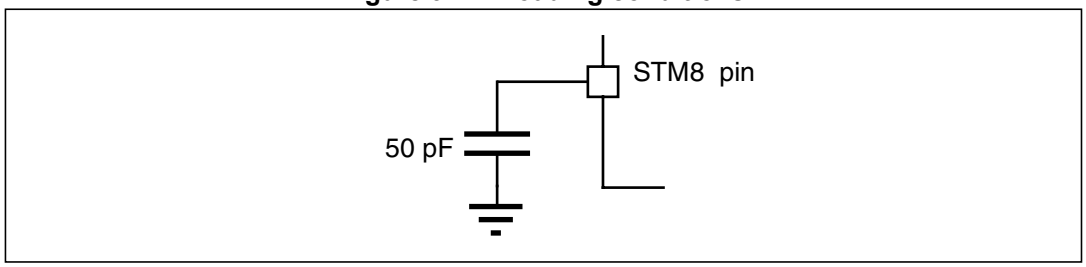
4.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5 V. They are given only as design guidelines and are not tested.

4.1.3 Loading capacitor

The loading conditions used for pin parameter measurement are shown in the following figure.

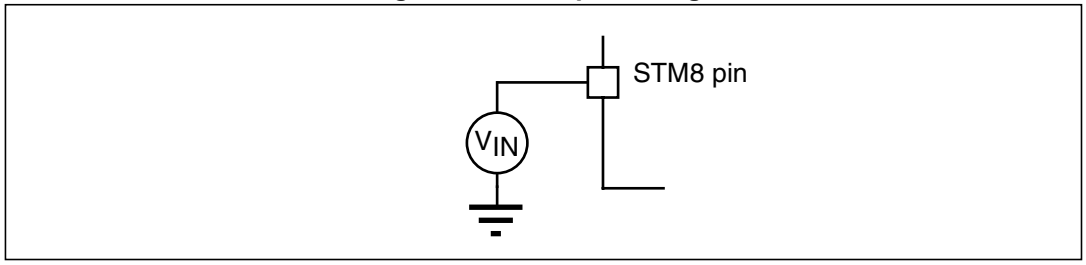
Figure 9. Pin loading conditions



4.1.4 Pin input voltage

The input voltage measurement on a pin of the device is described in the following figure.

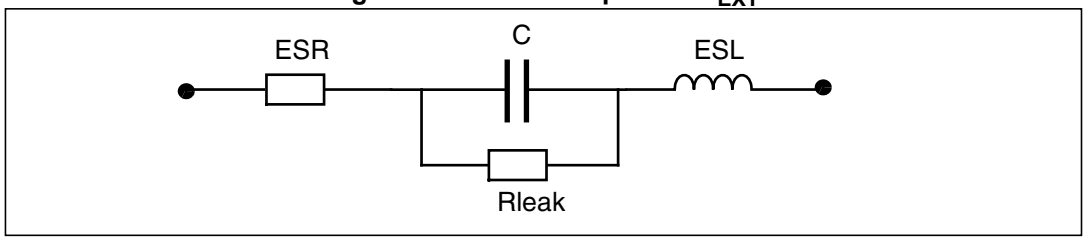
Figure 10. Pin input voltage



4.3.2 V_{CAP} external capacitor

Stabilization for the internal voltage regulator is achieved connecting an external capacitor C_{EXT} to the V_{CAP} pin (see *Figure 2: STM8SPLNB1 typical configuration*). C_{EXT} is specified in *Table 22: General operating conditions*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 11. External capacitor C_{EXT}



1. ESR is the equivalent series resistance and ESL is the equivalent inductance.

4.3.3 Supply current characteristics

Total current consumption in run mode

The MCU is placed under the following conditions:

– All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)

Subject to general operating conditions for V_{DD} and T_A.

Table 24. Total current consumption at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in run mode	f_{CPU} = 16 MHz, V_{DD} = 5V	HSI RC osc. (16 MHz)	4.7	5.8	mA
		f_{CPU} = 16 MHz, V_{DD} = 3.3V	HSI RC osc. (16 MHz)	4.7	5.8	
$I_{DD(R)}$	Supply current in reset state(2)	V_{DD} = 5 V	-	400	-	µA

1. Data based on characterization results, not tested in production.
2. Characterized with all I/Os tied to V_{SS}.

Table 25. Output driving current

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level	I_{IO} = 10 mA, V_{DD} = 5 V	-	2	V
		I_{IO} = 4 mA, V_{DD} = 3.3 V	-	1(1)	
V_{OH}	Output high level	I_{IO} = 10 mA, V_{DD} = 5 V	2.8	-	
		I_{IO} = 4 mA, V_{DD} = 3.3 V	2.1(1)	-	

1. Data based on characterization results, not tested in production

Static latch up

Two complementary static tests are required on ten parts to assess the latch up performance:

- A supply overvoltage (applied to each power supply pin)
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch up standard. For more details, refer to the application note AN1181.

Table 30. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch up class	$T_A = 25$ °C	A
		$T_A = 85$ °C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

5 Package information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.2 Package mechanical data

5.2.1 TSSOP package mechanical data

Figure 13. 20-pin, 4.40 mm body, 0.65 mm pitch

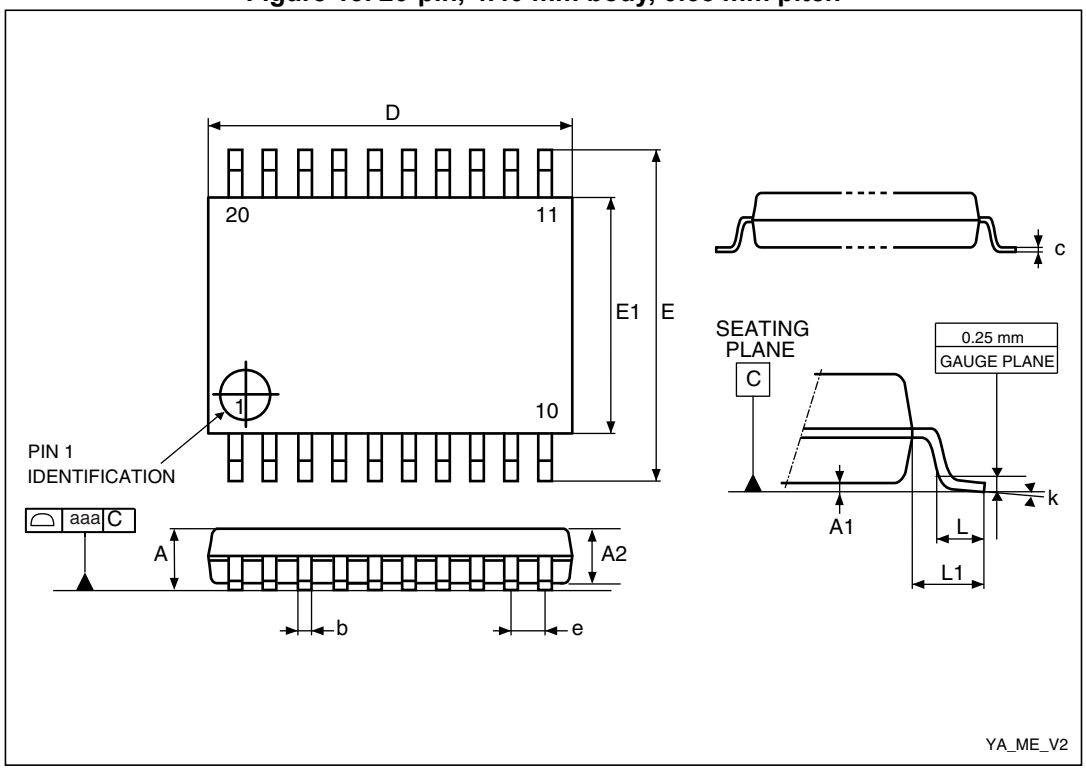


Table 31. 20-pin, 4.40 mm body, 0.65 mm pitch mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D[2]	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1[3]	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-

Table 31. 20-pin, 4.40 mm body, 0.65 mm pitch mechanical data (continued)

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
k	0.0°	-	8.0°	0.0°	-	8.0°
aaa	0.100			0.0039		

1. Values in inches are converted from mm and rounded to 4 decimal digits
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 14. TSSOP20 recommended footprint

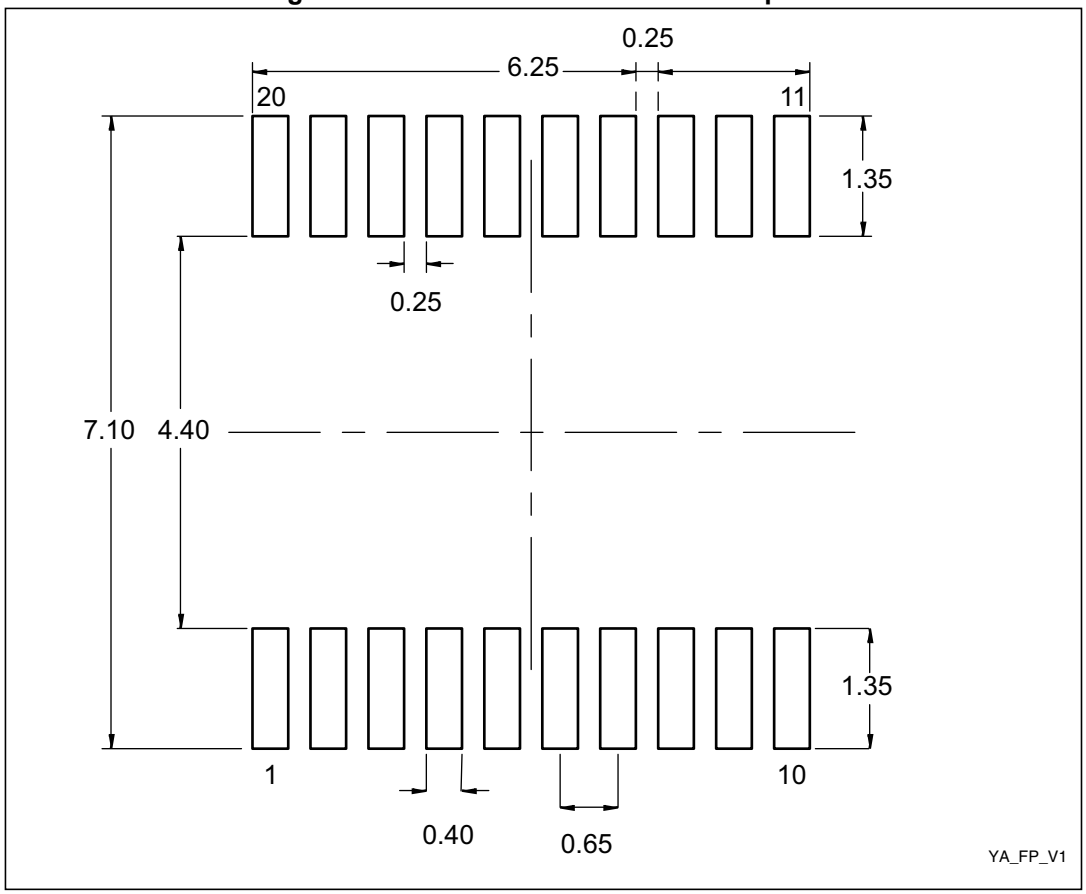
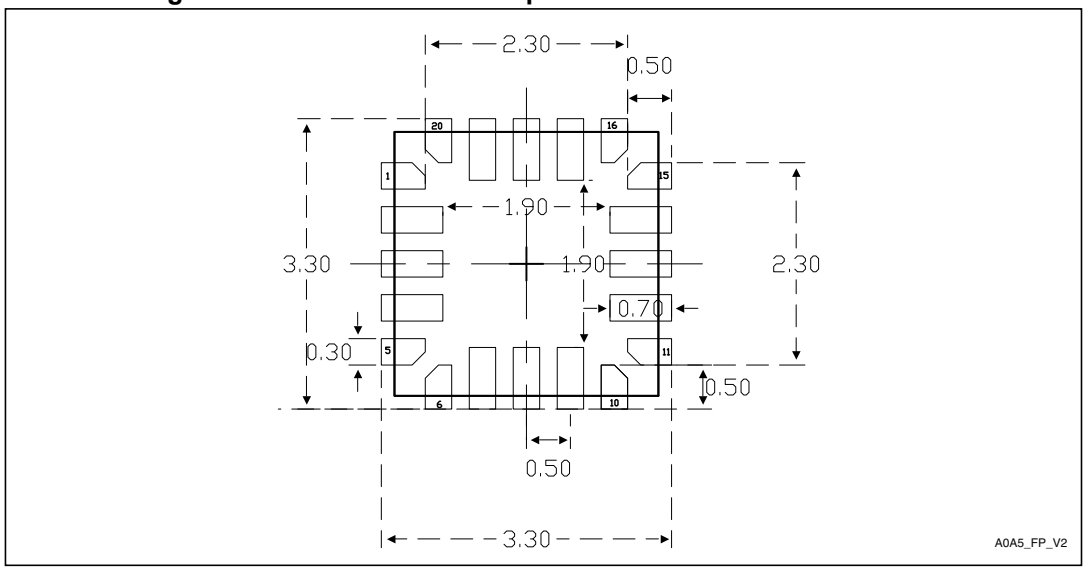


Figure 18. Recommended footprint without on-board emulation



1. Drawing is not to scale
2. Dimensions are in millimeters

5.3 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 22: General operating conditions*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 34. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient TSSOP20 - 4.4 mm	84	°C/W
	Thermal resistance junction-ambient SO20W - (300 mils)	91	
	Thermal resistance junction-ambient UFQFPN20 - 3 x 3 mm	90	

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

5.3.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

A.1.3 Data transfer on coaxial cable

The 22 kHz signal is also used for data communication through coaxial cable (bidirectional transfer). In this case is used amplitude modulation of 22 kHz signal.

Bit “logical 0” coding:

- 1.0 ms 22 kHz signal
- 0.5 ms no signal

Bit “logical 0” coding:

- 0.5 ms 22 kHz signal
- 1.0 ms no signal

By this modulation is transferred full DiSEqC™ message (8 bits per byte + parity, several bytes in message - see *A.1: Physical layer*).

Figure 20. DiSEqC™ bit modulation

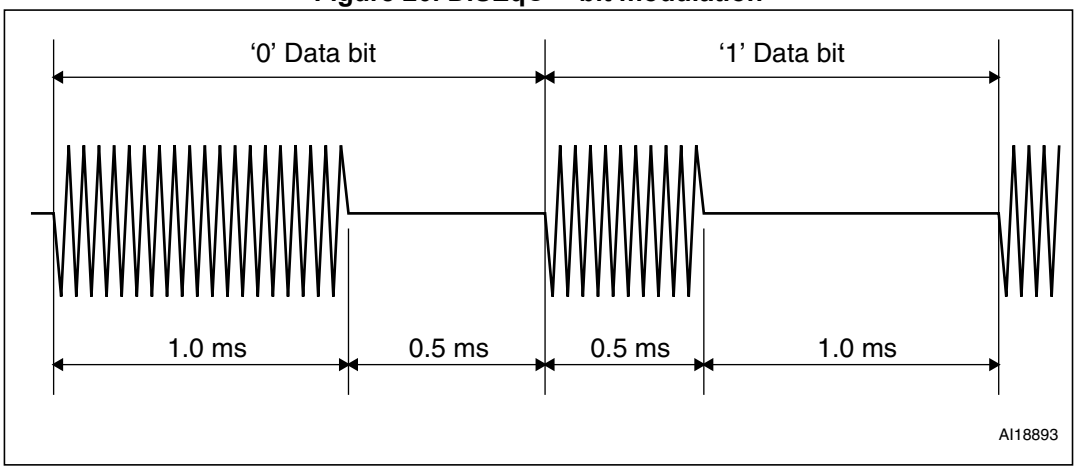
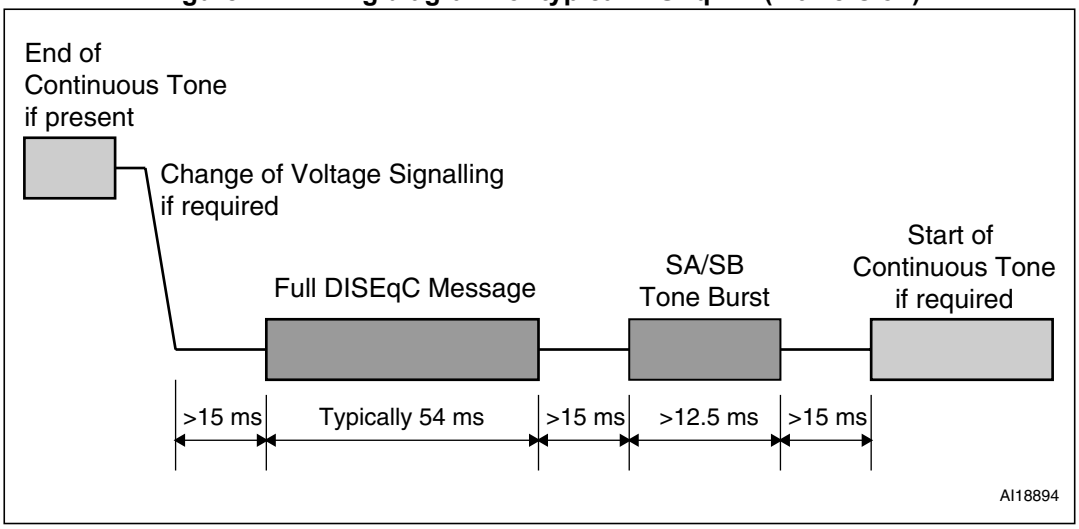


Figure 21. Timing diagram for typical DiSEqC™ (1.0 version)



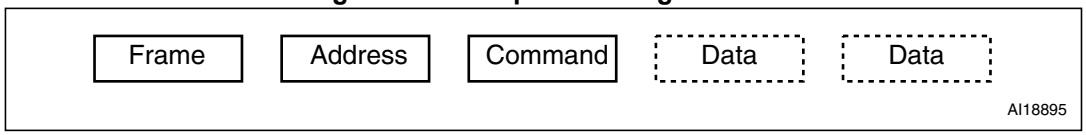
For more detailed information about DiSEqC™ protocol - see *DiSEqC™ bus functional specifications* and *DiSEqC™ slave microcontroller specifications.* Refer to www.eutelsat.com.

A.2 Protocol layer

The DiSEqC™ messages are transferred in packets. One packet consists from several bytes - each byte has 8 bits followed by parity bit (odd).

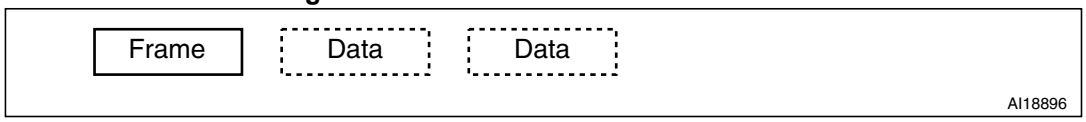
The full DiSEqC™ message contains a frame byte, an address byte, a command byte which can be followed by several data bytes.

Figure 22. DiSEqC™ message format



When host is requesting an answer from the slave (microcontroller) then the answer consists from frame byte which can be followed by several data bytes

Figure 23. Microcontroller answer format.



The frame byte identifies the direction, reply requirements and error status - see following *Table 35.*

Table 35. DiSEqC™ frame byte definition

Frame byte	definition
0xE0	Command from master, no reply required, first transmission
0xE1	Command from master, no reply required, repeated transmission
0xE2	Command from master, reply required, first transmission
0xE3	Command from master, reply required, repeated transmission
0xE4	Reply from slave, OK, no errors found
0xE5	Reply from slave, command not supported
0xE6	Reply from slave, parity error, repeat requested
0xE7	Reply from slave, command not recognized, repeat necessary

The address byte identifies the receiver. There also exist address groups (families). The family address is valid for all devices with similar (family) function - all given family devices receive message. Address families are described in *DiSEqC™ slave microcontroller specifications*. Universal (broadcast) address is 0x00 - all devices should receive messages with this address.

Command byte describes given command for device - according this command the device selects method for data processing.

Optional data bytes are data for given command. Data in answer (from slave) specify required information. There is specified data byte format only for 3 required bytes from slave:

- Status byte (bus collision, reset status, standby status, supply voltage)
- Configuration byte (more detailed information about current slave configuration)
- Switches byte (describes status of the committed switches)

For more information about format of those 3 data bytes refer to *DiSEqC™ slave microcontroller specifications* available at www.eutelsat.com (and *Table 4: STM8SPLNB1 DiSEqC™ supported commands*).

7 Revision history

Table 36. Document revision history

Date	Revision	Changes
28-Jul-2011	1	Initial release.
08-Sep-2011	2	Updated RESET capacitor value in *Figure 2: STM8SPLNB1 typical configuration*. Updated AppliNum and SaTCRs number parameters. Added note on V_{CAP} parameter in *Table 22: General operating conditions*.
03-Nov-2011	3	Updated datasheet description. Updated conditions and notes related to V_{CAP} parameter in *Table 22: General operating conditions*.
11-Jun-2012	4	Updated typical and maximum values of R_{PU} in *Table 26: RESET pin characteristics*. Modified *Figure 16: 20-lead, ultra thin, fine pitch quad flat no-lead package outline (3 x 3)* to add package top view.
18-Dec-2014	5	Updated: – *Section 5.2.1: TSSOP package mechanical data*, – *Section 5.2.2: SO20W package mechanical data*, – *Section 5.2.3: UFQFPN package mechanical data*.